Computer Architecture Project

Project Description

In this project, you are required to implement a GPIO controller and UART controller connected to the APB bus in Verilog. The code should be synthesizable and tested.

APB is one of the AMBA buses that has no arbitration as it is a single bus. Figure 1 shows an example of data transfer on the APB bus.

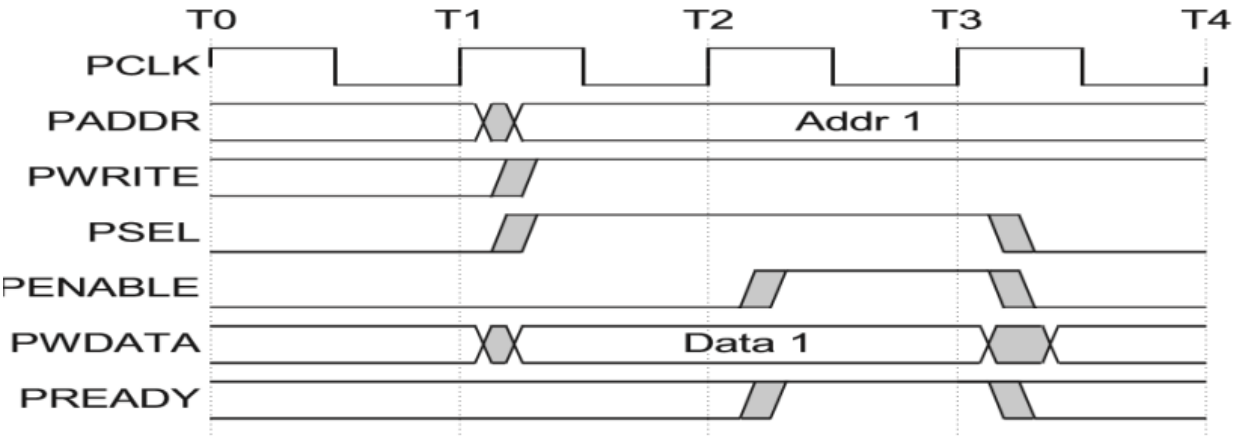

Figure 1: Write transfer on APB bus

The **UART controller** handles the asynchronous serial communication between a computer and a peripheral device connected to the serial port of the computer and converts data from serial to parallel and vice-versa.

From the functions of the UART:

- Converts parallel data into serial data for outbound communications
- Converts serial data into parallel data for inbound communications

UART has many registers to set needed configurations, such as baud rate. Figure 2 shows an example of a uart block that receives data from APB bus and converts it into a serial stream.

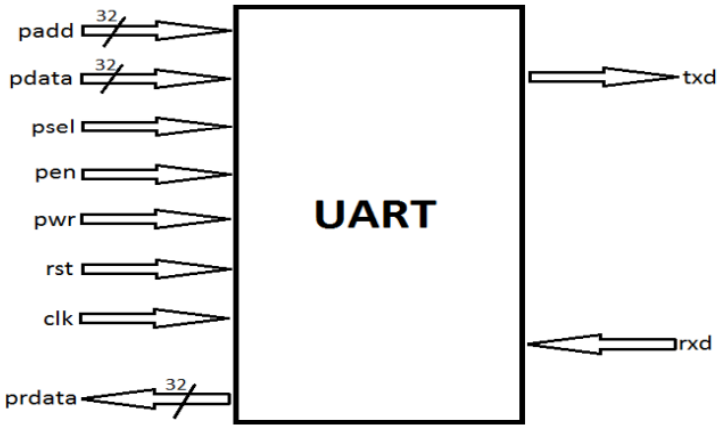

Figure 2: UART block diagram that has APB interface

The **GPIO controller** is used to configure the pins of the microcontroller to be either input (which means external devices can feed data through these pins) or output (which means that data can be produced on these pins). Usually, pins are grouped into 8 pins to make a port. GPIO controller has many categories of registers such as a control register to control the direction of the pins and a data register that has the value that will be produced on the pins.

Required

The students should be divided into groups/teams of max 6 members.

Expected delivery

1. Each group should deliver the following.
    a. A **report** in pdf format describing the project details (e.g., block diagram, signals description, and implementation).
    b. The **source code** of the project and the **testbench** used to verify it.
    c. **5-minute presentation** per each group. All the team/group members should participate in the presentation.
2. The report should contain.
    a. Cover with team member names and team members IDs.
    b. Table of contents.
    c. Block Diagram for your design.
    d. Description for all signals used in your design in tabular format (signal, description).
    e. Brief description of the testing strategy.
    f. Snap shots of simulation waves.
    g. A part that describes the work for each team member (who did what).
    h. Any additional information, such as enhancements made in the implementation.

    i. Any figure in the pdf should have a caption under it and any existing figure should be referred in the written paragraphs.
3. Presentation should contain brief description about the done work associated with waveforms screenshots and live demo.
4. Report, source code, and test bench (not the presentation) should be delivered in a zip file that will be uploaded on LMS.

Delivery deadline date

1. The deadline of delivery date will be on **29th Dec.** at **11:59 PM**. The submission will be through LMS.
2. The presentations will be held on these preliminary dates **30th Dec.** and **31st Dec.** (the final dates will be announced later).

Competition

The best three projects will take financial prizes.

1. The first prize would be 3000 L.E for the best winning team.
2. The second team will get 2000 L.E.
3. The third team will get 1000 L.E.