Assignment 1 – Clock Management in STM32 Microcontrollers (English Version)

This assignment focuses on understanding the clock management system (RCC) in STM32 microcontrollers and how different clock sources, PLL, and bus configurations (AHB, APB) work together to provide flexibility, accuracy, and power efficiency.

a) Internal Clock Configuration Modes

STM32 microcontrollers have several main sources for clock generation:
1. HSI (High Speed Internal): An internal oscillator (usually 8 or 16 MHz) that starts quickly and requires no external components.
2. HSE (High Speed External): An external crystal or oscillator that provides high accuracy but requires extra components.
3. LSI (Low Speed Internal): An internal 32 kHz oscillator used mainly for the independent watchdog (IWDG) and low-power timing.
4. LSE (Low Speed External): A 32.768 kHz external crystal used for accurate RTC (Real-Time Clock) operation.
5. PLL (Phase-Locked Loop): A frequency multiplier circuit used to increase the clock frequency for the CPU and system buses.

b) Clock Paths in STM32F1 Series

In STM32F1 series, there are three main clock input paths:
1. HSI (internal clock)
2. HSE (external clock)
3. PLL (derived from HSI or HSE)
Having multiple clock paths ensures flexibility and reliability. If one source fails, another can take over. It also allows designers to balance between accuracy, power consumption, and startup time.

c) Increasing Internal Clock Frequency

To achieve a higher system frequency than the input clock, the PLL (Phase-Locked Loop) unit is used. PLL multiplies the input frequency (from HSE or HSI) by a programmable factor to generate a higher output frequency, which can then be distributed to the CPU and peripheral buses.

d) Enable CSS Option

The CSS (Clock Security System) feature is used to improve system reliability. When enabled, CSS monitors the external clock source (HSE). If a fault is detected, the system automatically switches to the internal HSI clock to prevent system failure or freeze.

e) AHB and APB Buses

After the system clock (SYSCLK) is generated, it is distributed through various buses:
- AHB (Advanced High-performance Bus): Connects the CPU, memory, and DMA with high

speed.
- APB1 and APB2 (Advanced Peripheral Bus): Used for slower peripherals.
  - APB1: For low-speed peripherals such as UART, I2C, CAN, and timers (TIM2–TIM7).
  - APB2: For high-speed peripherals such as ADC, SPI1, TIM1, and GPIOs.

This multi-bus architecture helps manage power consumption while ensuring optimal performance for each peripheral group.

Conclusion

Proper clock management in STM32 microcontrollers is essential for stable and efficient operation. By choosing suitable clock sources, using PLL for frequency scaling, and enabling CSS for protection, developers can achieve the right balance between accuracy, performance, and power consumption.