Final Project Report

High-Level Synthesis (HLS) Implementation

on Zynq Hardware

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Course:

System-Level Design Laboratory

Contents

1. Introduction

This report presents the re-implementation and evaluation of six digital design experiments that were originally developed in SystemC. The designs are now migrated to the hardware design flow using Vivado HLS and deployed on the Xilinx Zynq-7000 platform.

For each experiment:
- The problem statement and objectives are introduced.
- The C++/HLS implementation and applied pragmas are explained.
- A testbench validates the design functionality.
- Finally, synthesis reports are analyzed, including resource usage (LUT, FF, BRAM), latency, and timing results.

Target Device: xc7z020clg400-1 (Zynq-7000)

2. Experiment 1: XOR Gate

Objective: Implement and simulate a simple logical XOR gate in C++ using HLS.

- Files: xor_gate.h, xor_gate.cpp, xor_gate_tb.cpp
- Testbench validates all four input combinations.
- Synthesis Results: Only 2 LUTs used, negligible delay, minimal hardware footprint.

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================================================================
== Vivado HLS Report for 'xor_gate'
================================================================
* Date:           Tue Aug  5 18:38:30 2025

* Version:        2019.1 (Build 2552052 on Fri May 24 15:28:33 MDT 2019)
* Project:        xor_hls_project
* Solution:       xor_solution
* Product family: zynq
* Target device:  xc7z020-clg400-1


================================================================
== Performance Estimates
================================================================
+ Timing (ns):
    * Summary:
    +--------+-------+----------+------------+
    |  Clock | Target| Estimated| Uncertainty|
    +--------+-------+----------+------------+
    |ap_clk  |  10.00|     0.978|        1.25|
    +--------+-------+----------+------------+

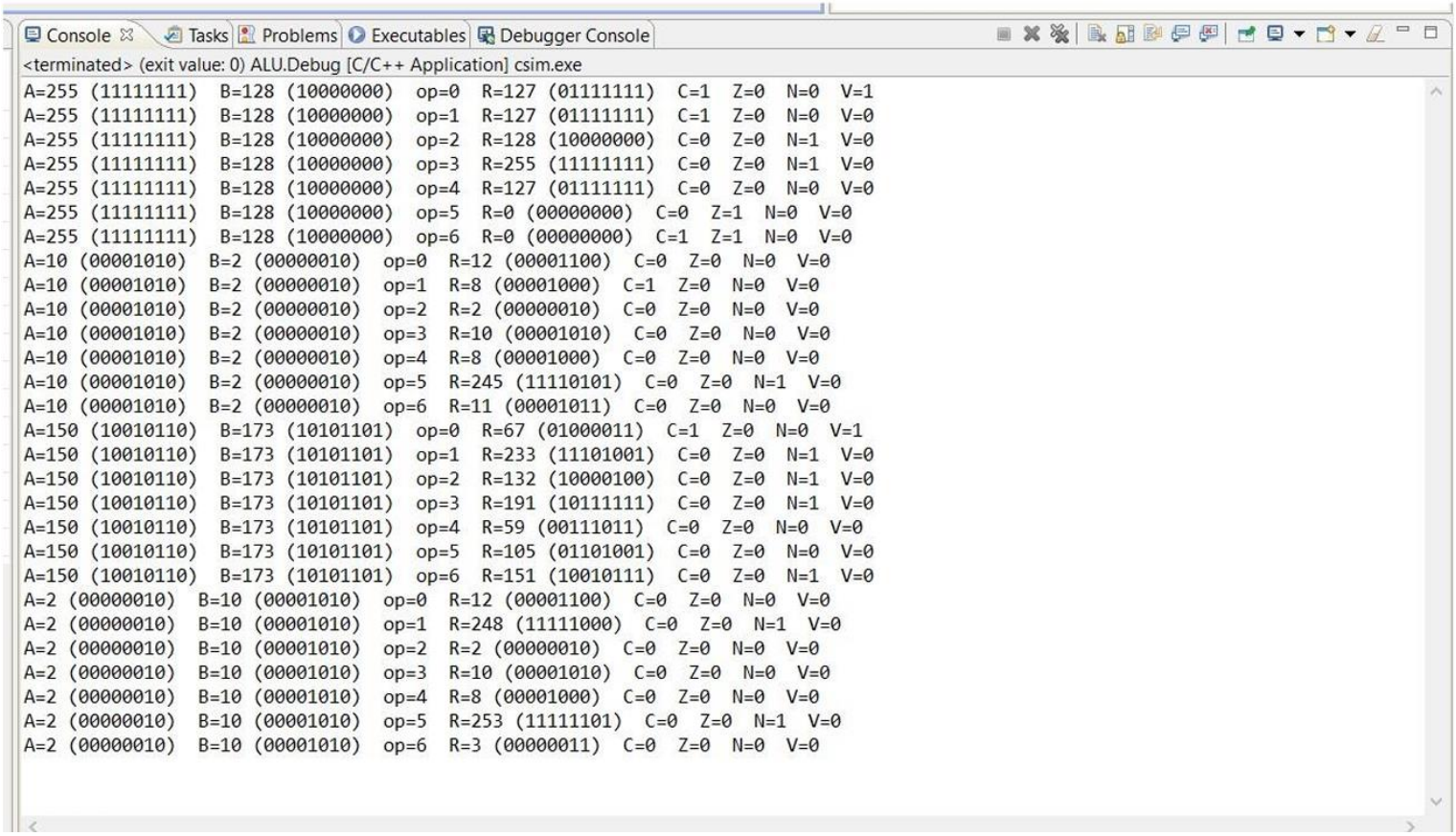
+ Latency (clock cycles):
    * Summary:
    +-----+-----+-----+-----+---------+
    |  Latency  |  Interval | Pipeline|
    | min | max | min | max |   Type  |
    +-----+-----+-----+-----+---------+
    |    0|    0|    0|    0|   none  |
    +-----+-----+-----+-----+---------+

================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-------+--------+-------+-----+
|       Name      | BRAM_18K| DSP48E|   FF   |  LUT  | URAM|
+-----------------+---------+-------+--------+-------+-----+
|DSP              |        -|      -|       -|      -|    -|
|Expression       |        -|      -|       0|      2|    -|
|FIFO             |        -|      -|       -|      -|    -|
|Instance         |        -|      -|       -|      -|    -|
|Memory           |        -|      -|       -|      -|    -|
|Multiplexer      |        -|      -|       -|      -|    -|
|Register         |        -|      -|       -|      -|    -|
+-----------------+---------+-------+--------+-------+-----+
|Total            |        0|      0|       0|      2|    0|
+-----------------+---------+-------+--------+-------+-----+
|Available        |      280|    220|  106400|  53200|    0|
+-----------------+---------+-------+--------+-------+-----+
|Utilization (%)  |        0|      0|       0|   ~0  |    0|
```

3. Experiment 2: Arithmetic Logic Unit (ALU)

Objective: Implement an 8-bit ALU supporting arithmetic and logical operations with condition flags.

- Inputs/Outputs: Two 8-bit inputs (A, B), 3-bit opcode, Result R (8-bit), Flags (C, Z, N, V)
- Supported Operations: ADD, SUB, AND, OR, XOR, NOT, INC
- Testbench: Validates overflow and borrow conditions.
- Synthesis Results: Single-cycle latency, clock ≈ 3.98 ns, very low resource usage.



```
================================================================
== Vivado HLS Report for 'alu_hls_ex'
================================================================
* Date:           Sun Aug 10 14:59:01 2025

* Version:        2019.1 (Build 2552052 on Fri May 24 15:28:33 MDT
* Project:        ALU
* Solution:       ALU_Solution
* Product family: virtex7
* Target device:  xc7vx485t-ffg1157-1


================================================================
== Performance Estimates
================================================================
+ Timing (ns):
    * Summary:
    +--------+-------+----------+------------+
    |  Clock | Target| Estimated| Uncertainty|
    +--------+-------+----------+------------+
    |ap_clk  |  10.00|     3.981|        1.25|
    +--------+-------+----------+------------+

+ Latency (clock cycles):
    * Summary:
    +-----+-----+-----+-----+---------+
    |  Latency  |  Interval | Pipeline|
    | min | max | min | max |   Type  |
    +-----+-----+-----+-----+---------+
    |    1|    1|    1|    1|   none  |
    +-----+-----+-----+-----+---------+

    + Detail:
        * Instance:
        N/A

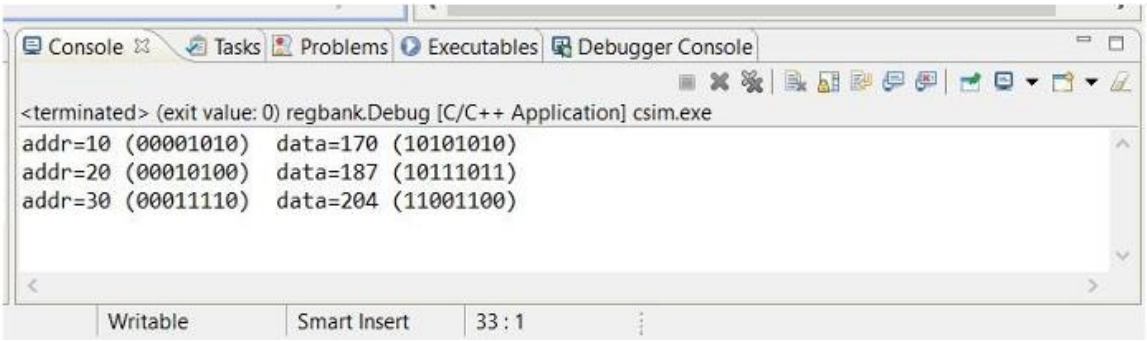
        * Loop:
        N/A


================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-------+--------+--------+-----+
|       Name      | BRAM_18K| DSP48E|   FF   |   LUT  | URAM|
+-----------------+---------+-------+--------+--------+-----+
|DSP              |        -|      -|       -|       -|    -|
|Expression       |        -|      -|       0|     153|    -|
|FIFO             |        -|      -|       -|       -|    -|
|Instance         |        -|      -|       -|       -|    -|
|Memory           |        -|      -|       -|       -|    -|
|Multiplexer      |        -|      -|       -|     157|    -|
|Register         |        -|      -|       2|       -|    -|
+-----------------+---------+-------+--------+--------+-----+
|Total            |        0|      0|       2|     310|    0|
+-----------------+---------+-------+--------+--------+-----+
|Available        |     2060|   2800|  607200|  303600|    0|
+-----------------+---------+-------+--------+--------+-----+
|Utilization (%)  |        0|      0|   ~0   |   ~0   |    0|
+-----------------+---------+-------+--------+--------+-----+
```

4. Experiment 3: Register Bank

Objective: Implement a 256x8-bit memory block with read, write, and enable signals.

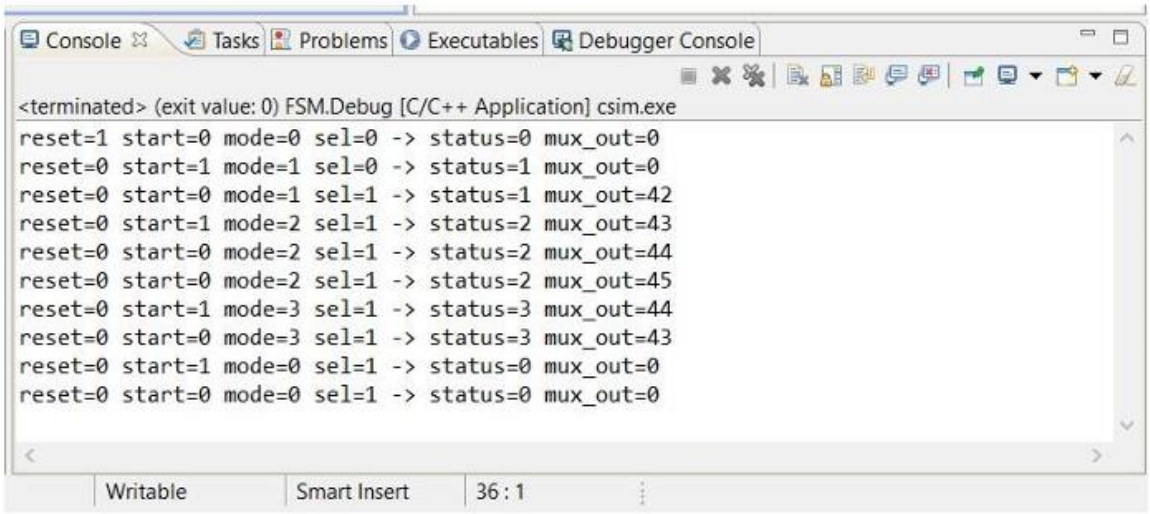
- Priority: Write takes precedence over read when enabled.
- Testbench: Writes values to addresses, then reads back correctly.
- Synthesis Results: Clock ≈ 2.27 ns, latency 1–2 cycles, minimal resources.



5. Experiment 4: Finite State Machine (FSM)

Objective: Design an FSM with states: IDLE, LOAD, COUNT_UP, COUNT_DOWN.

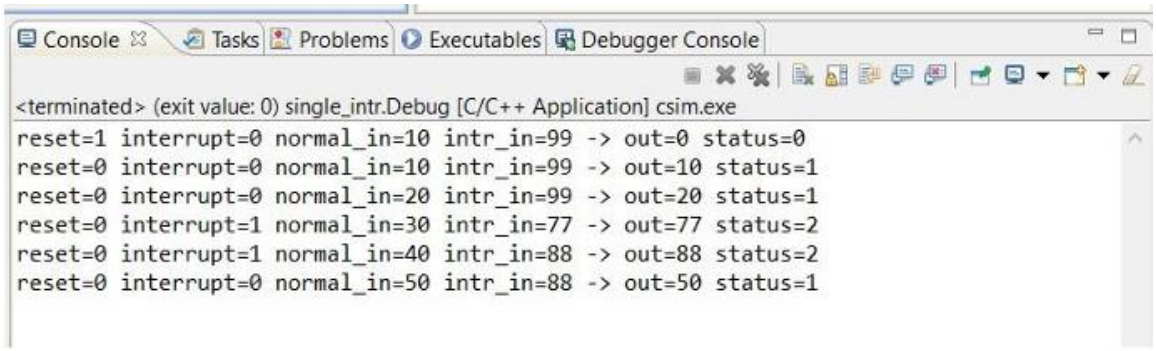
- Includes a 2:1 multiplexer for output selection.
- Testbench: Demonstrates transitions across states.
- Synthesis Results: Clock ≈ 5.12 ns, latency = 1 cycle, minimal resources.



6. Experiment 5: Single Interrupt

Objective: Implement a module reacting to a single interrupt signal.

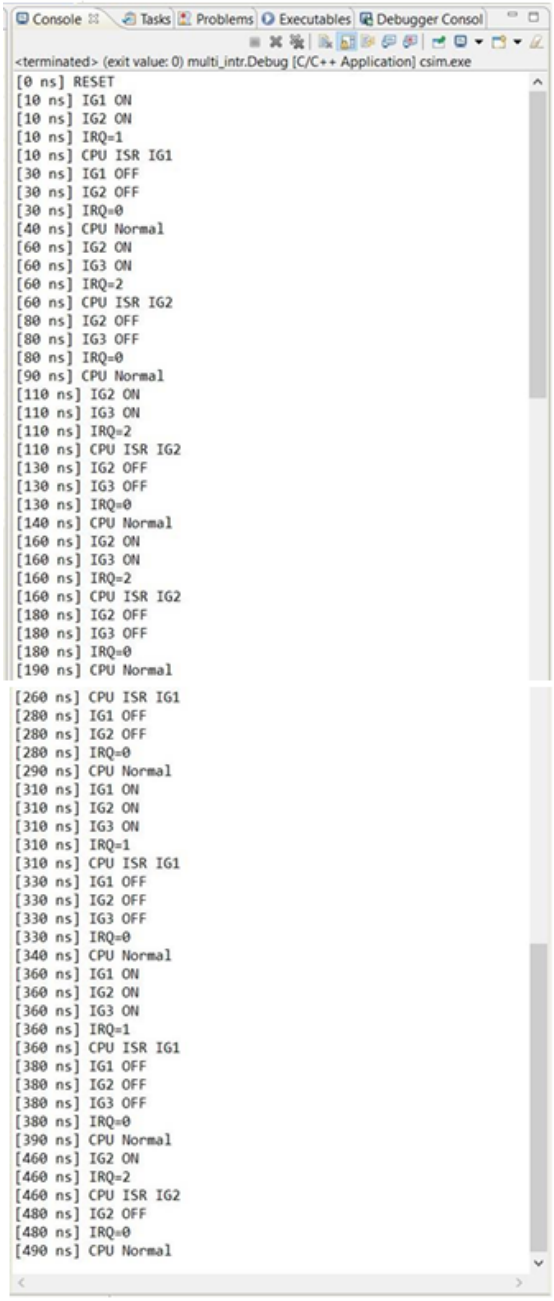
- Modes: Normal → output=in_normal, Interrupt → output=in_intr.
- States: 0=IDLE, 1=Normal, 2=ISR
- Testbench: Reset → Normal → Interrupt → Back to Normal.
- Synthesis Results: Clock ≈ 1.24 ns, latency=0 cycles, only 23 LUTs.



7. Experiment 6: Multi Interrupt

Objective: Implement a multi-interrupt controller with 3 sources (IG1, IG2, IG3) and fixed priority (IG3>IG2>IG1).

- Behavior: Each interrupt ON for 20ns, OFF for 30ns.
- CPU services ISR for 30ns, then returns to Normal.
- Outputs: irq, cpu_state, ig1, ig2, ig3
- Testbench: 500 ns simulation confirms priority and ISR timing.
- Synthesis Results: Clock ≈ 4.39 ns, latency=1–2 cycles, ~400 LUTs, 70 FFs.



8. Conclusion

All six experiments were successfully migrated from SystemC (software simulation) to Vivado HLS (hardware design). The designs synthesized on Zynq-7000 with minimal resource utilization and very low latencies. This demonstrates effective use of C++/HLS for hardware-software co-design.