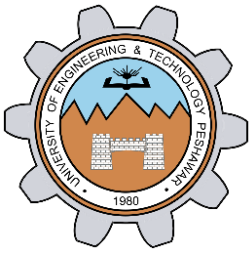
Circuit and System-I

LAB # 06



Spring 2022

Submitted by: Ali Asghar

Registration No.: **21PWCSE2059**

Class Section: **C**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Faiz Ullah

26 May, 2022

Department of Computer Systems Engineering

ASSESSMENT RUBRICS LAB # 6

Verification of KVL using Breadboard

LAB REPORT ASSESSMENT				
Criteria	**Excellent**	**Average**	**Nill**	**Marks Obtained**
1. Objectives of Lab	All objectives of lab are properly covered [Marks 1]	Objectives of lab are partially covered [Marks 0.5]	Objectives of lab are not shown [Marks 0]	
2. Kirchhoff's Voltage Law (Statement, Mathematical Expression, Circuit Diagram)	Correct KVL statement and mathematical expression is written. Circuit diagram shown is correct and properly labeled [Marks 2]	KVL statement or mathematical expression or circuit diagram is missing or circuit diagram is not properly labeled [Marks 1]		
3. PSPICE Simulator	Brief introduction of PSPICE simulator [Marks 1]	Brief introduction of PSPICE simulator Is not shown [Marks 0]		
4. Observations & Calculations	All experimental results are completely shown in form of table [Marks 4]	Experimental results are partially shown and some of the observations are missing [Marks 2]	No experimental results are shown [Marks 0]	
5. Analysis	Analysis and discussion about all experimental results are shown [Marks 2]	Analysis and discussion about experimental results are partially shown [Marks 1]	Analysis is not shown [Marks 0]	

Total Marks Obtained:_____

Instructor Signature: _____

TITLE:

Verification of **KVL** using **Breadboard**

OBJECTIVES :

- To know about KVL.
- Find voltage drop across different resistors using KVL.

KIRCHHOFF'S VOLTAGE LAW (KVL):

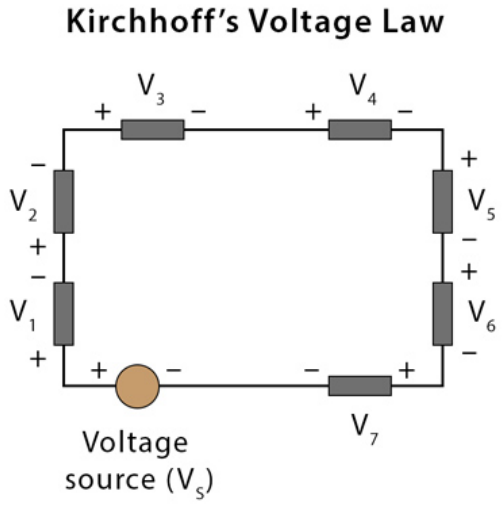
STATEMENT:

Kirchhoff's Voltage Law states that in any closed loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop which is also equal to zero. In other words, the algebraic sum of all voltages within the loop must be equal to zero.

MATHEMATICAL FORM :

$$\sum V = 0 \text{ (Across a loop)}$$

CIRCUIT DIAGRAM :



$$V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + V_7 - V_S = 0$$

PSPICE:

PSpice is a SPICE analog circuit and digital logic simulation software that runs on personal computers, hence the first letter "P" in its name. It was developed by MicroSim and is used in electronic design automation. MicroSim was bought by OrCAD which was subsequently purchased by Cadence Design Systems. The name is an acronym for Personal Simulation Program with Integrated Circuit Emphasis. Today it has evolved into an analog mixed signal simulator.

OR

"PSPICE is a circuit analysis tool that allows the user to simulate a circuit and extract key voltages and currents."

APPARATUS :

Apparatus used in this verification experiment is given as follow:

1. Breadboard
2. Voltage source
3. 2 x Resistors
4. Connecting wires.
5. Digital multi-meter

PROCEDURE:

1) Design the following circuit on breadboard

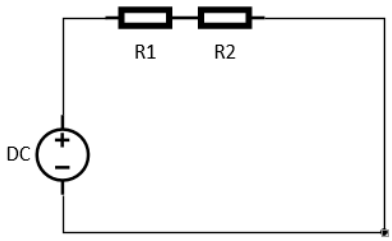


Figure 1 Circuit diagram

2) Using DMM find resistance of the resistors and note down in the table.
3) Find voltage of DC source and voltage drop on each resistor and note down in the table.
4) Add the voltage drops and compare with the source voltage by finding the percentage error.

OBSERVATION:

S.no	Vs (actual) (V)	R1 (Measured) (Ω)	R2 (Measured) (Ω)	V1 (Measured) (V)	V2 (Measured) (V)	V1+V2 (V)	Error	Percentage Error (%)
1.	5	3.42K	9.7K	1.35V	3.86V	5.21V	+0.21V	+4.2%
2.	10	3.42K	9.7K	2.6V	7.39V	9.99V	-0.01V	-0.07%
3.	15	3.42K	9.7K	3.96V	11.33V	15.3V	+0.3V	+0.2%
4.	20	3.42K	9.7K	5.21V	14.78V	19.9V	-0.1V	-0.05%
5.	30	3.42K	9.7K	7.82V	22.179V	30.2	+0.2V	+0.6%

ANALYSIS:

From the above experimental result we have seen that there is a little difference between source voltage which is measured with the help of DMM. This is because we can't prove every law 100% correctly practically. All the laws are verified theoretically or mathematically but not practically. But at the same time we see that this difference is very less and may be negligible which gives the proofs of KVL. Only in the 1st case the error is 4.2% which is greater as compared to the other cases.