

Lab 12

Synchronous counters

OBJECTIVES

After completing this experiment, you will be able to:

- Analyze the count sequence of a synchronous counter.
- To design and implement 3 bit synchronous up/down counter.

COMPONENTS REQUIRED

- Two 7476, JK flip flop ICs
- One 7411, 3 I/P AND gate
- One 7432, 2 I/P OR gate
- One 7486, 2 I/P XOR gate
- One 7404, hex inverter

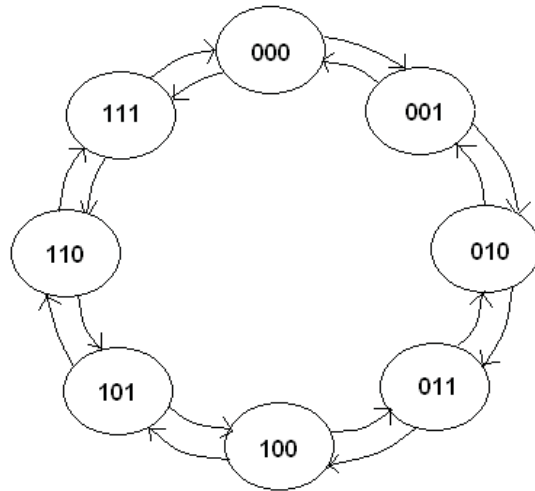
THEORY

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived.

Synchronous counters have all clock lines tied to a common clock, causing all flip-flops to change at the same time. For this reason, the time from the clock pulse until the next count transition is much faster than in a ripple counter. This greater speed reduces the problem of glitches (short, unwanted signals due to non-synchronous transitions) in the decoded outputs. However, glitches are not always eliminated, because stages with slightly different propagation delays can still have short intermediate states.

An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

STATE DIAGRAM



CHARACTERISTICS TABLE

Q	Q _{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

K MAP

	QB QC			
UD QA	1	0	0	0
	X	X	X	X
	X	X	X	X
	0	0	1	0

$JA = \overline{UD} \overline{QB} \overline{QC} + UD \overline{QB} QC$

	QB QC			
UD QA	X	X	X	X
	1	0	0	0
	0	0	1	0
	X	X	X	X

$KA = \overline{UD} \overline{QB} \overline{QC} + UD \overline{QB} QC$

	QB QC			
UD QA	1	X	X	1
	1	X	X	1
	1	X	X	1
	1	X	X	1

$JC = 1$

	QB QC			
UD QA	1	0	X	X
	1	0	X	X
	0	1	X	X
	0	1	X	X

$JB = UD \oplus QC$

	QB QC			
UD QA	X	X	0	1
	X	X	0	1
	X	X	1	0
	X	X	1	0

$KB = (UD \oplus QC)$

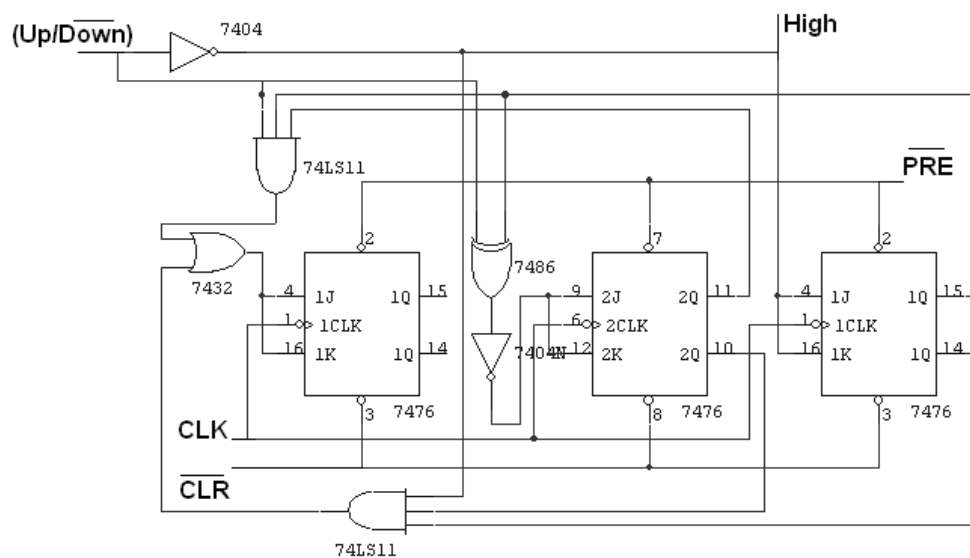
	QB QC			
UD QA	X	1	1	X
	X	1	1	X
	X	1	1	X
	X	1	1	X

$KC = 1$

TRUTH TABLE

Input Up/Down	Present State			Next State			A		B		C	
	Q _A	Q _B	Q _C	Q _{A+1}	Q _{B+1}	Q _{C+1}	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

LOGIC DIAGRAM



PROCEDURE

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

REVIEW QUESTIONS

- 1) What is the difference between asynchronous and synchronous counters? Which counter will you prefer to use in your circuits and why? Also specify the main drawbacks of asynchronous counters.
- 2) Design a synchronous counter which count the sequence 0, -1, -2, -3 using D-flip flops. List all steps.
- 3) Draw the timing diagram for each flip flop output in part 2.