*Name: _____

*Registration: _____

Department of Computer Systems Engineering
University of Engineering & Technology Peshawar

Digital Logic Design
CSE 202

Finalterm Examination Fall 2021

7 March 2022, Duration: 180 Minutes

Exam Rules

Please read carefully before proceeding.

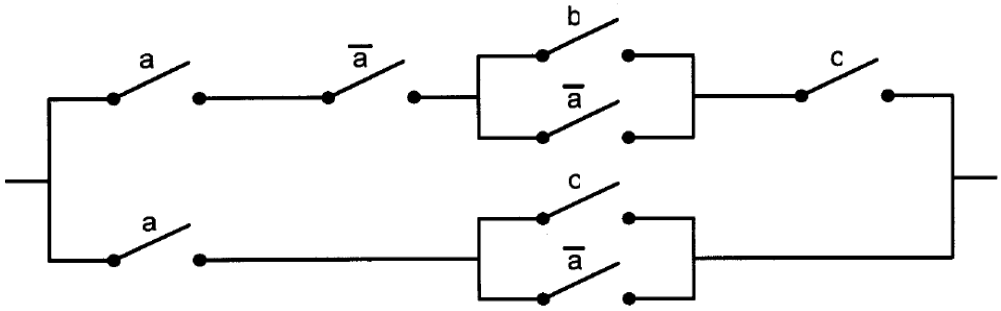
- This exam is OPEN books/notes but CLOSED Internet/laptops/phones.
- Sharing of books, notes, and other materials during this exam is not permitted.
- No calculators/phones of any kind are allowed.
- Attempt all problems on the problem sheet. Use the answer sheet for scratch space and write a neat copy of your final answer in the provided space on the problem sheet. **Very Important!!!**
- Be precise and concise in your answers (no extra explanatory text).
- Some problems are harder than others. User your time wisely.
- **Problems will not be interpreted during the exam.**
- This exam booklet contains 10 pages, including this one. Count them to be sure you have them all.

Problem 1	_____	(23 pts.)
Problem 2	_____	(15 pts.)
Problem 3	_____	(30 pts.)
Problem 4	_____	(20 pts.)
Problem 5	_____	(12 pts.)
Exam Total	_____	**(100 pts.)**

Good luck!

Problem 1: **(23 pts.)** Answer the following questions.

(a) **(2 pts.)** Write the minimized Boolean expression for the following switch network.



Minimized Boolean expression = _____

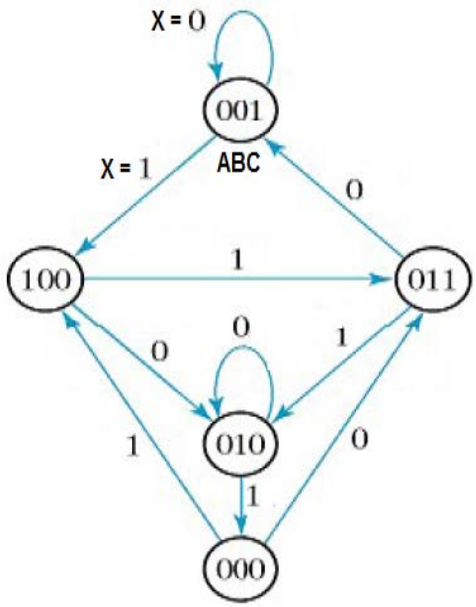
(b) **(2 pts.)** For the counter shown beside, if the present state (ABC) is 101, and the input X = 0; what will be the next state if the flip-flops input functions are as follows:

$J_A = \overline{B}.X, K_A = 1$

$J_B = A + \overline{C}.\overline{X}, K_B = X.\overline{C} + C.\overline{X}$

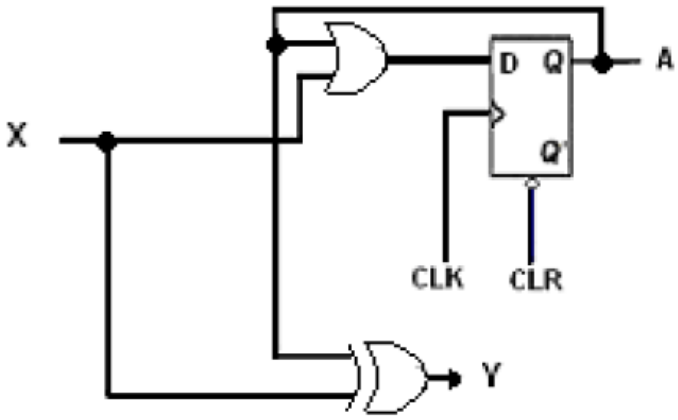
$J_C = A.X + \overline{A}.\overline{B}.\overline{X}, K_C = X$

Next state = _____



(c) **(3 pts.)** Given that the flip-flop shown beside is initially cleared. A serial input data X = 1010 is applied to the circuit from right to left (i.e. 0 is the first bit to be received). What is the output Y?

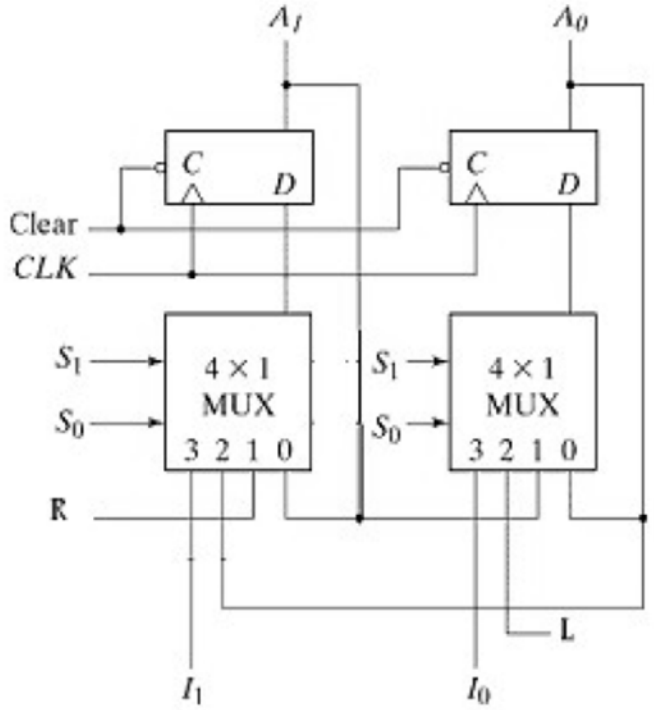
Y = _____



(d) (2 pts.) When designing the circuit with the state table given below using JK flip-flops, then the Boolean expression for J_A =_____and K_A = _____.

Present State		Input	Next State		FFs Inputs	
A	B	X	A^+	B^+	J_A	K_A
0	0	0	0	0		
0	0	1	0	1		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	1	1		
1	1	0	1	1		
1	1	1	0	0		

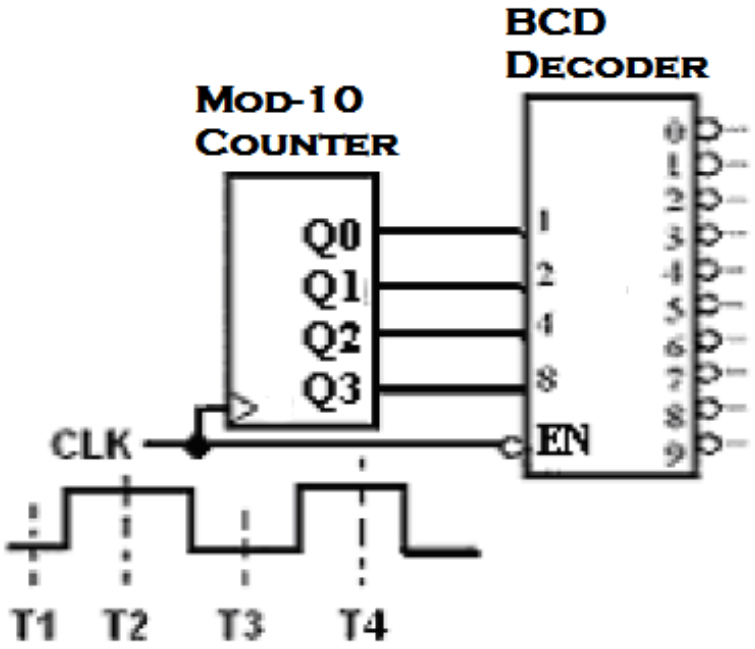
(e) (2 pts.) For the circuit shown below, if S_1 = 1 and S_0 = 0, with S_0 being least significant, when the CLK is received, then $A_{0(t+1)}$ and $A_{1(t+1)}$ will be:



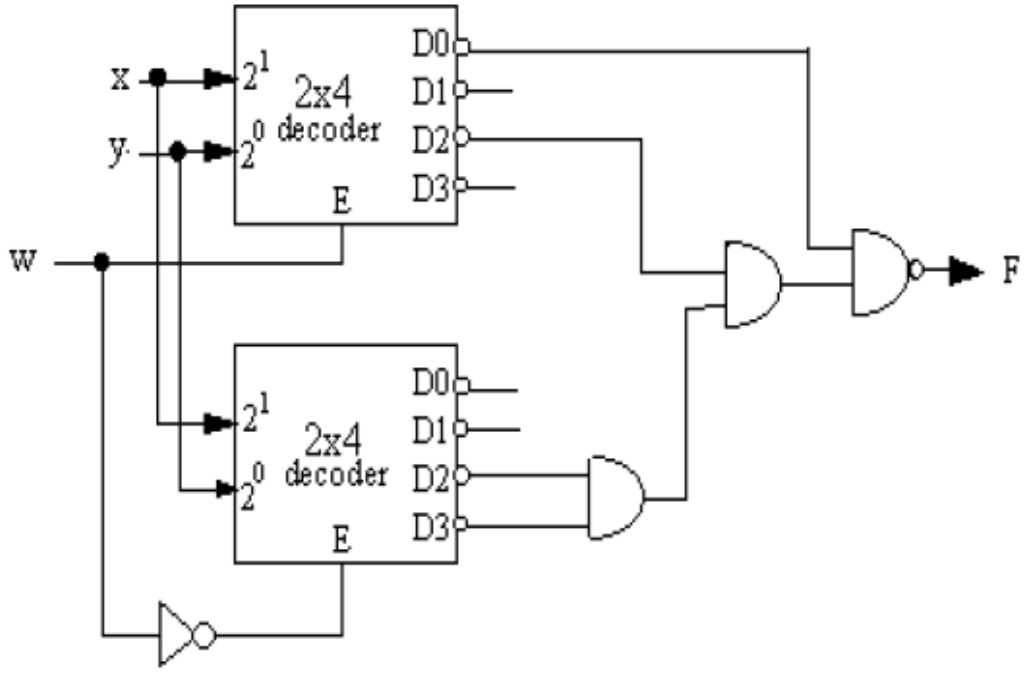
$A_{0(t+1)}$ =_____

$A_{1(t+1)}$ =_____

(f) **(2 pts.)** For the circuit shown below, if $Q_3Q_2Q_1Q_0$ = 1001 at time T_1, then at time T_3, $Q_3Q_2Q_1Q_0$ = _____ and output number _____ of the Decoder will be activated.



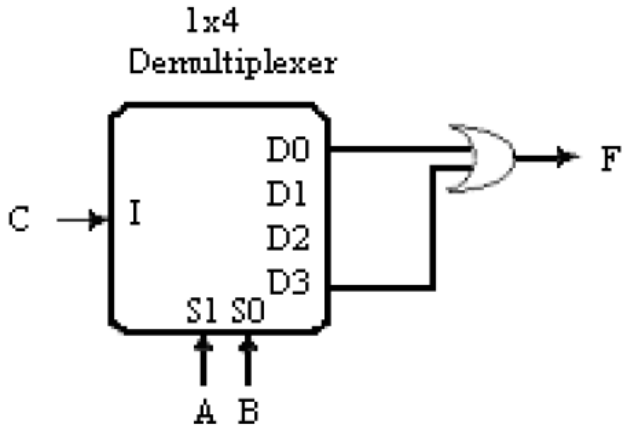
(g) **(2 pts.)** Determine the output function F(W, X, Y) as a sum of minterms in the following logic circuit.



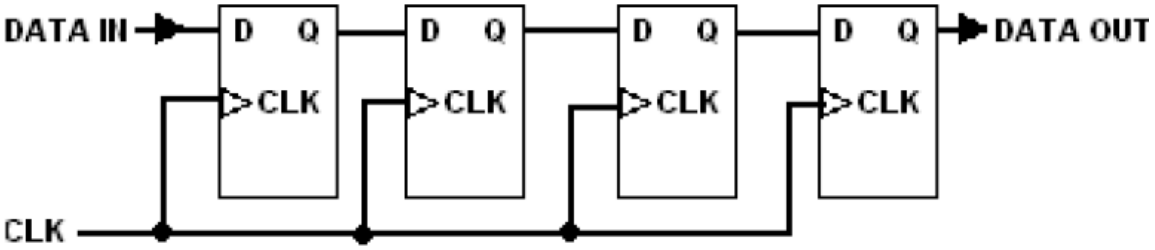
F(W, X, Y) = $\sum_m$ (_____)

(h) **(2 pts.)** The Boolean expression for the function F(A, B, C) in the circuit shown beside is:

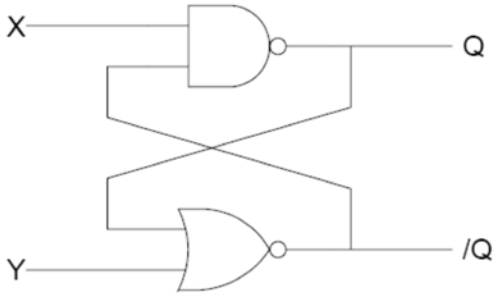
F(A, B, C) = _____



(i) **(2 pts.)** The number of data bits that can be stored in the register shown below is _____ and the number of clock cycles needed to store the data is _____.



(j) **(4 pts.)** A committee of logic designers could not agree on whether to use NAND gates or NOR gates to build a set-reset latch. The compromise design is shown below.



Fill in the function table for this sequential circuit.

X	Y	Q	/Q
0	0		
0	1		
1	0		
1	1		

Explain what is wrong with this "latch"? _____

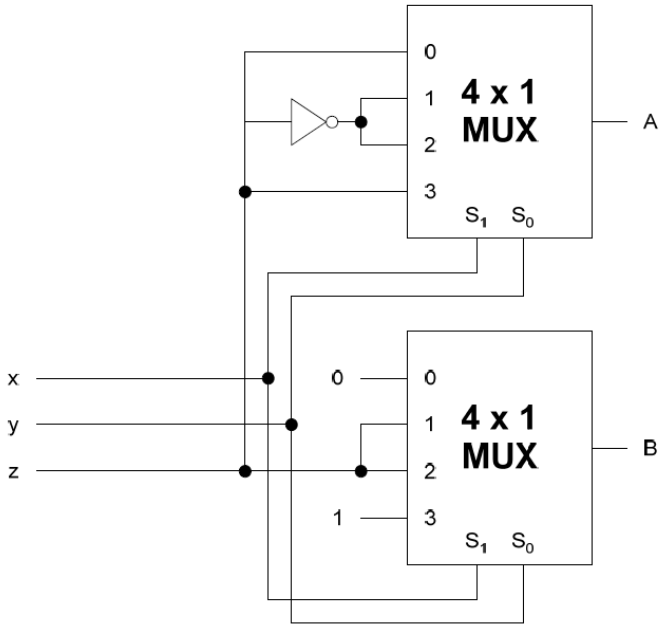
_____

_____

_____.

Problem 2: **(15 pts,)** Answer the following questions.

(a) **(10 pts.)** Determine the output functions A(X, Y, Z) and B(X, Y, Z) as sums of minterms. You may use any process to determine A and B, but show your work.



A(X, Y, Z) = $\sum m$ (_____)

B(X, Y, Z) = $\sum m$ (_____)

(b) **(5 pts.)** The circuit shown in **(a)** has the functionality of a commonly used arithmetic component. What does the circuit do and what are other names for A and B?

Problem 3: **(30 pts.)** You are a Hardware Design Engineer working for DCSE. They want you to design a sequential circuit that will automate their newest peon Speedo's movement on the UET campus. The Chairman wirelessly transmits the travel plans to Speedo, and then Speedo moves according to that information.

To design your circuit, you first select the following locations around the UET campus and assign each location with a state in 3-bit binary representation: Chairman's Office **[000]**, Lab-1 **[001]**, Lab-2 **[010]**, Lab-3 **[011]**, Coordinator's Office **[100]**, Dean's Office **[101]**, Registrar's Office **[110]**, and the VC's Office **[111]**.

To simplify your design, you inform the Chairman to send Speedo a binary sequence for travel plans (e.g. '1-0-0-0-1' to cause Speedo to move five times). In other words, Speedo receives either '0' or '1' for each move and travels to the next destination as specified below. Speedo starts off at Chairman's Office for each run, and your circuit should output Speedo's current location.

Current Location	**Moves**	
Chairman's Office **[000]**:	If 0, stay at Chairman's Office.	If 1, go to Lab-1.
Lab-1 **[001]**:	If 0, go to Lab-2.	If 1, go to Coordinator's Office.
Lab-2 **[010]**:	If 0, go to Lab-3.	If 1, go to Coordinator's Office.
Lab-3 **[011]**:	If 0, stay at Lab-3.	If 1, go to Chairman's Office.
Coordinator's Office **[100]**:	If 0, go to VC's Office.	If 1, go to Dean's Office.
Dean's Office **[101]**:	If 0, go to Lab-3.	If 1, go to Registrar's Office.
Registrar's Office **[110]**:	If 0, go to VC's Office.	If 1, stay at Registrar's Office.
VC's Office **[111]**:	If 0, go to Lab-1.	If 1, go to Dean's Office.

(a) **(10 pts.)** Draw the state diagram for this circuit.

(b) **(5 pts.)** If Speedo is forever given a sequence of 1s (i.e. 11111…), where will he eventually end up?

(c) **(5 pts.)** If Speedo is forever given a sequence of 01s (i.e. 010101…), which location(s) will he never visit?

(d) **(10 pts.)** Design a circuit for Speedo using T flip-flops and the state diagram in part **(a)**.

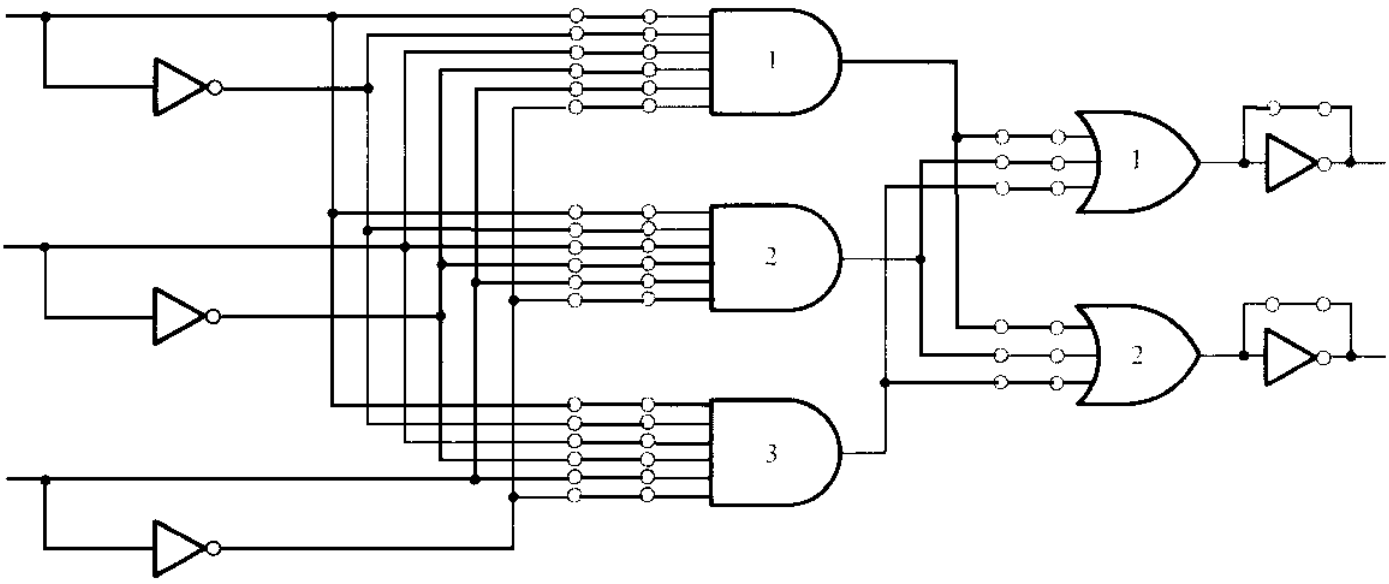
Problem 4: **(20 pts.)** A combinational circuit is defined by the functions

$$A(X, Y, Z) = \sum_m (3, 5, 7)$$
$$B(X, Y, Z) = \sum_m (0, 1, 2, 3, 4)$$

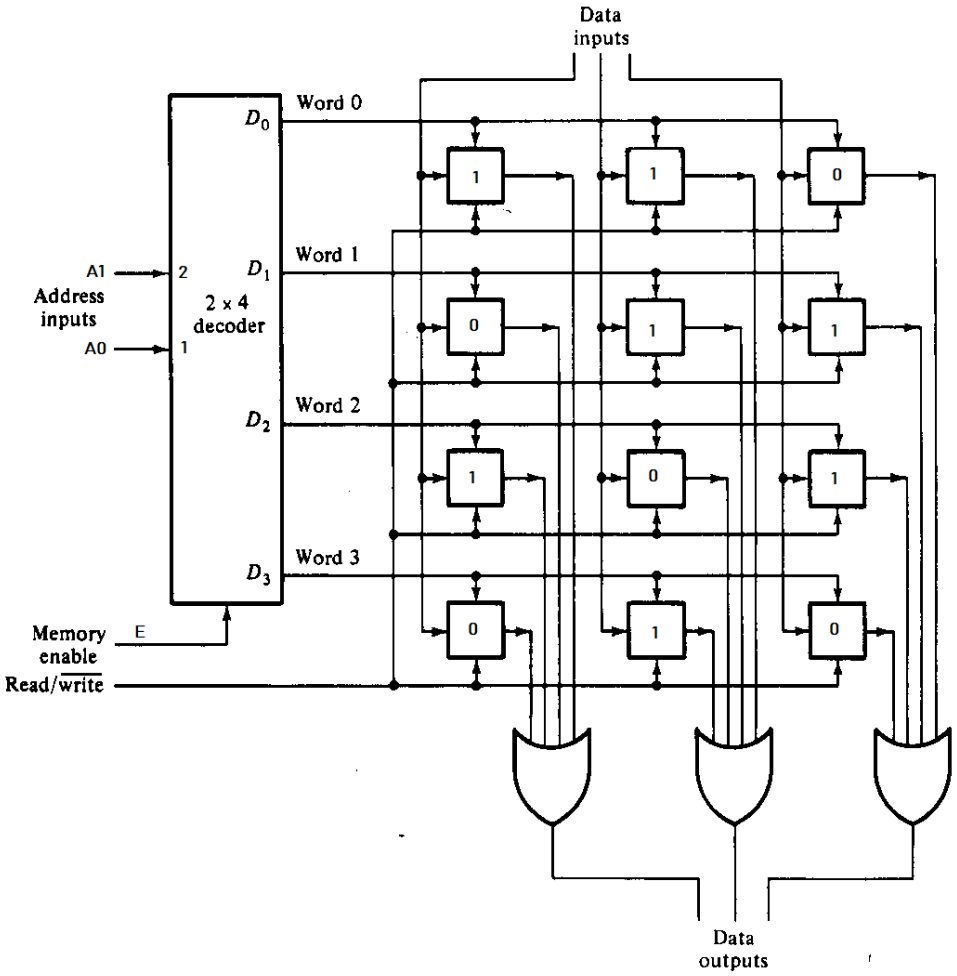
Implement the circuit with the below given PLA.

(a) **(10 pts.)** Draw the PLA program table.

(b) **(10 pts.)** Program the PLA to implement the circuit. Clearly label all inputs and outputs.



Problem 5: **(12 pts.)** Answer the following questions related to the below given 4x3 RAM with content as shown.



(a) **(2 pts.)** What is the output of the RAM when **E=0**, **R/$\overline{W}$=1**, and **A_1A_0=10**.

Output = _____.

(b) **(2 pts.)** What is the output of the RAM when **E=1**, **R/$\overline{W}$=1**, and **A_1A_0=01**.

Output = _____.

(c) **(2 pts.)** What is the output of the RAM when **E=1**, **R/$\overline{W}$=1**, and **A_1A_0=11**.

Output = _____.

(d) **(3 pts.)** What is the content of the RAM when **E=0**, **R/$\overline{W}$=0**, **A_1A_0=00,** and **input data=101**.

Word 0 = _____ Word 1 = _____ Word 2 = _____ Word 3 = _____.

(e) **(3 pts.)** What is the content of the RAM when **E=1**, **R/$\overline{W}$=0**, **A_1A_0=10,** and **input data=010**.

Word 0 = _____ Word 1 = _____ Word 2 = _____ Word 3 = _____.