LAB # 6

CSE-202L Digital Logic Design Lab

Fall 2022

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Lab 6

DECODERE AND NCODER

1 OBJECTIVES

After completing this experiment you will be able to:

- Design and construct Decoder and Encoder
- Verify their truth tables using logic gates

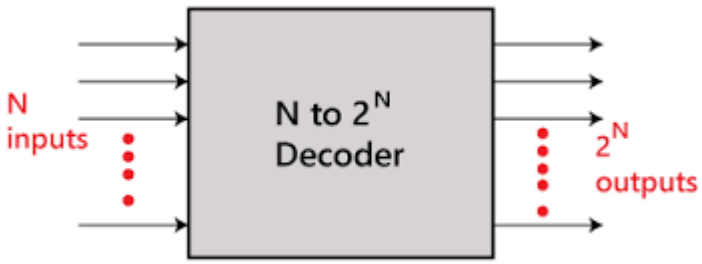
2 COMPONENTS REQUIRED

- Two 7410, 3 I/P NAND gate
- Three 7432, 2 I/P OR gate
- 7404 hex inverter

3 THEORY

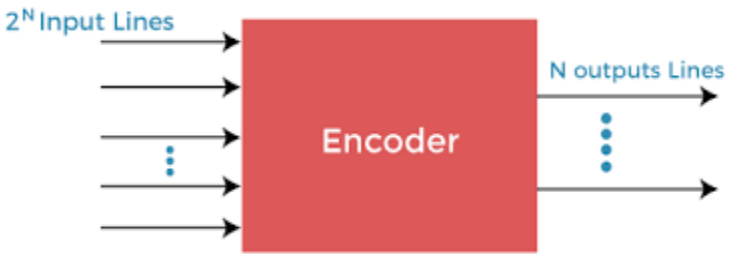
DECODER:

A Decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of Decoder circuit the encoded information is present as n input producing 2^npossible outputs. 2^noutput values are from 0 through out 2^n– 1.



ENCODER:

An Encoder is a digital circuit that perform inverse operation of a Decoder. An Encoder has 2^ninput lines and n output lines. In Encoder the output lines generates the binary code corresponding to the input value. In octal to binary Encoder it has eight inputs, one for each octal digit and three outputs that generate the corresponding binary code. In Encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.



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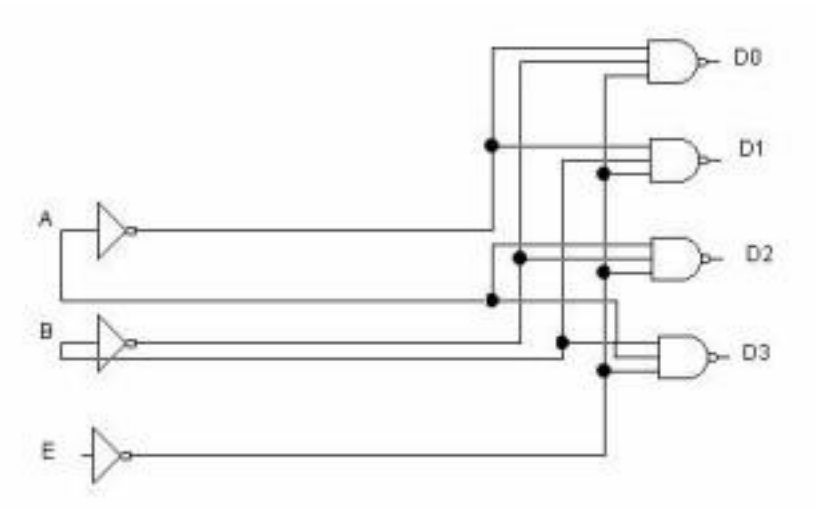
4 LOGIC DIAGRAM FOR DECODER

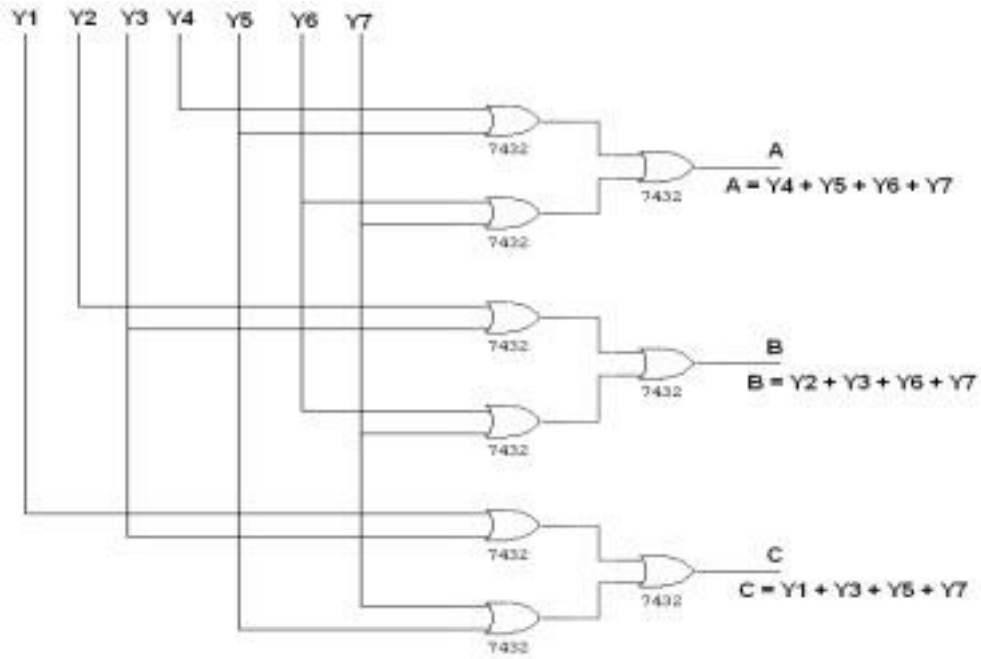


5 TRUTH TABLE

INPUTS				OUTPUTS	
Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

2

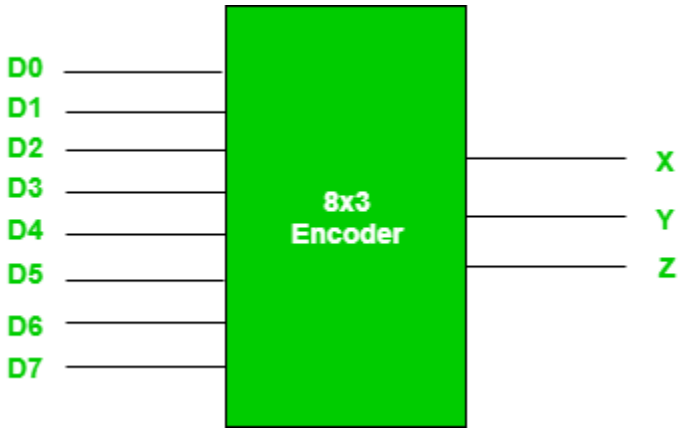
6 LOGIC DIAGRAM FOR ENCODER



TRUTH TABLE

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1



PROCEDURE

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

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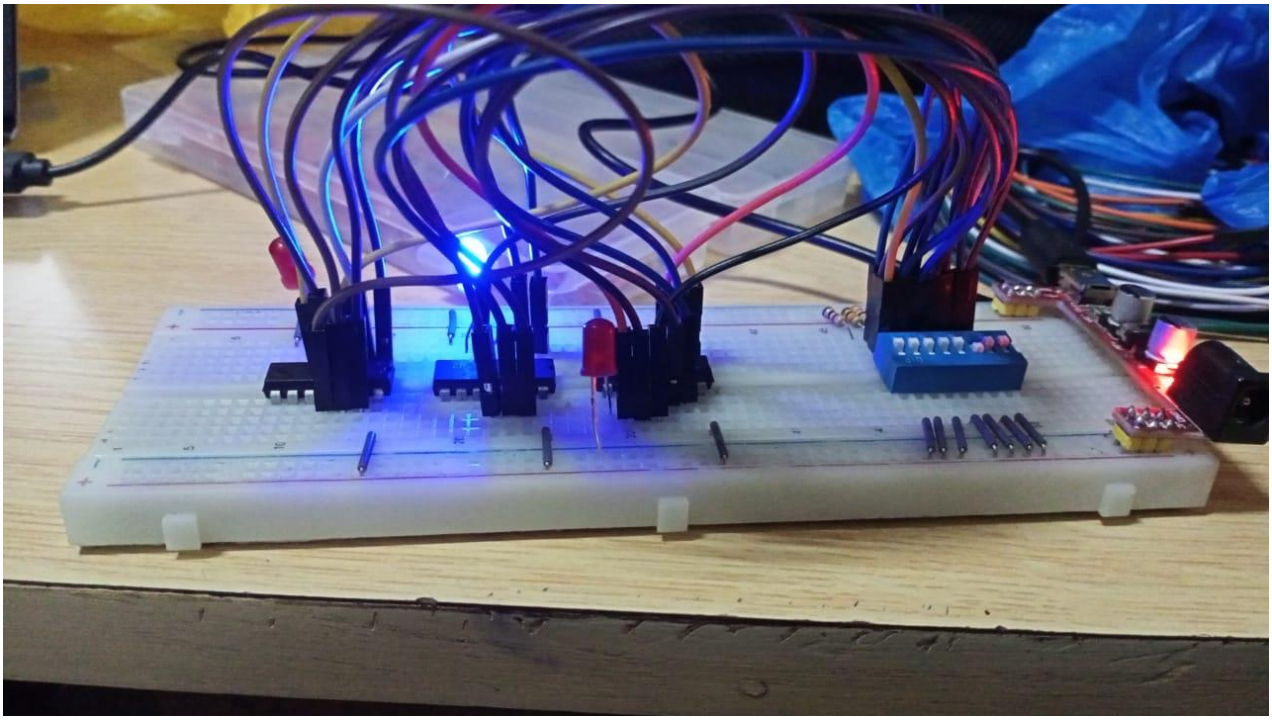
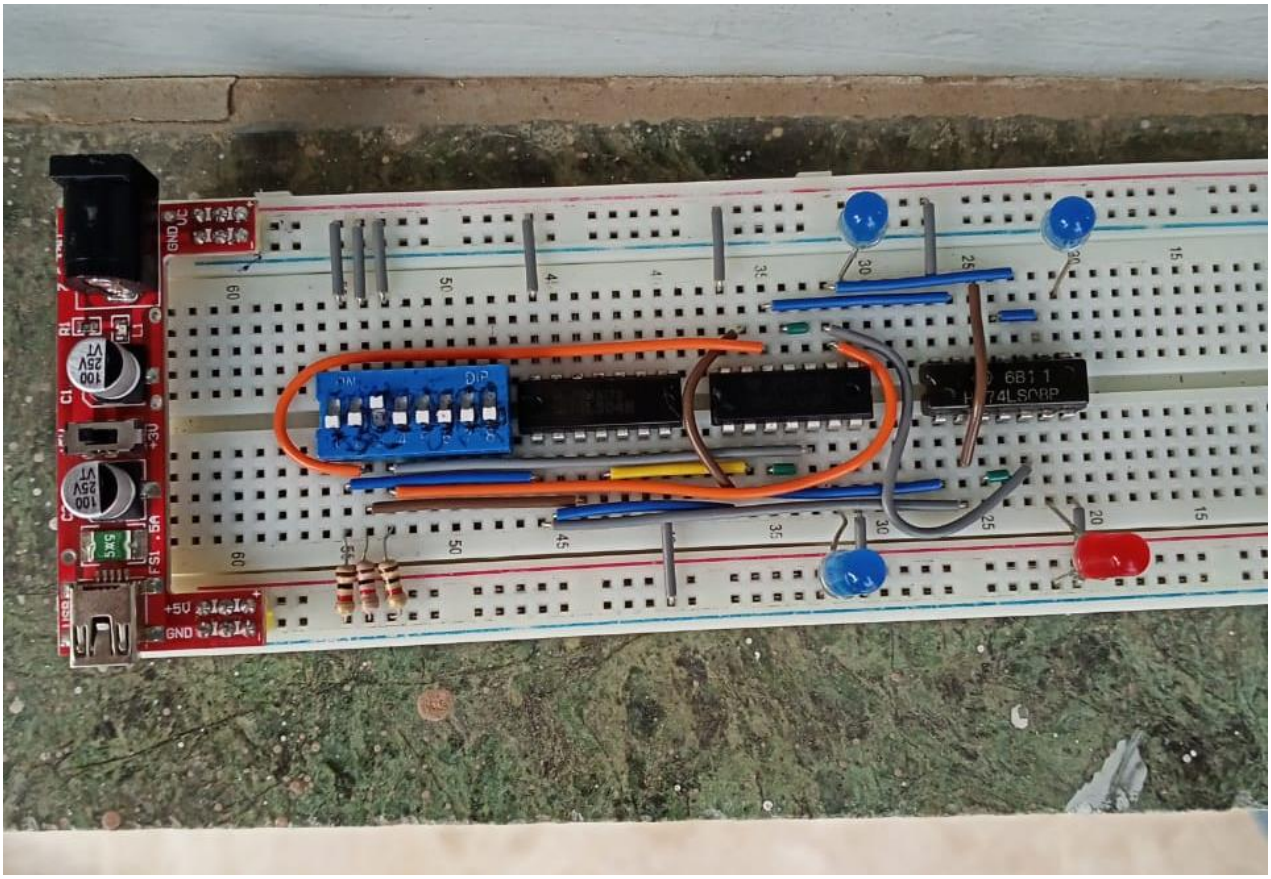


8 x 3 Encoder



3 x 8 Decoder

REVIEW QUESTIONS:

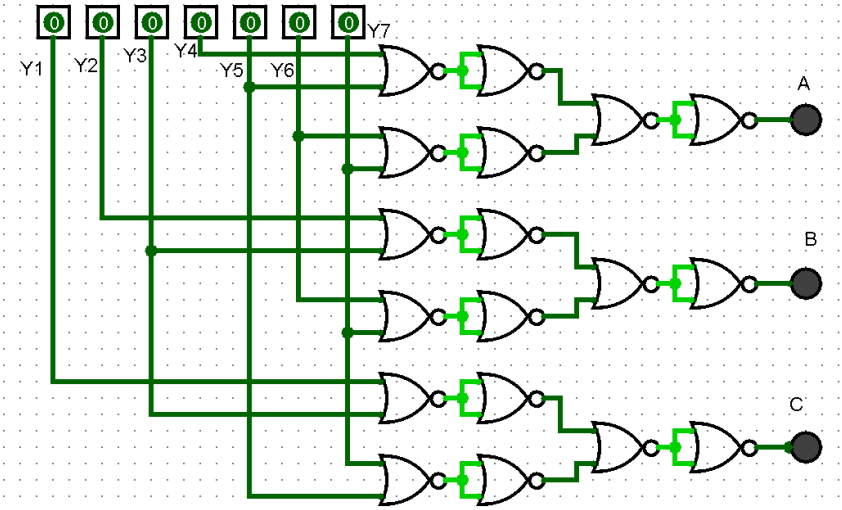
QUESTION 1:

Design an Encoder using NOR gates only.

ANSWER:

We can make an Encoder using only NOR gates. By using the gate combination of making a logical or OR using NOR, we can practically implement an encoder circuit using NOR gates only.

The circuit diagram is as under;

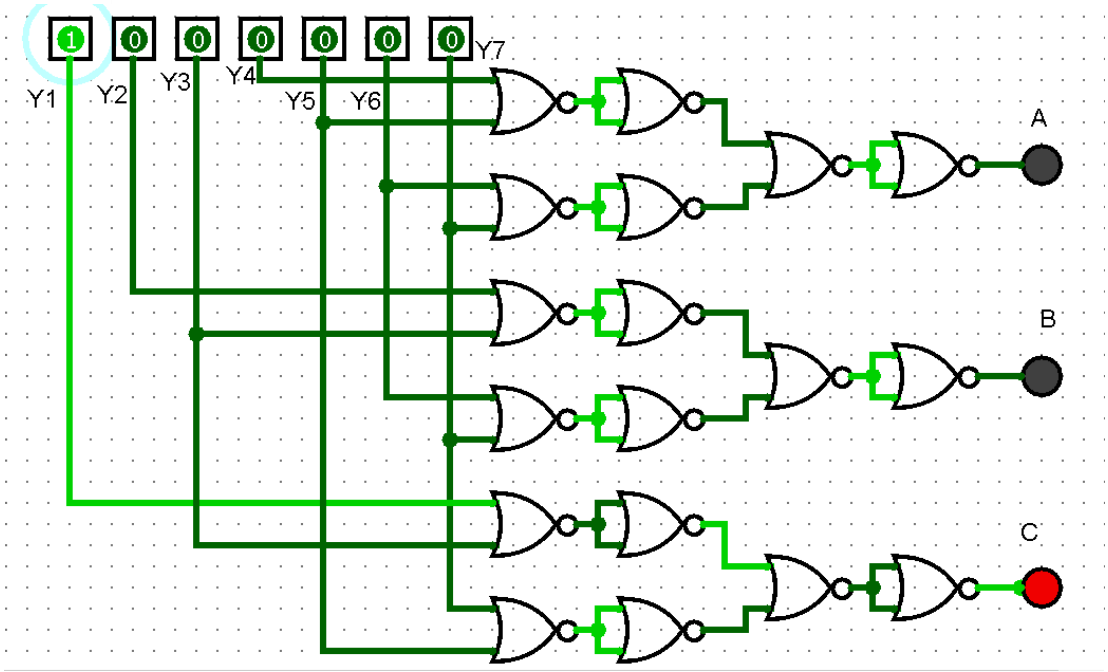


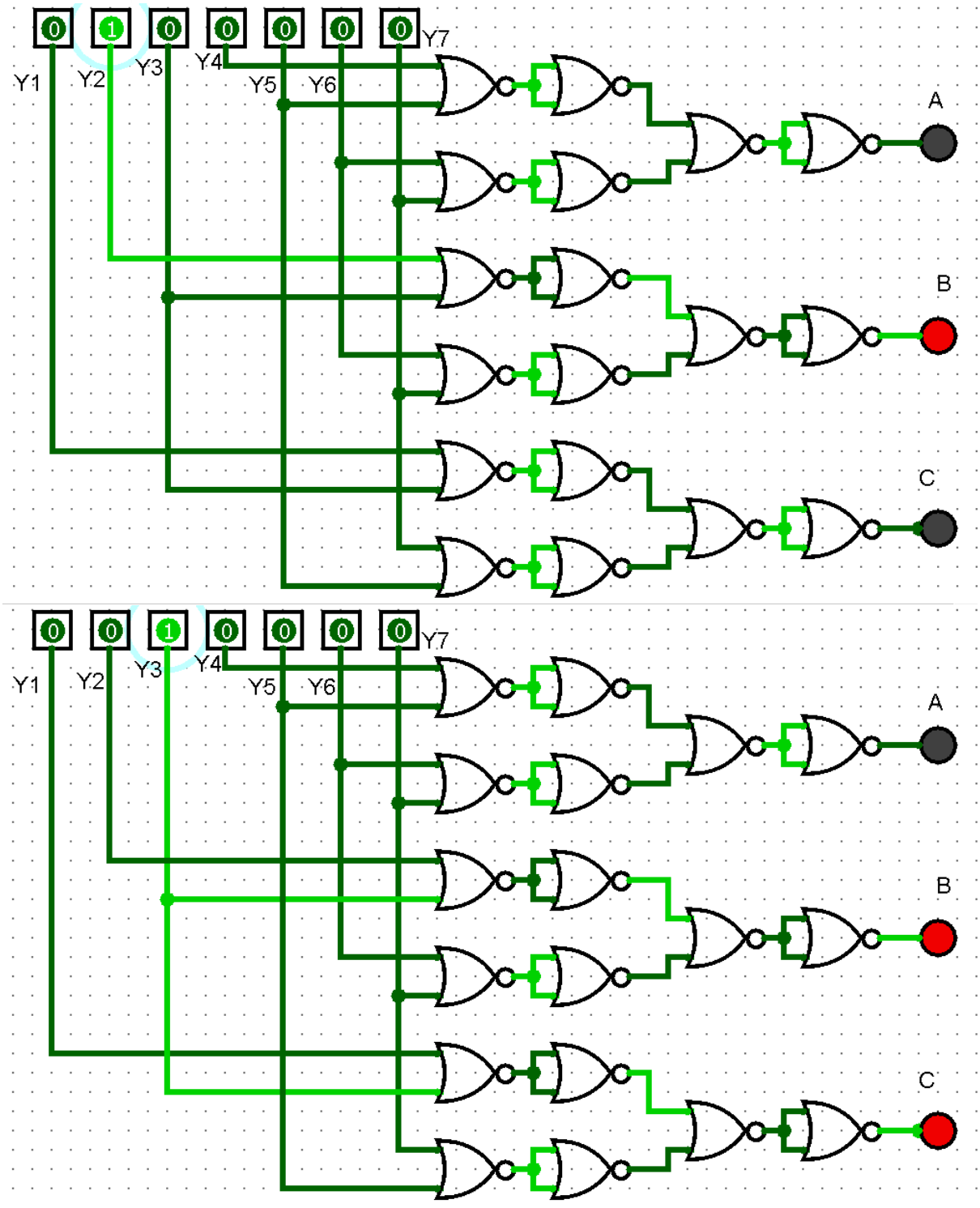
Now for different inputs, we verify the truth table.

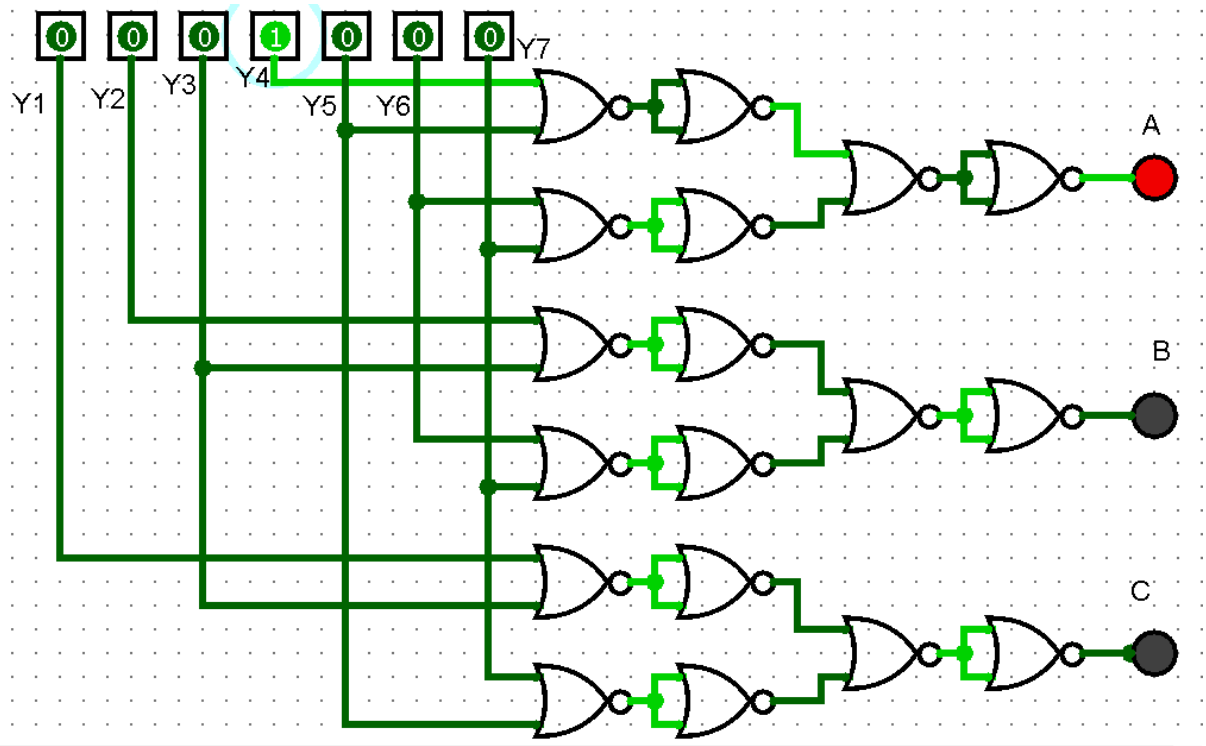
TRUTH TABLE:

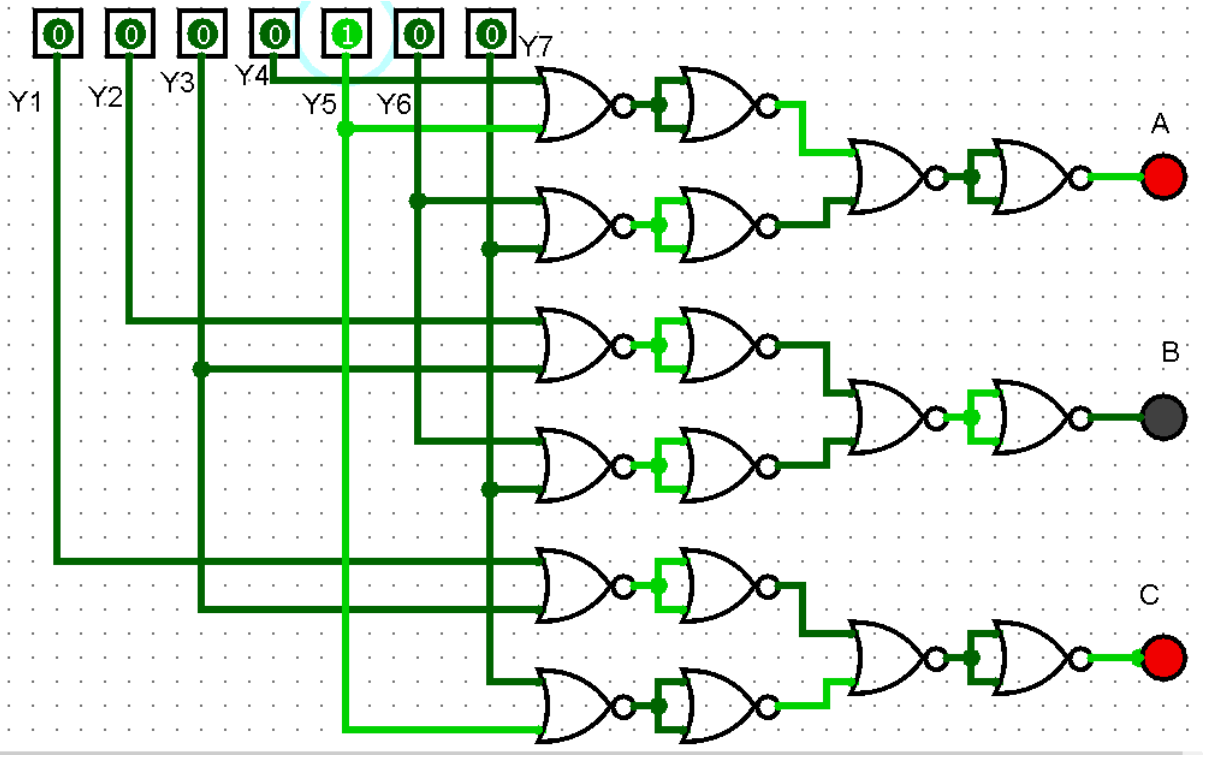
INPUT							OUTPUT		
Y1	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**A**	**B**	**C**
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

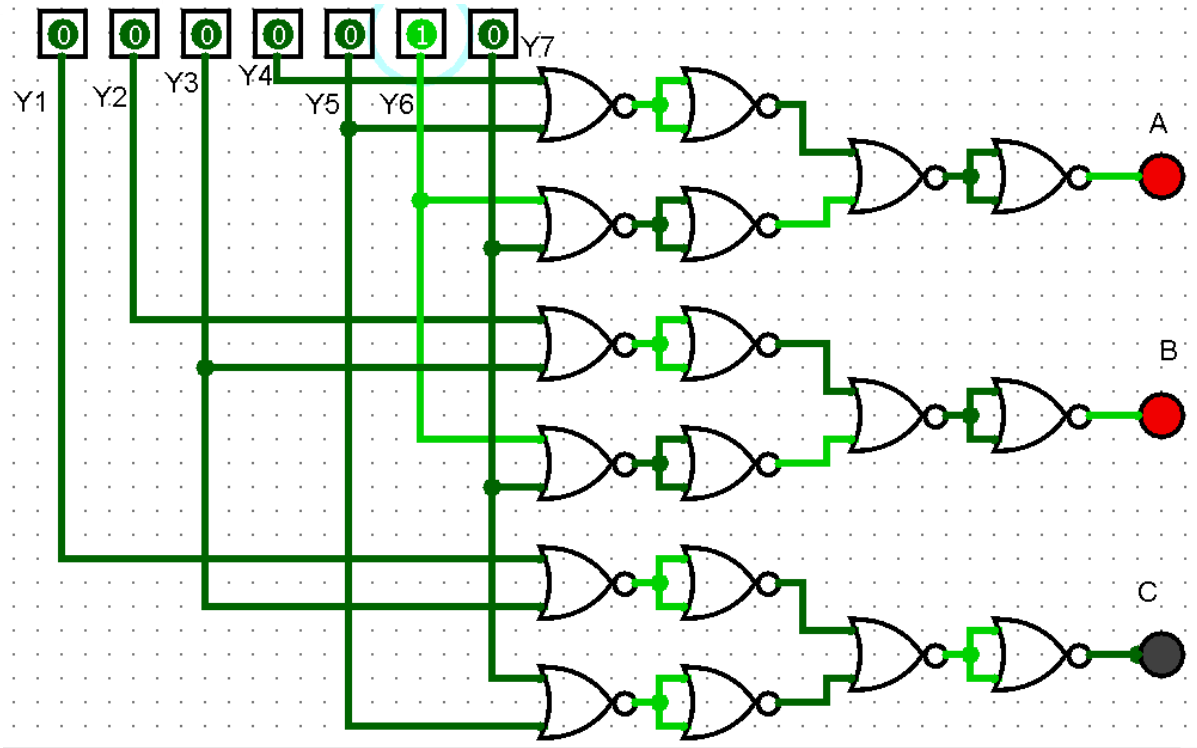
OBSERVATIONS:

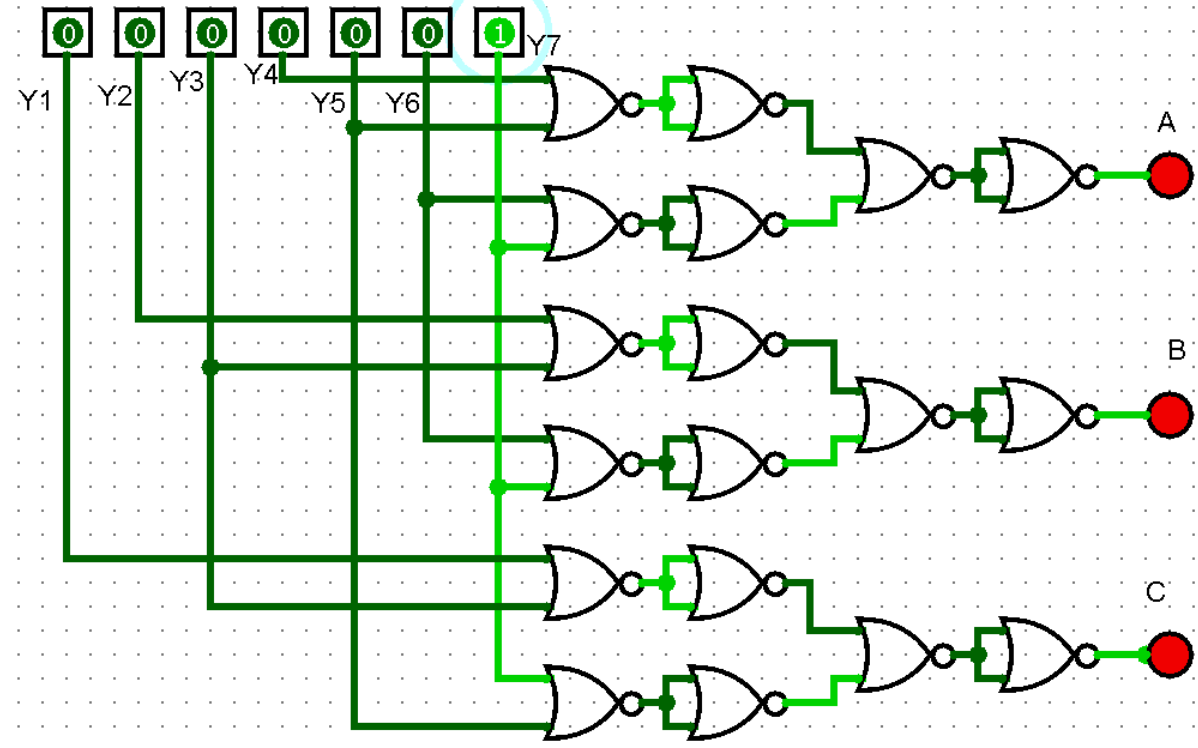

1
0
0
0
0
0
0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A
B
C


0
1
0
0
0
0
0
Y7
Y1
Y2
Y3
Y4
Y5
Y6
A
B
C
0
0
1
0
0
0
0
Y7
Y1
Y2
Y3
Y4
Y5
Y6
A
B
C


0
0
0
1
0
0
0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A
B
C


0
0
0
0
1
0
0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A
B
C





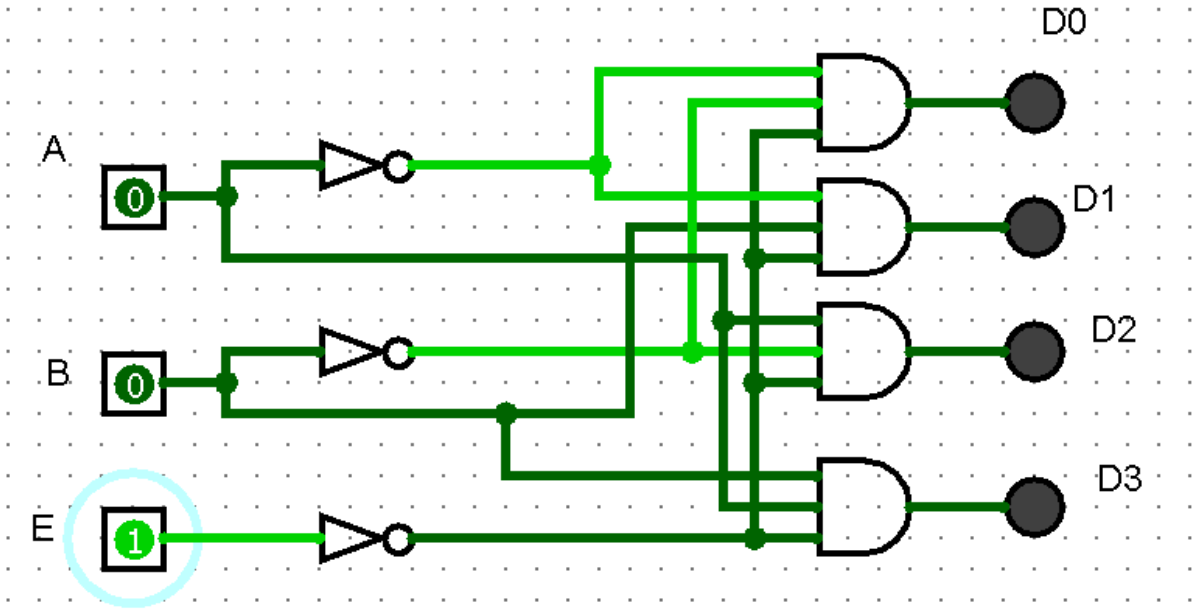
QUESTION 2:

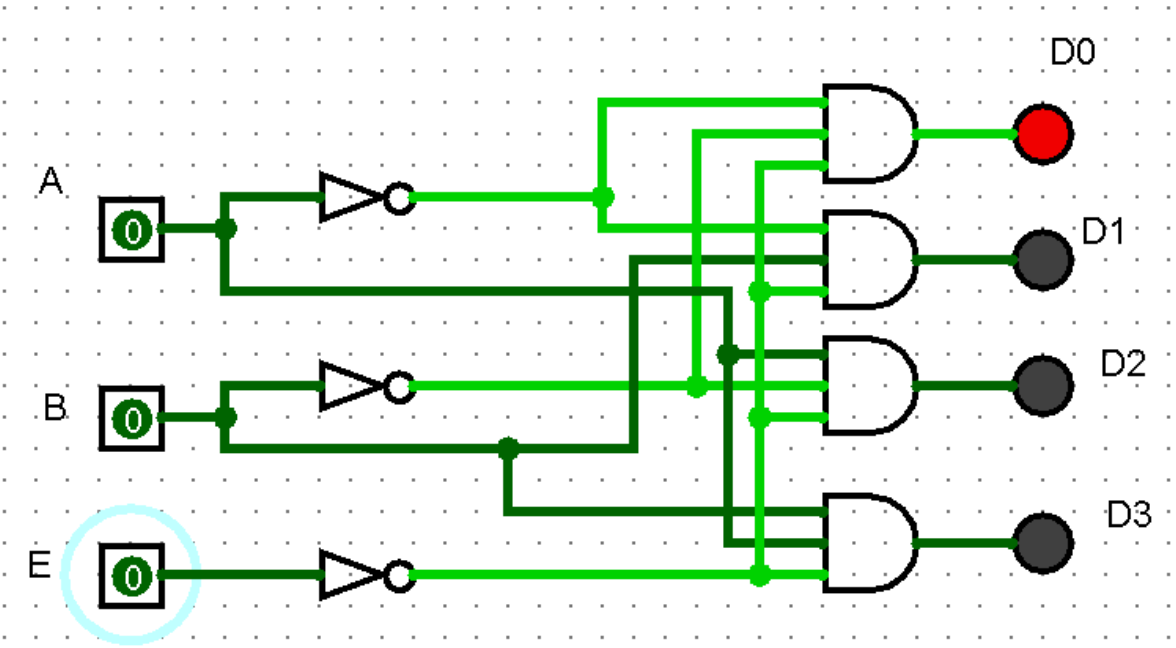
What will be the output of the Decoder circuit if NAND gates are replaced by AND gates?

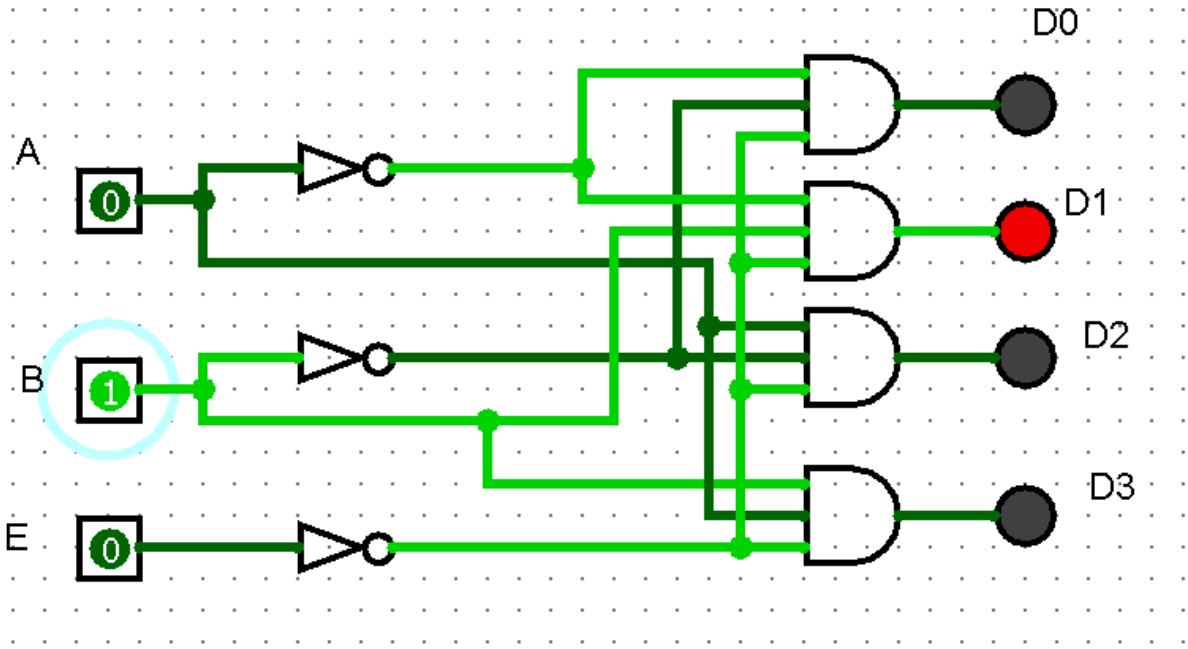
ANSWER:

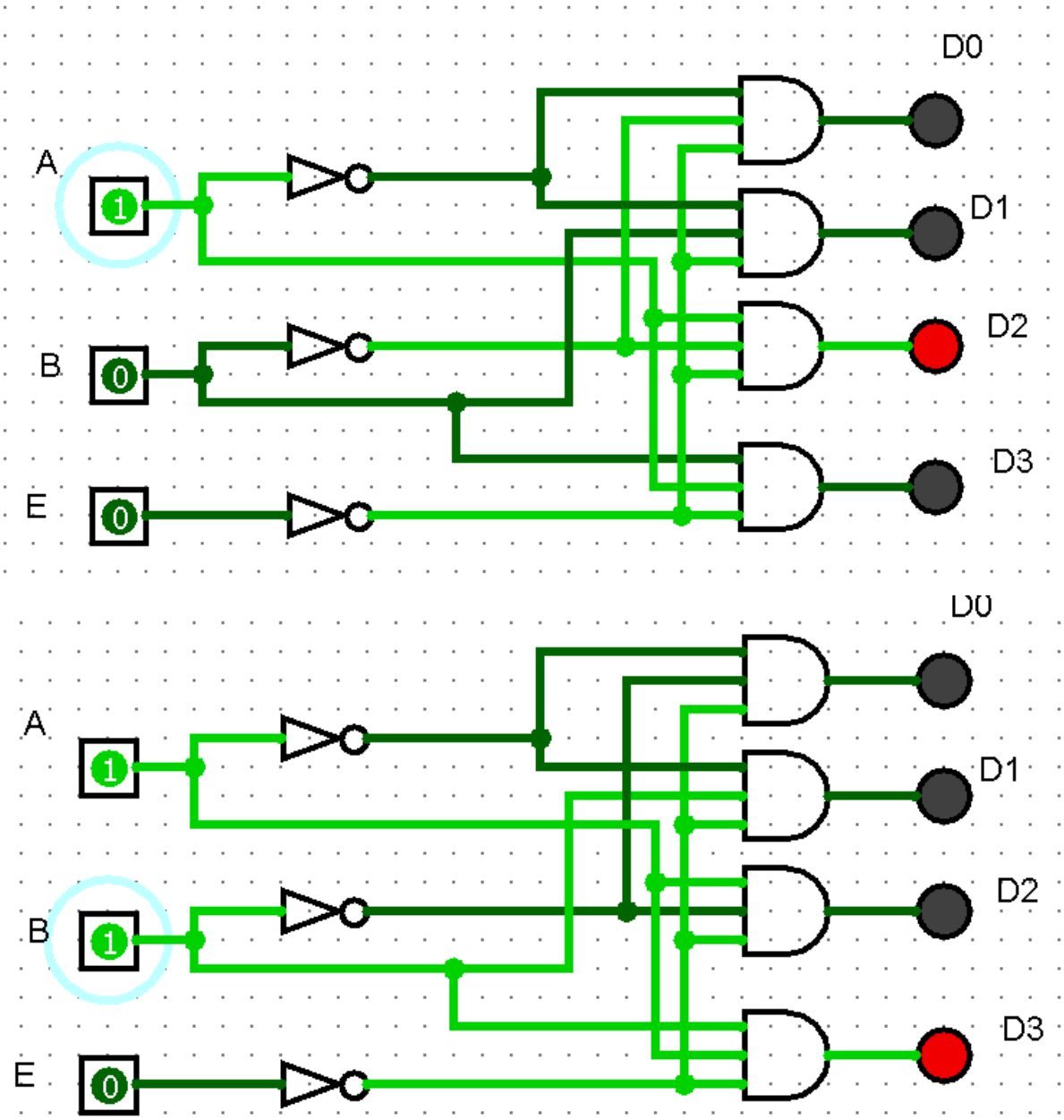
If we replace the NAND gates in the decoder with the AND gates than we will high value for every output in contrast to the fact that we got low values for output when we used NAND gates.

E	A	B	D_0	D_1	D_2	D_3
1	x	x	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1




D0
A
0
D1
B
0
D2
E
0
D3


D0
A
0
D1
B
1
D2
E
0
D3



QUESTION 3:

What is the purpose of enable input in Decoder?

ANSWER:

A standard decoder typically has an additional input called Enable.

Output is only generated when the Enable input has value 1 or we can set it to 0; otherwise, all outputs are vice versa. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs.

Many components have an Enable input which works in this way. Sometimes the Enable input is ``**active high**'', sometimes ``**active low**''.

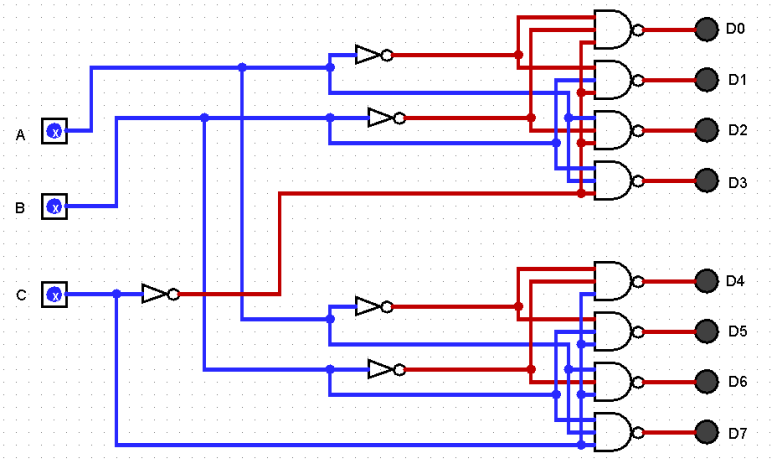
QUESTION 4:

Design a 3x8 Decoder using two 2x4 Decoders (74LS139).

ANSWER:

We can easily make a 3x8 decoder using two 2x4 decoders.

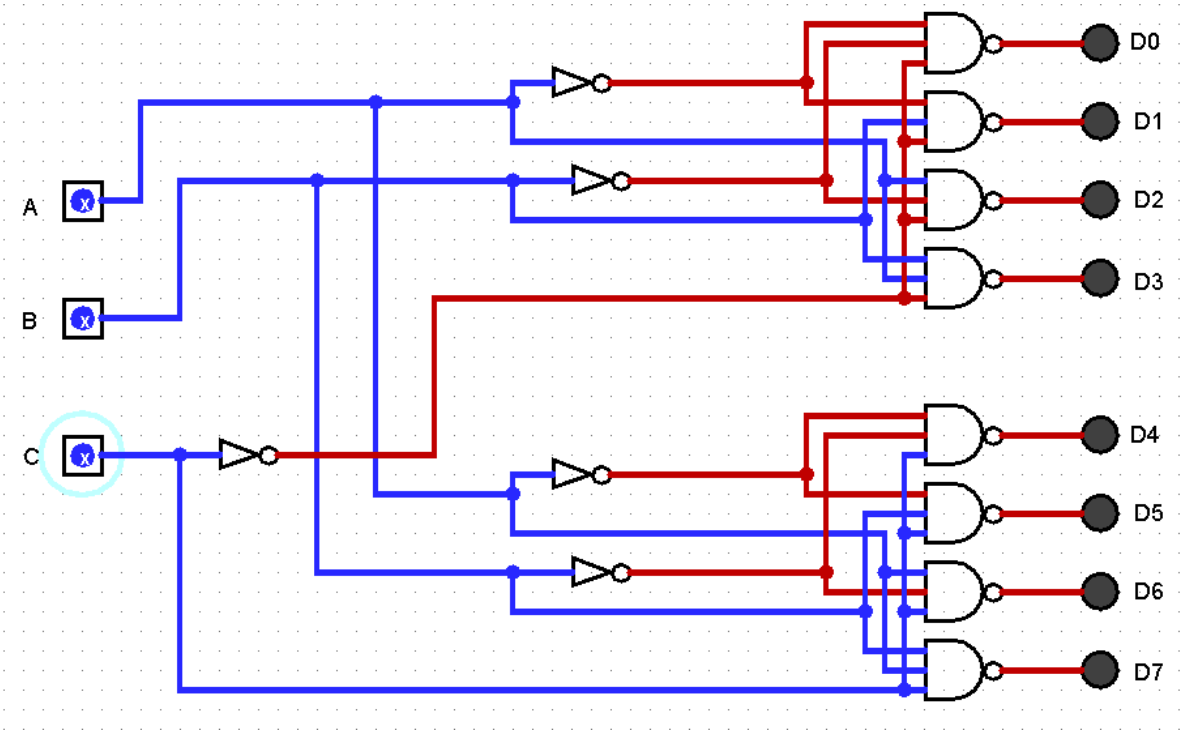
The circuit is as following.



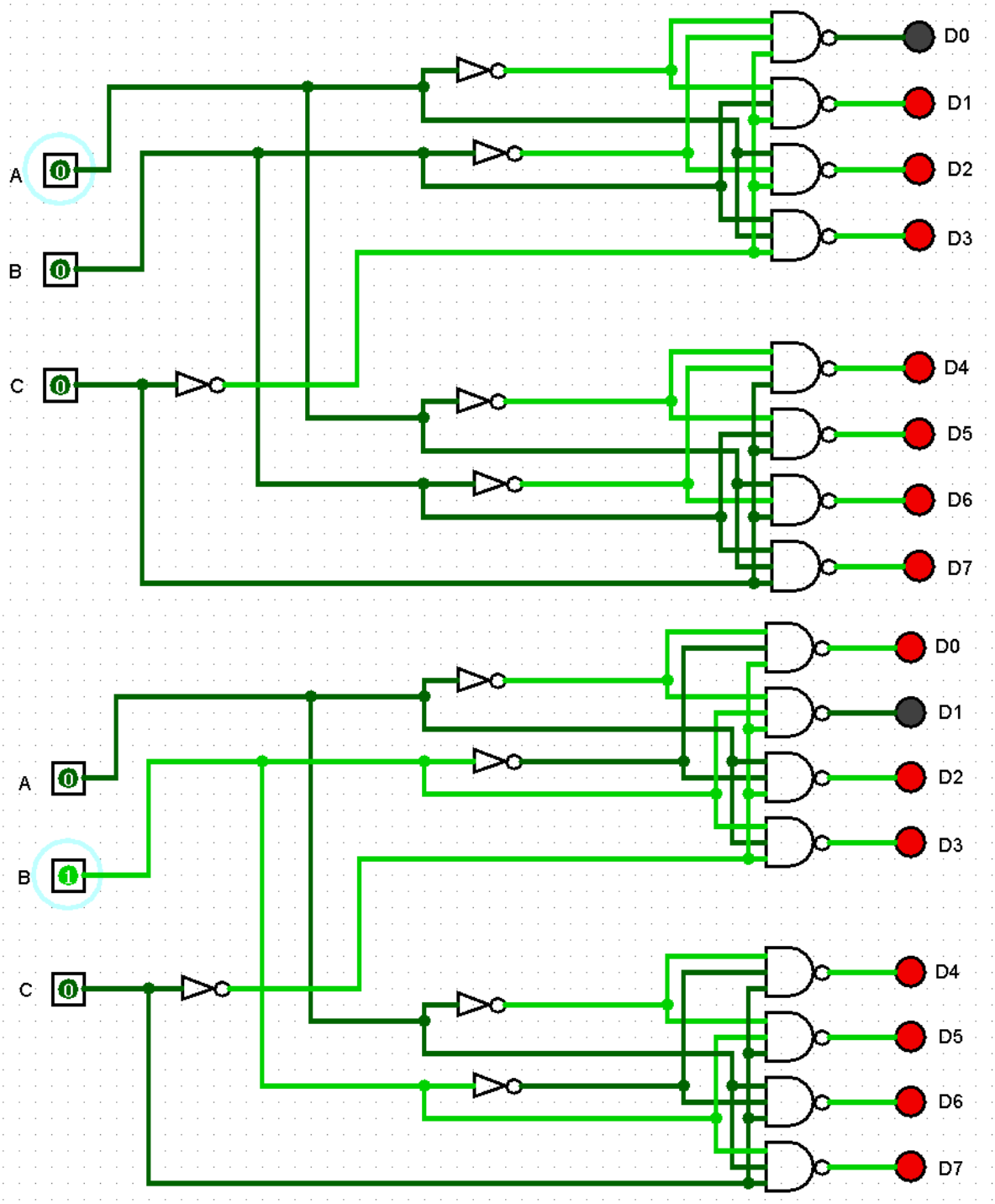
Now we construct the truth table:

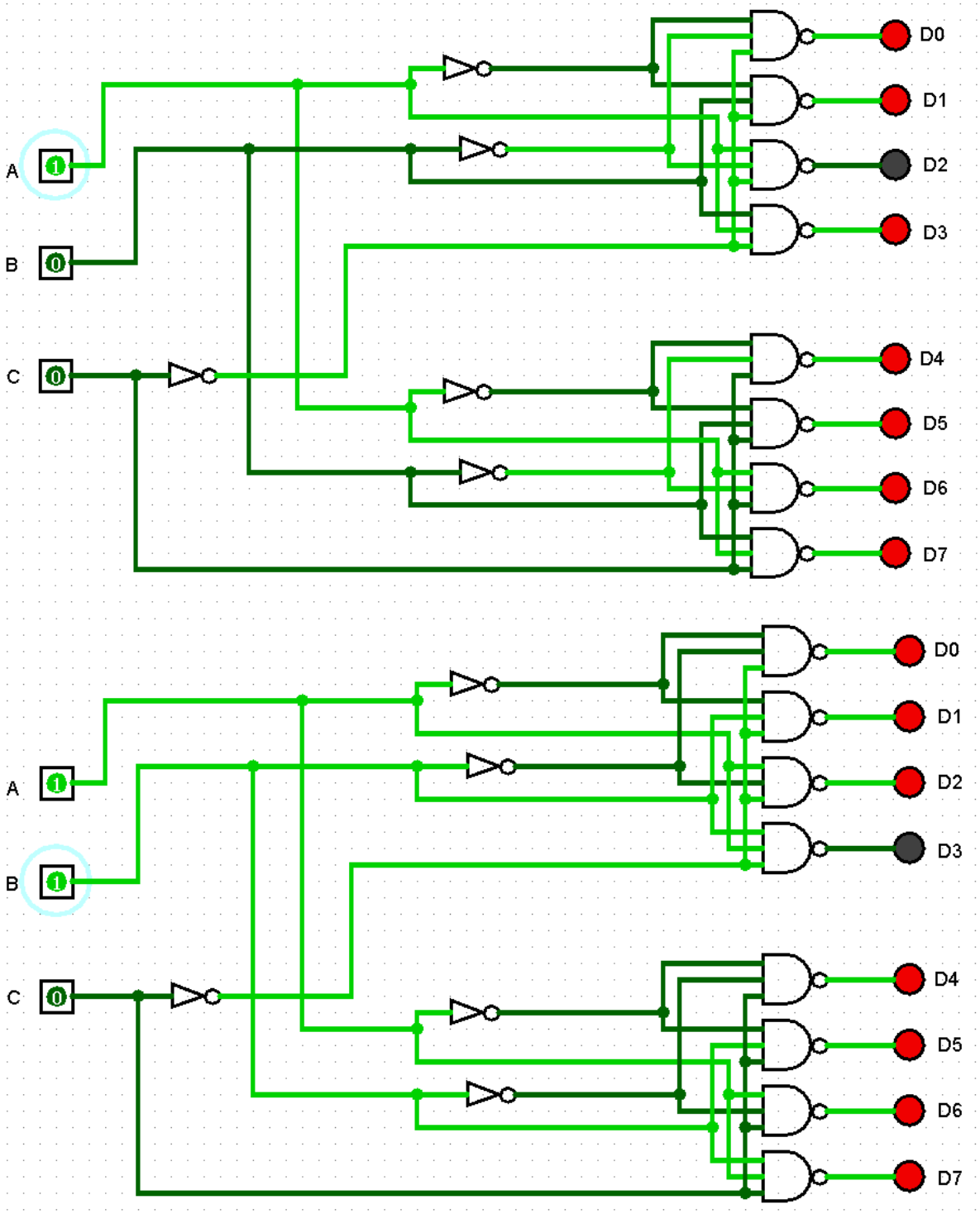
E	A	B	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Since we are using Enable active at low input than we get outputs at low also. We get 0 as output.



Now the observations:


A
B
C
D0
D1
D2
D3
D4
D5
D6
D7
A
B
C
D0
D1
D2
D3
D4
D5
D6
D7


A
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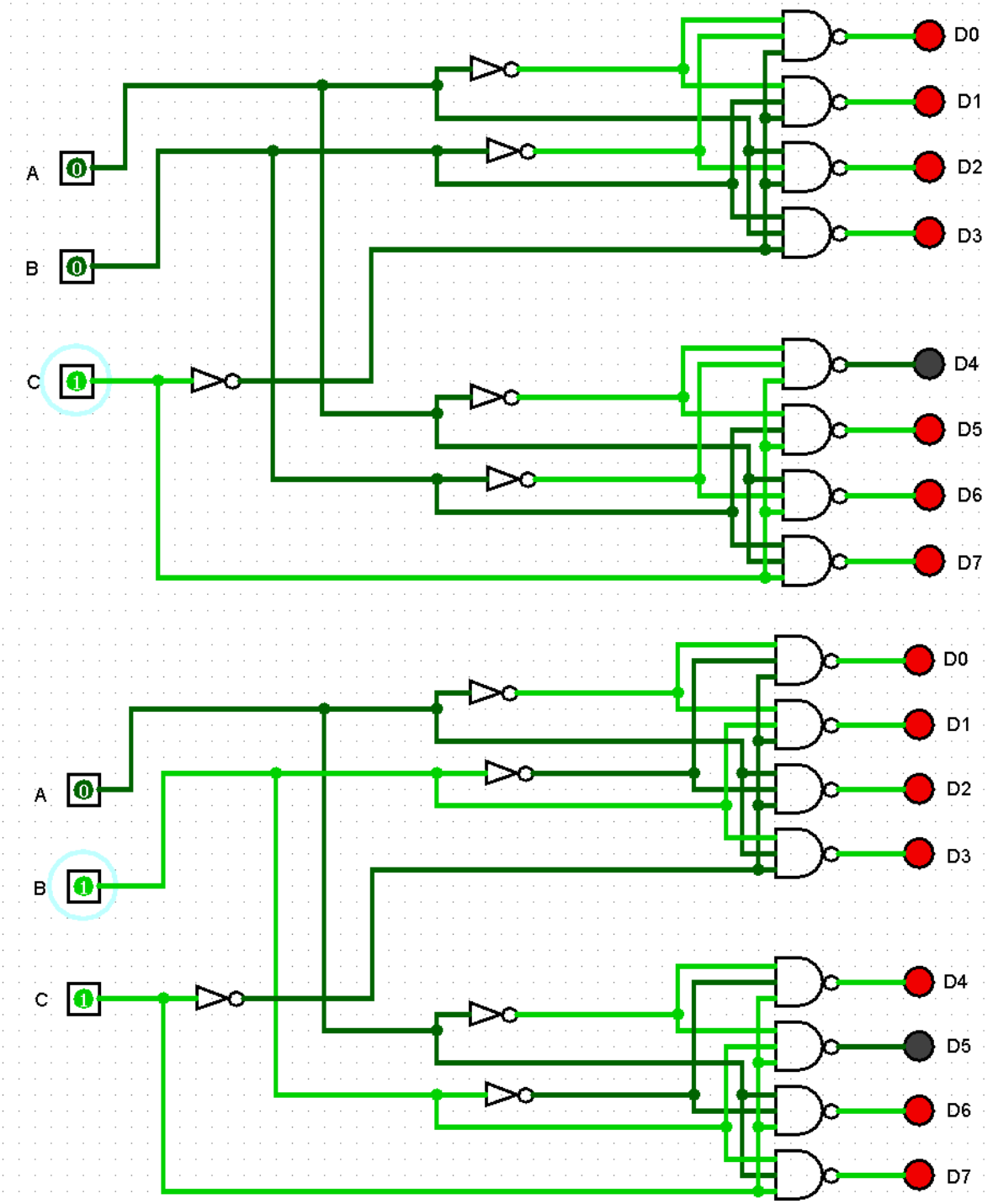
D6
D7


A
B
C
0
0
1
D0
D1
D2
D3
D4
D5
D6
D7
A
B
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D1
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D3
D4
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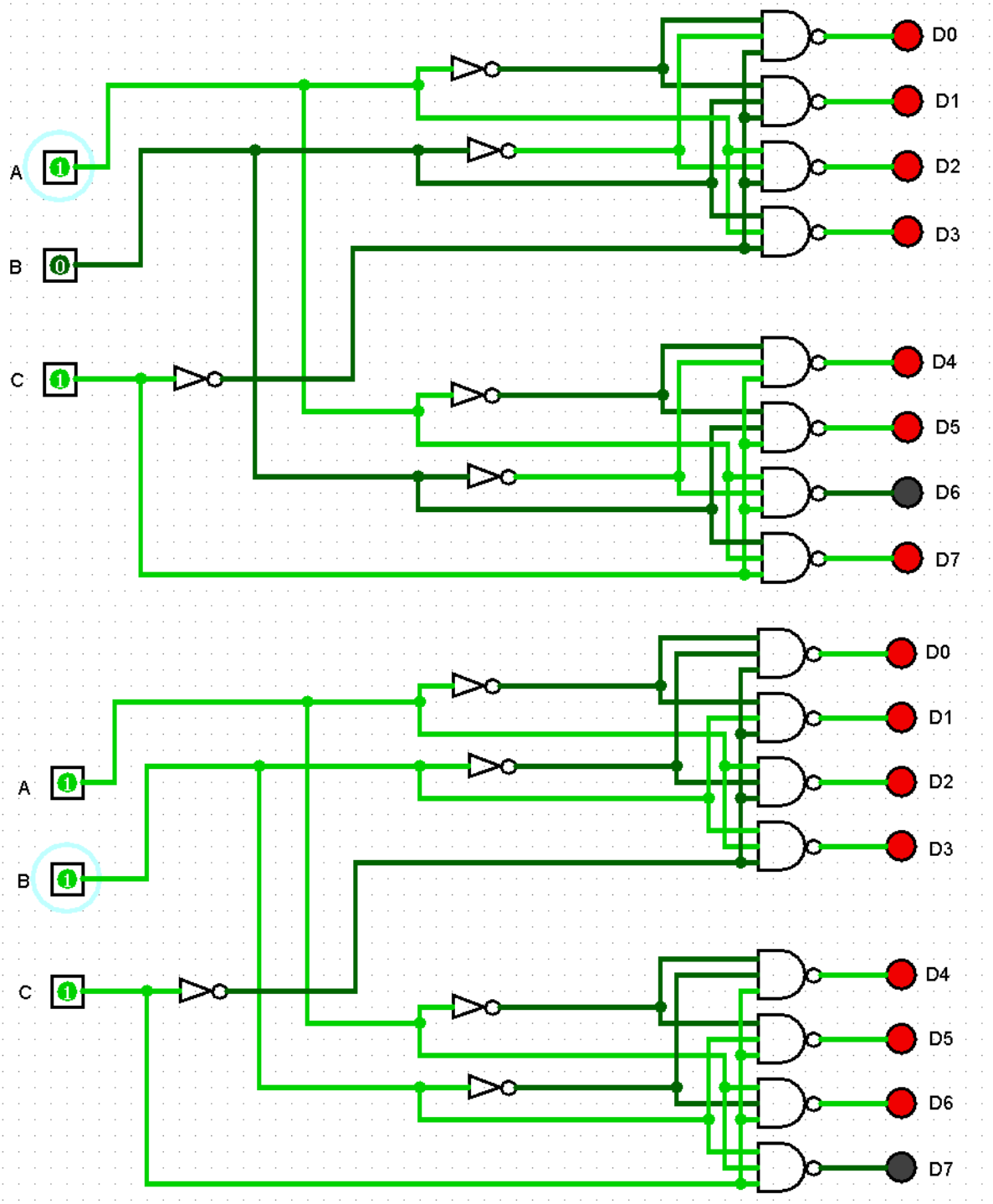
D6
D7


A
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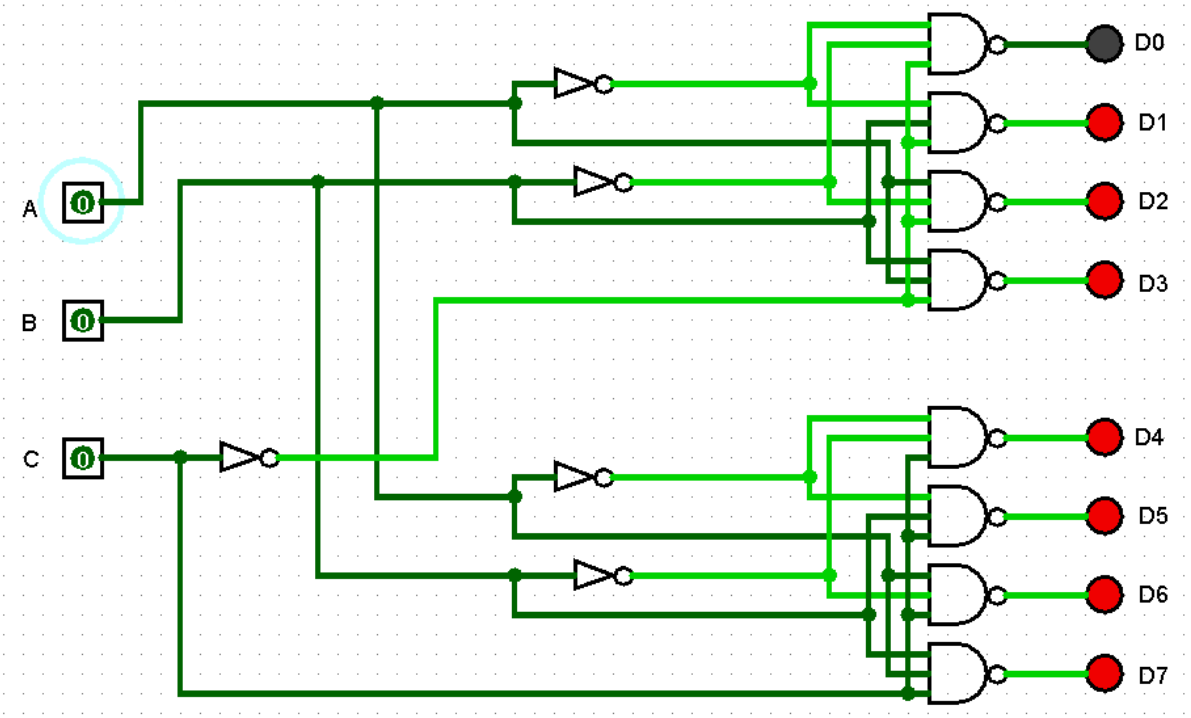

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