

# **LAB # 11**

# CSE-202L Digital Logic Design Lab Fall 2022

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# **DATED:**

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# **SUBMITTED TO:**

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#### **OBJECTIVES**

After completing this experiment, you will be able to:

- Design and verify a 4-bit Ripple Counter
- Design and verify MOD-10 and MOD-12 Ripple Counter
- Explain how a Ripple Counter can be used as a frequency divider

#### **COMPONENTS REQUIRED**

- Two 7476 (JK Flip-Flop ICs)
- One 7400 (2-Input NAND gate)

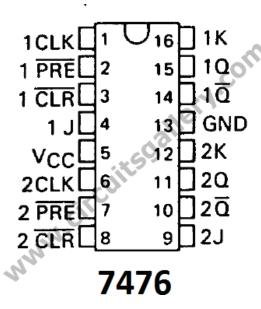
#### **THEORY**

A circuit used for counting the pulses is known as Counter. Basically there are two types of Counters: Asynchronous Counters (Ripple Counters) and Synchronous Counters.

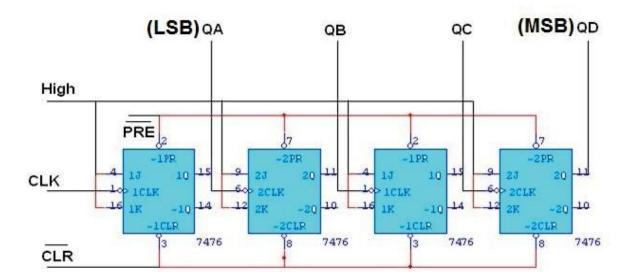
**Asynchronous Counter:** In the case of an Asynchronous Counter, all the Flip-Flops are not clocked simultaneously. This Counter is simple in operation & requires a minimum of hardware. But its speed is slow. Each FF is triggered by a previous FF o/p. Each FF takes its own time to give o/p (due to propagation delay). So final settling time is high.

**Synchronous Counter:** In Synchronous Counter all the FFs are clocked simultaneously. It is complex in construction, but speed is more. In this case since each FF is clocked simultaneously thus settling time is the delay time of single FF.

#### PIN DIAGRAM FOR IC 7476



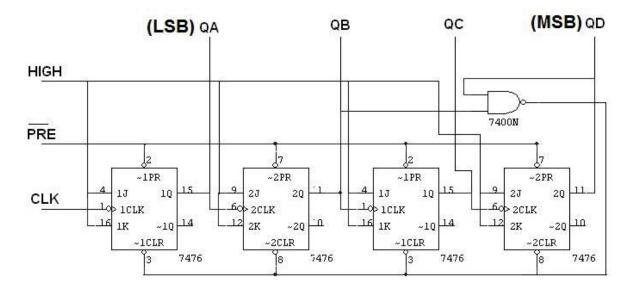
### **LOGIC DIAGRAM FOR 4-BIT RIPPLE COUNTER**



# **TRUTH TABLE**

| CV V |    | O.D. | 0.0 | O.D. |
|------|----|------|-----|------|
| CLK  | QA | QB   | QC  | QD   |
| 0    | 0  | 0    | 0   | 0    |
| 1    | 1  | 0    | 0   | 0    |
| 2    | 0  | 1    | 0   | 0    |
| 3    | 1  | 1    | 0   | 0    |
| 4    | 0  | 0    | 1   | 0    |
| 5    | 1  | 0    | 1   | 0    |
| 6    | 0  | 1    | 1   | 0    |
| 7    | 1  | 1    | 1   | 0    |
| 8    | 0  | 0    | 0   | 1    |
| 9    | 1  | 0    | 0   | 1    |
| 10   | 0  | 1    | 0   | 1    |
| 11   | 1  | 1    | 0   | 1    |
| 12   | 0  | 0    | 1   | 1    |
| 13   | 1  | 0    | 1   | 1    |
| 14   | 0  | 1    | 1   | 1    |
| 15   | 1  | 1    | 1   | 1    |

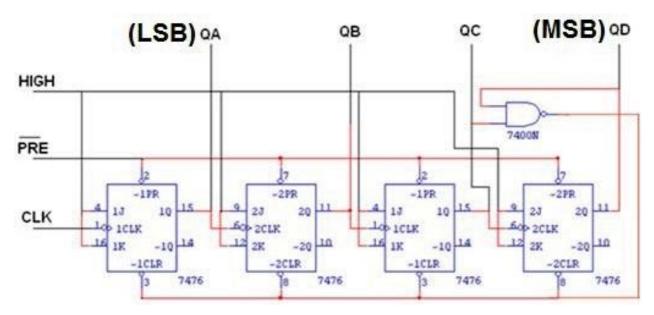
### **LOGIC DIAGRAM FOR MOD-10 RIPPLE COUNTER**



### **TRUTH TABLE**

| CLK | QA | QB | QC | QD |
|-----|----|----|----|----|
| 0   | 0  | 0  | 0  | 0  |
| 1   | 1  | 0  | 0  | 0  |
| 2   | 0  | 1  | 0  | 0  |
| 3   | 1  | 1  | 0  | 0  |
| 4   | 0  | 0  | 1  | 0  |
| 5   | 1  | 0  | 1  | 0  |
| 6   | 0  | 1  | 1  | 0  |
| 7   | 1  | 1  | 1  | 0  |
| 8   | 0  | 0  | 0  | 1  |
| 9   | 1  | 0  | 0  | 1  |
| 10  | 0  | 0  | 0  | 0  |

# **LOGIC DIAGRAM FOR MOD-12 RIPPLE COUNTER**



# **TRUTH TABLE**

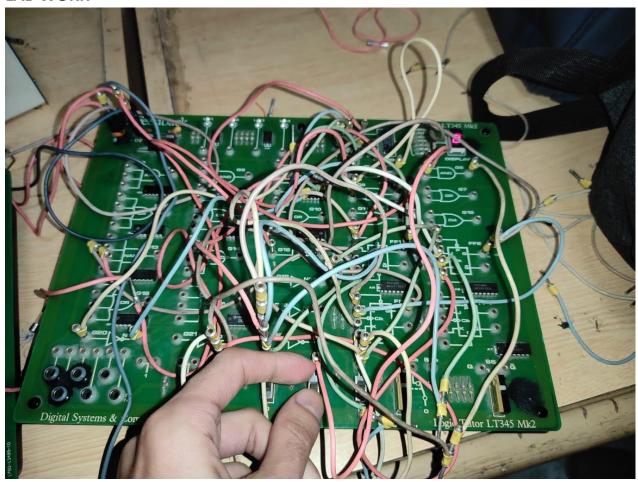
| CLK | QA | QB | QC | QD |
|-----|----|----|----|----|
| 0   | 0  | 0  | 0  | 0  |
| 1   | 1  | 0  | 0  | 0  |
| 2   | 0  | 1  | 0  | 0  |
| 3   | 1  | 1  | 0  | 0  |
| 4   | 0  | 0  | 1  | 0  |
| 5   | 1  | 0  | 1  | 0  |
| 6   | 0  | 1  | 1  | 0  |
| 7   | 1  | 1  | 1  | 0  |
| 8   | 0  | 0  | 0  | 1  |
| 9   | 1  | 0  | 0  | 1  |
| 10  | 0  | 1  | 0  | 1  |

| 11 | 1 | 1 | 0 | 1 |
|----|---|---|---|---|
| 12 | 0 | 0 | 0 | 0 |

### **PROCEDURE**

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

### **LAB WORK**



#### **REVIEW QUESTIONS**

1. Counters can be used as frequency dividers. When the clock frequency in the 4-bit Ripple Counter given above is 1 kHz, what will be the output frequency of Flip-Flop A and Flip-Flop B?

fA = Half of Clock Frequency

fB =Quarter of Clock Frequency

2. Would inverters on the clock inputs change the count direction of a Ripple Counter?

Yes, result will be in reverse direction

3. How many Flip-Flops are needed to build a MOD-5 Counter?

At least 3 flip flop since mod equals 2 squared the flip-flop number