LAB # 7

CSE-202L Digital Logic Design Lab

Fall 2022

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LAB 7

MULTIPLEXER AND DEMULTIPLEXER

1 OBJECTIVES

After completing this experiment, you will be able to:

- Design and construct Multiplexer and DeMultiplexer
- Verify their truth tables using basic logic gates

2 COMPONENTS REQUIRED

- Two 7411, 3 I/P AND gates
- 7432, 2 I/P OR gate
- 7404, hex inverter

3 THEORY

MULTIPLEXER:

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^ninput line and n selection lines whose bit combination determine which input is selected.

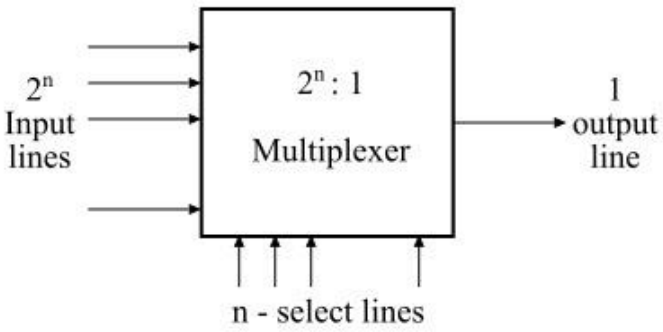


Figure 1 - Multiplexer

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1x4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

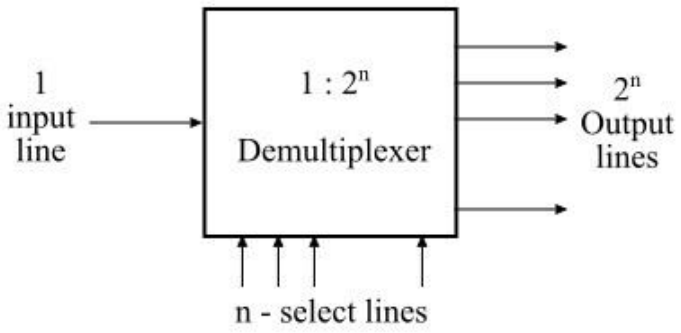
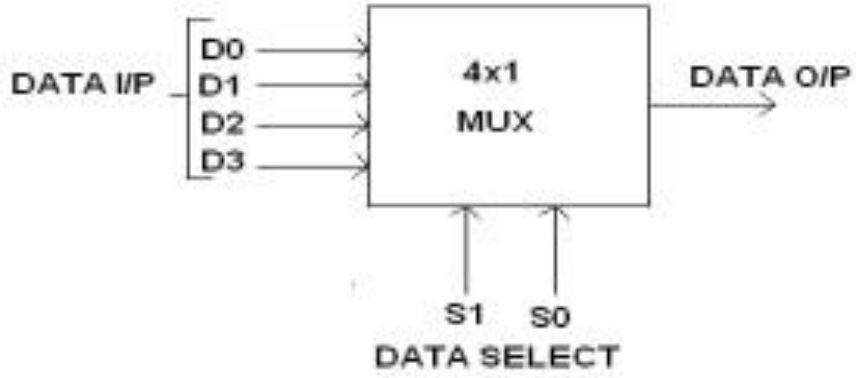


Figure 2 - Demultiplexer

BLOCK DIAGRAM FOR 4x1 MULTIPLEXER:

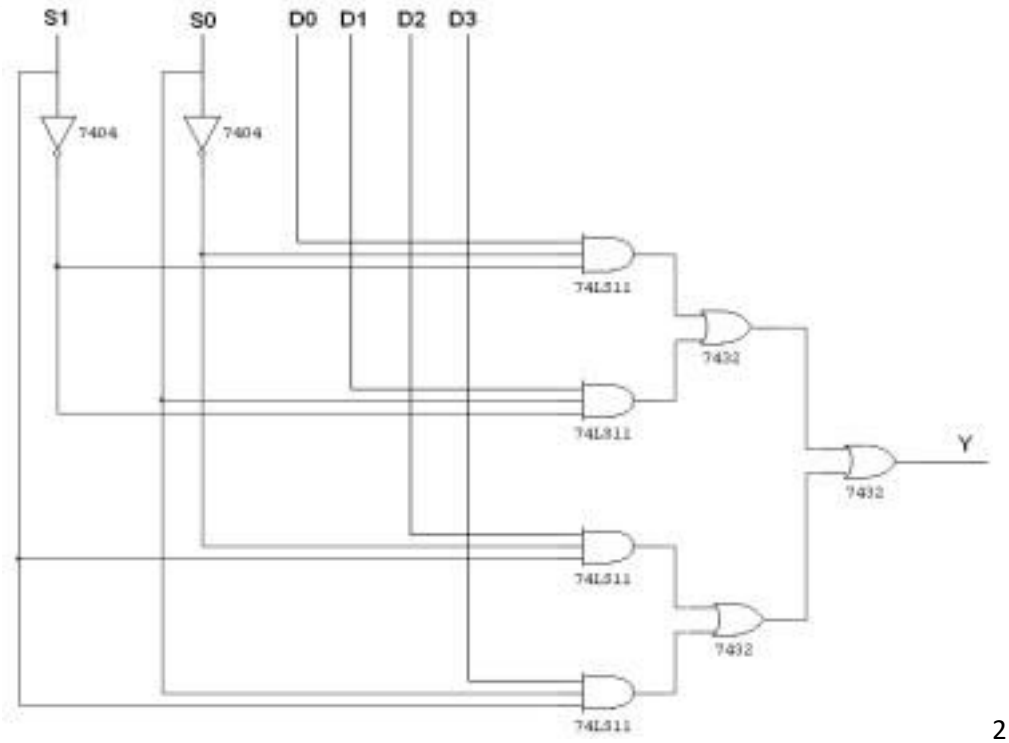


FUNCTION TABLE:

S1	S0	OUTPUT Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

CIRCUIT DIAGRAM FOR 4x1 MULTIPLEXER:



2

TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

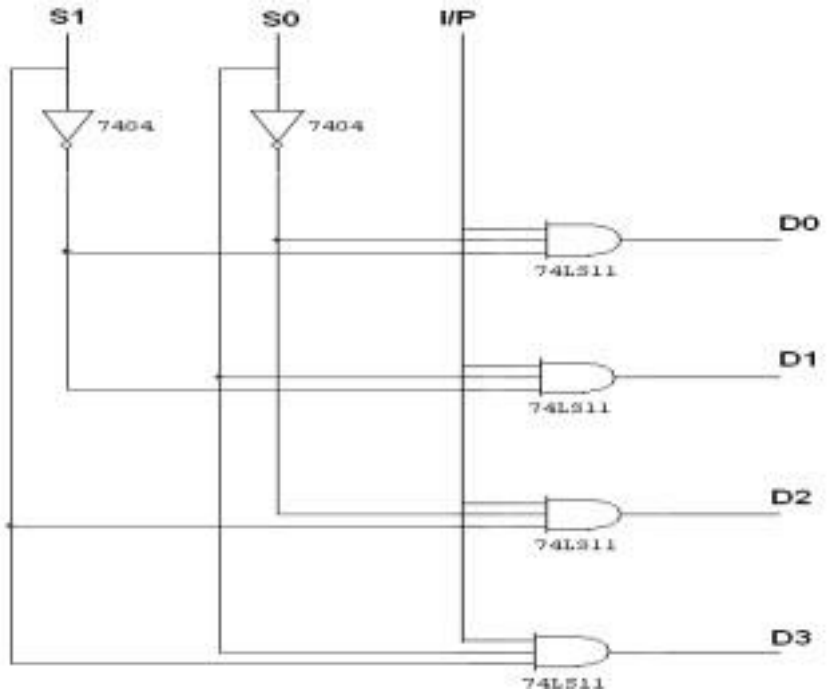
BLOCK DIAGRAM FOR 1x4 DEMULTIPLEXER:

FUNCTION TABLE:

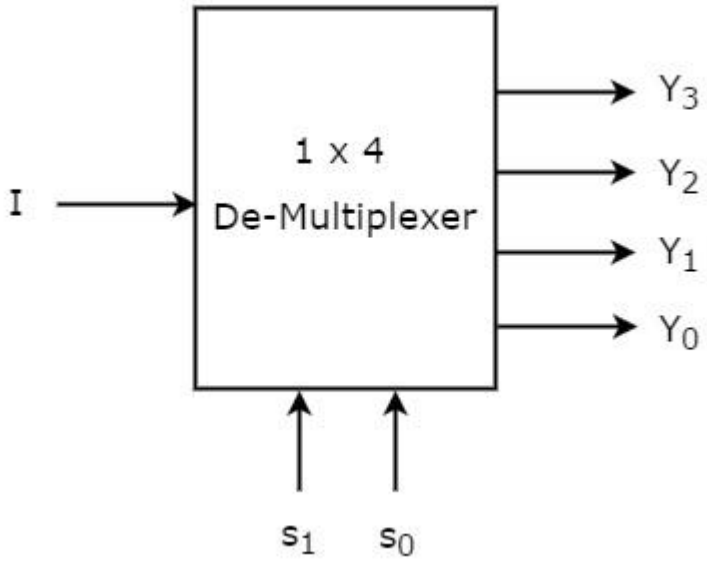
S1	S0	OUTPUT
0	0	X → D0 = X S1’ S0’
0	1	X → D1 = X S1’ S0
1	0	X → D2 = X S1 S0’
1	1	X → D3 = X S1 S0

Y = X S1’ S0’ + X S1’ S0 + X S1 S0’ + X S1 S0

LOGIC DIAGRAM FOR DEMULTIPLEXER:



BLOCK DIAGRAM:

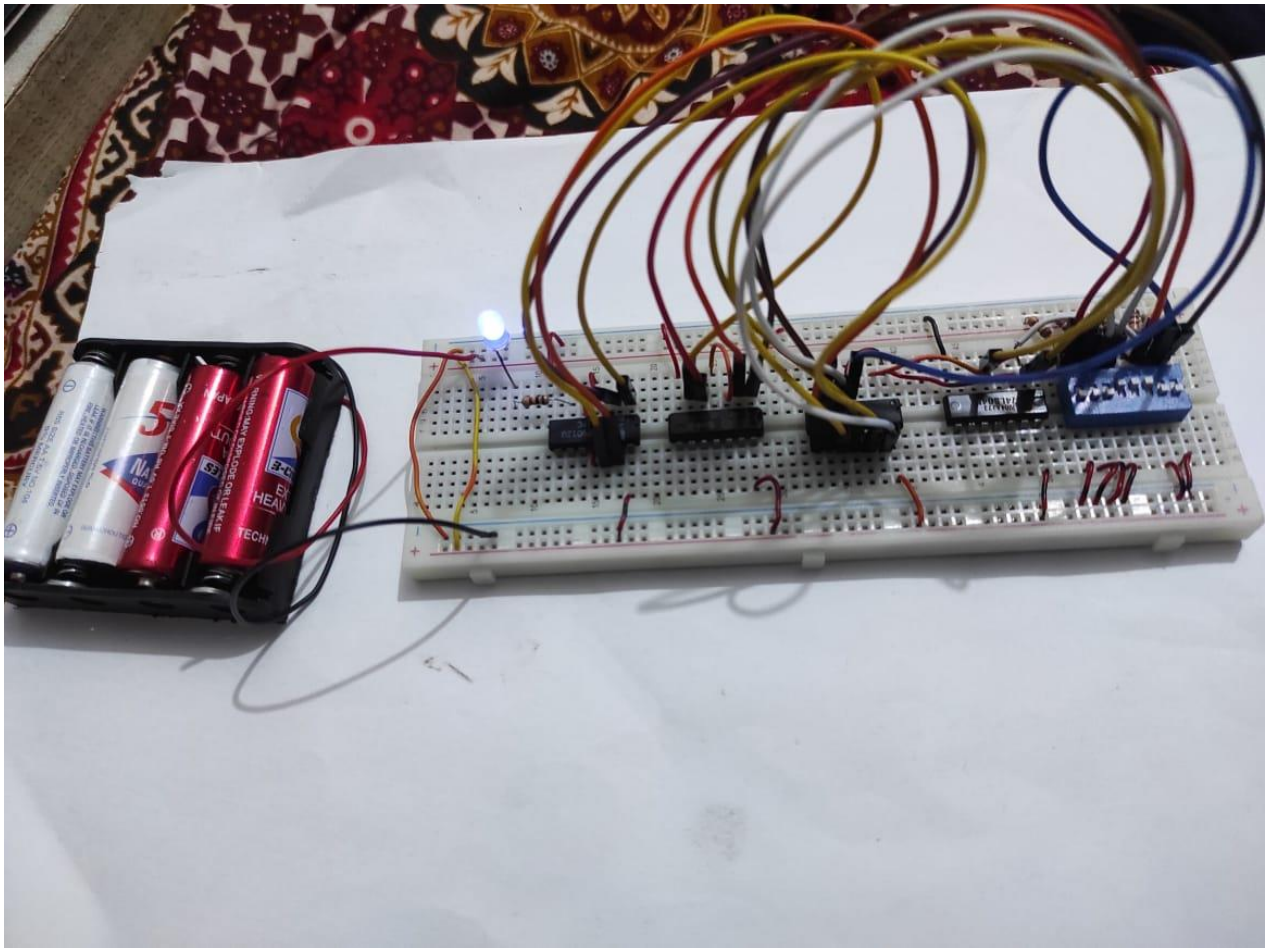


TRUTH TABLE:

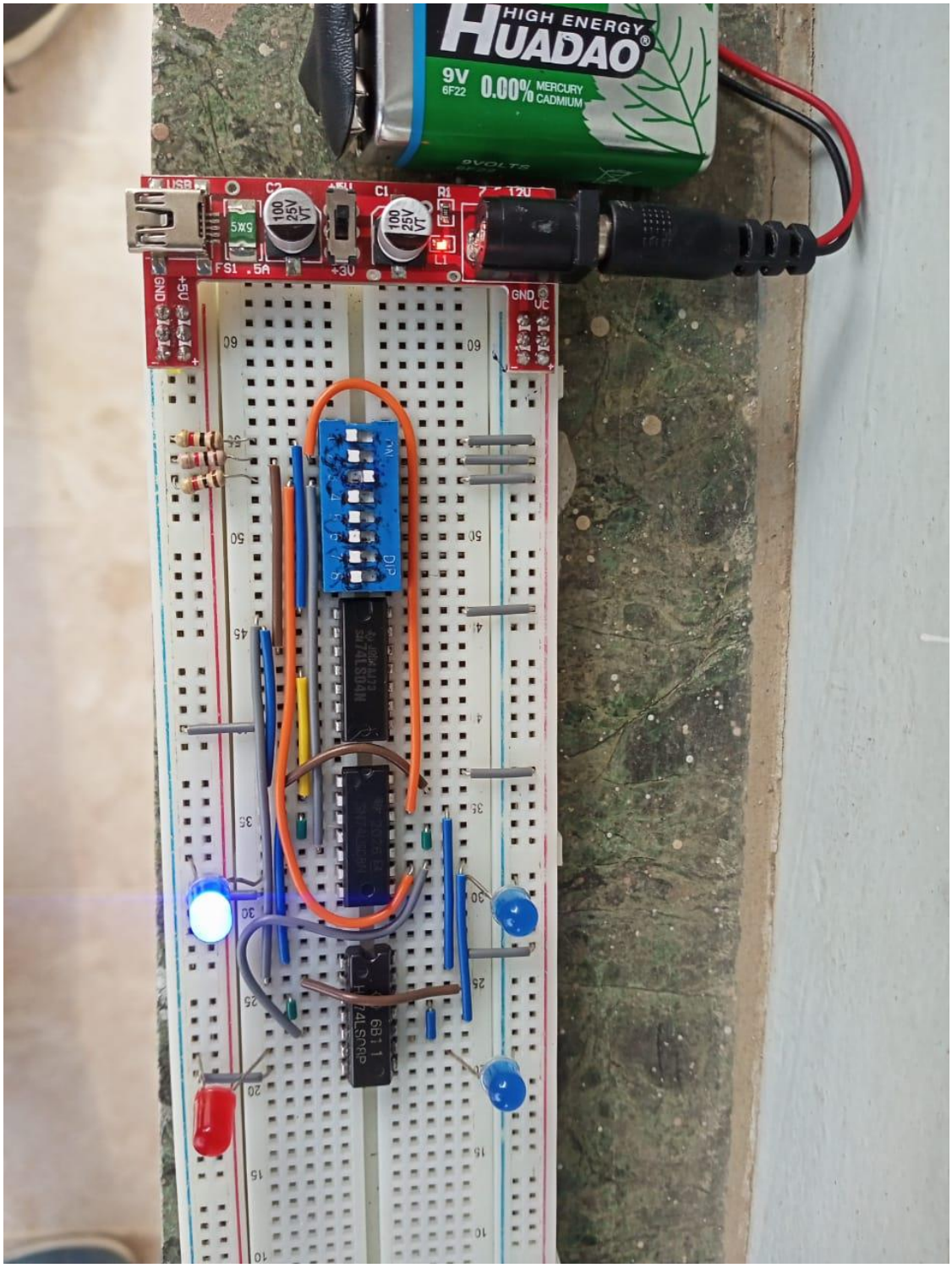
INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**0**	**1**

PROCEDURE

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.



4 x 1 Mux


HIGH ENERGY
HUADAO
9V
6F22
0.00% MERCURY
CADMIUM
USB
FS1 .5A
+3V
GND
+5V
GND
VC
DIP

1 x 4 Demux

REVIEW QUESTIONS:

QUESTON 1:

What is the difference between Multiplexer and De-Multiplexer?

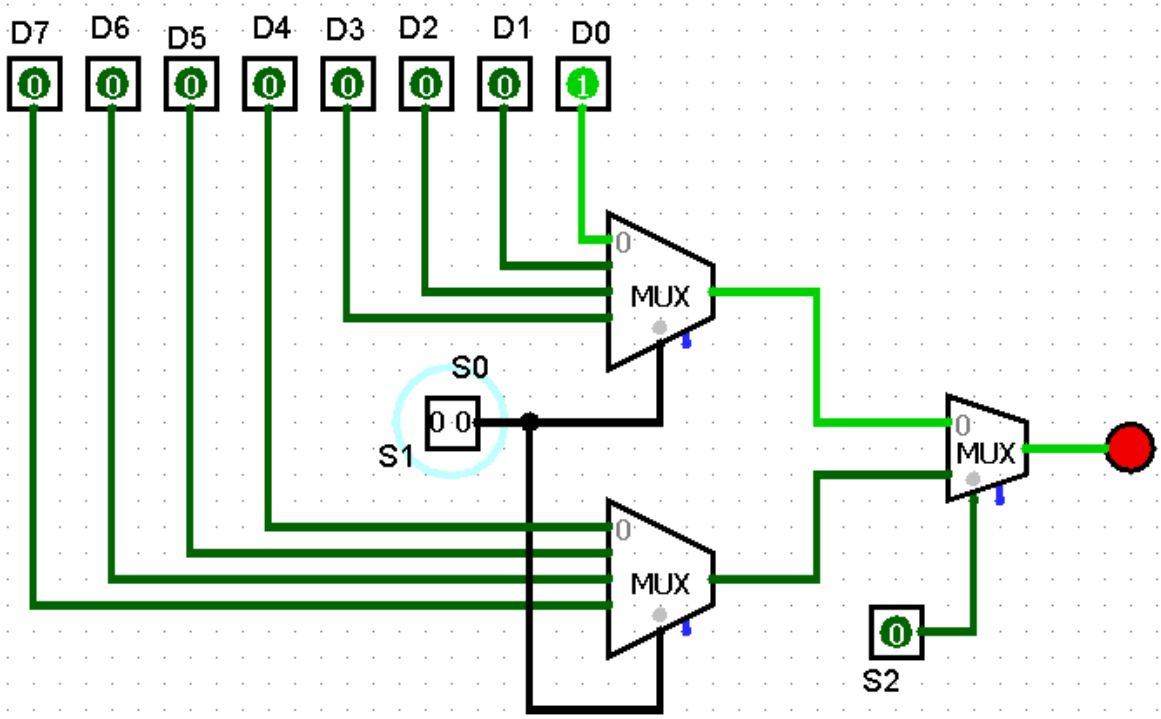
ANSWER:

MULTIPLEXER	DEMULTIPLEXER
Multiplexer processes the digital information from various sources into a single source	Demultiplexer receives digital information from a single source and converts it into several sources
It is known as Data Selector	It is known as Data Distributor
Multiplexer is a digital switch	Demultiplexer is a digital circuit
It follows combinational logic type	It follows combinational logic type
It has n data input	It has single data input
It has a single data output	It has n data outputs
It works on many to one operational principle	It works on one to many operational principle

QUESTON 2:

Design a 8x1 MUX using two 4x1 MUXes (74153) and a 2x1 MUX (74157).

ANSWER:


D7
D6
D5
D4
D3
D2
D1
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0
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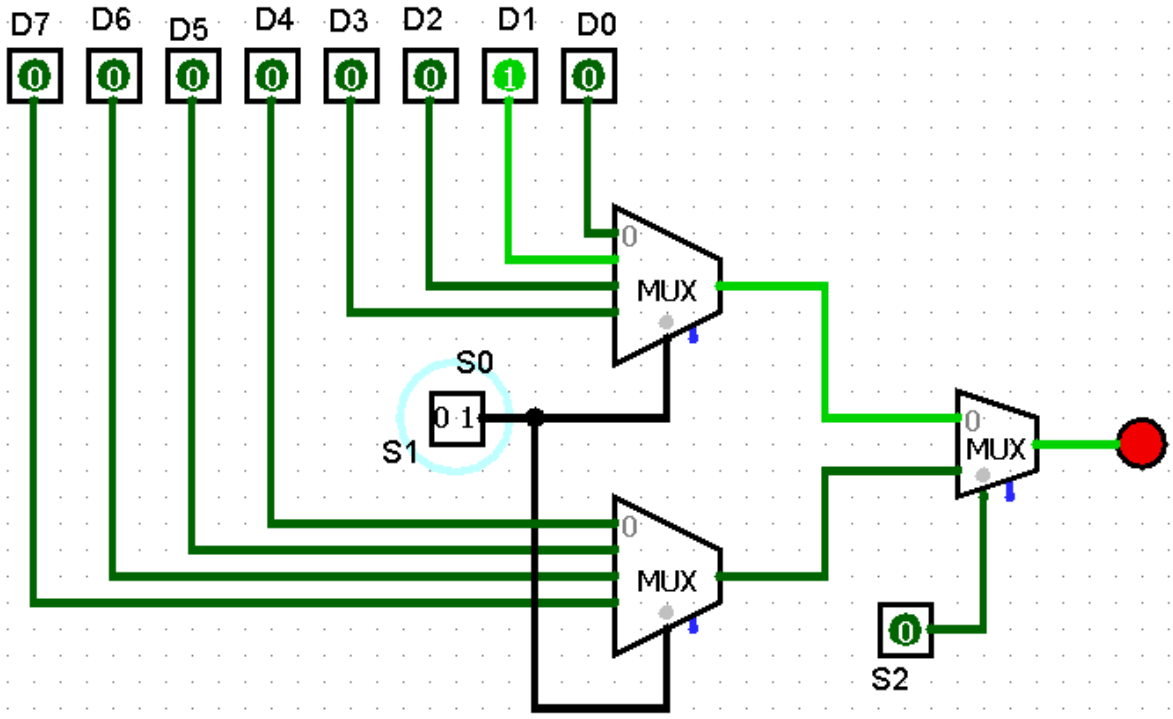
0
0
0
1
MUX
MUX
MUX
S0
0 0
S1
S2
0


D7
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D2
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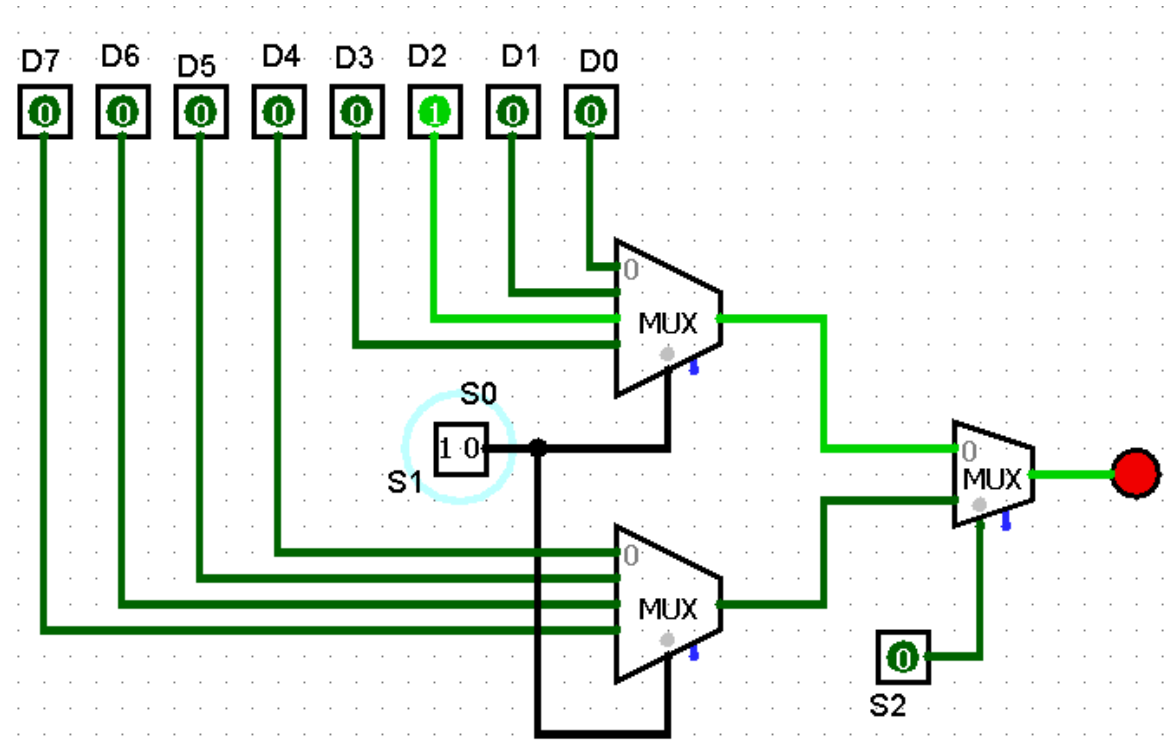
MUX
MUX
MUX
S0
0 1
S1
S2
0


D7
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D1
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MUX
S0
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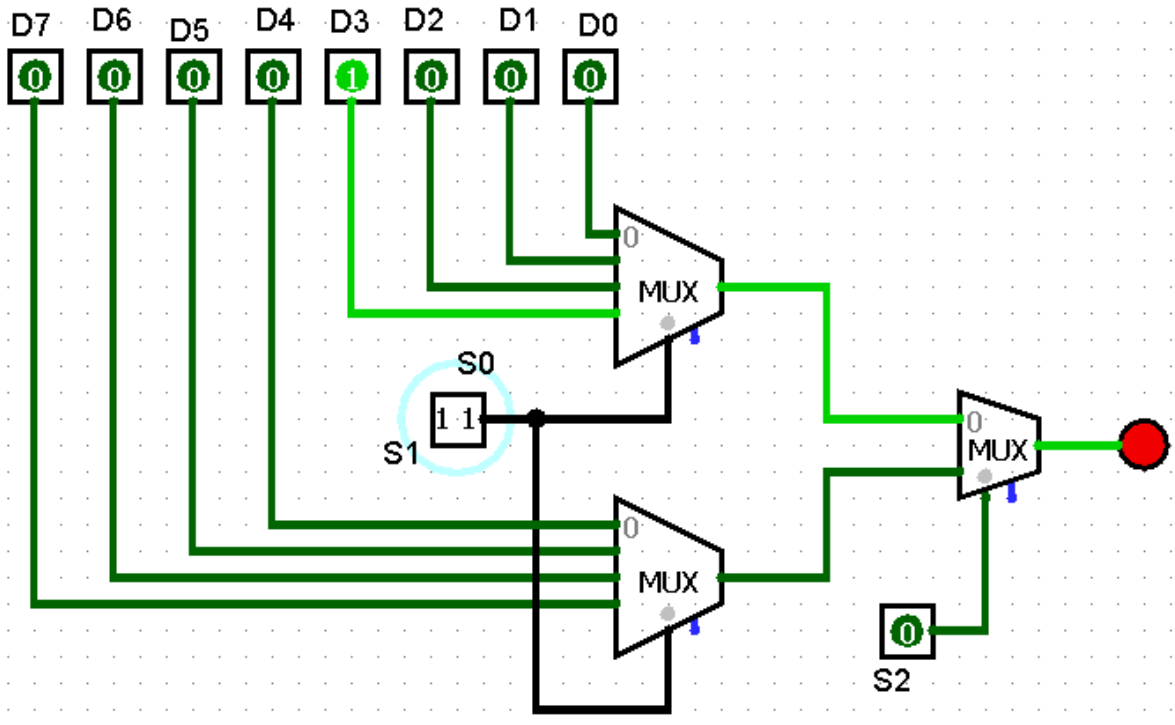
S1
MUX
MUX
0
S2


D7
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MUX
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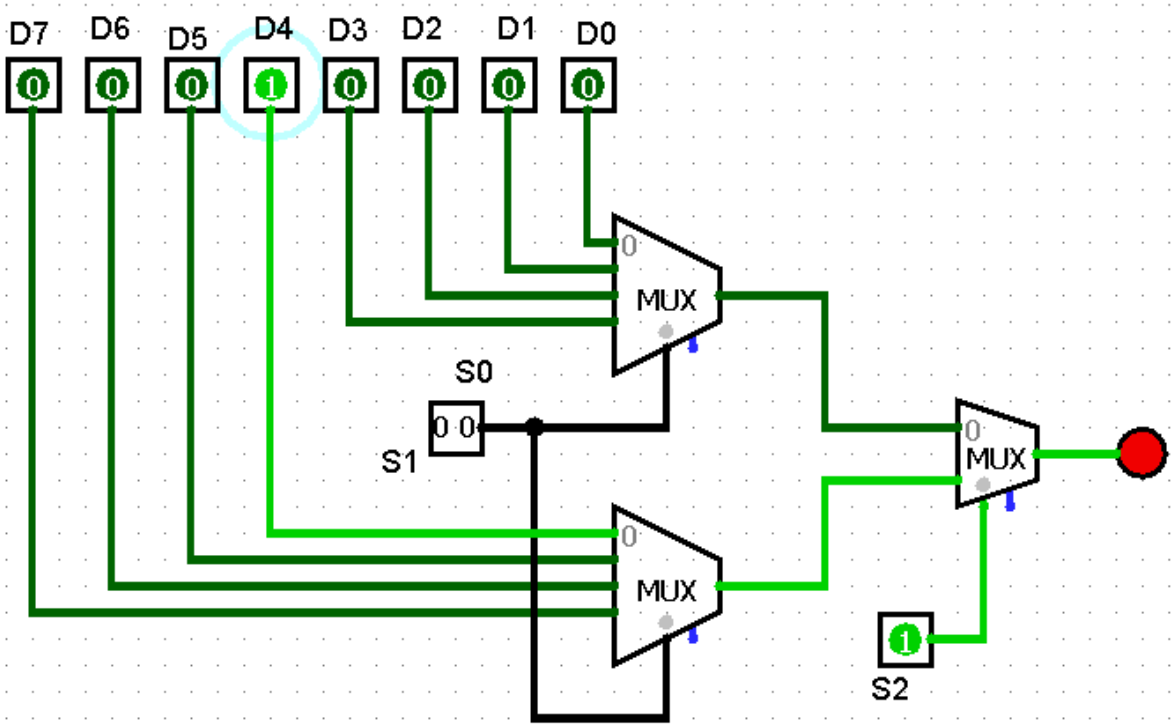
S1
MUX
MUX
0
S2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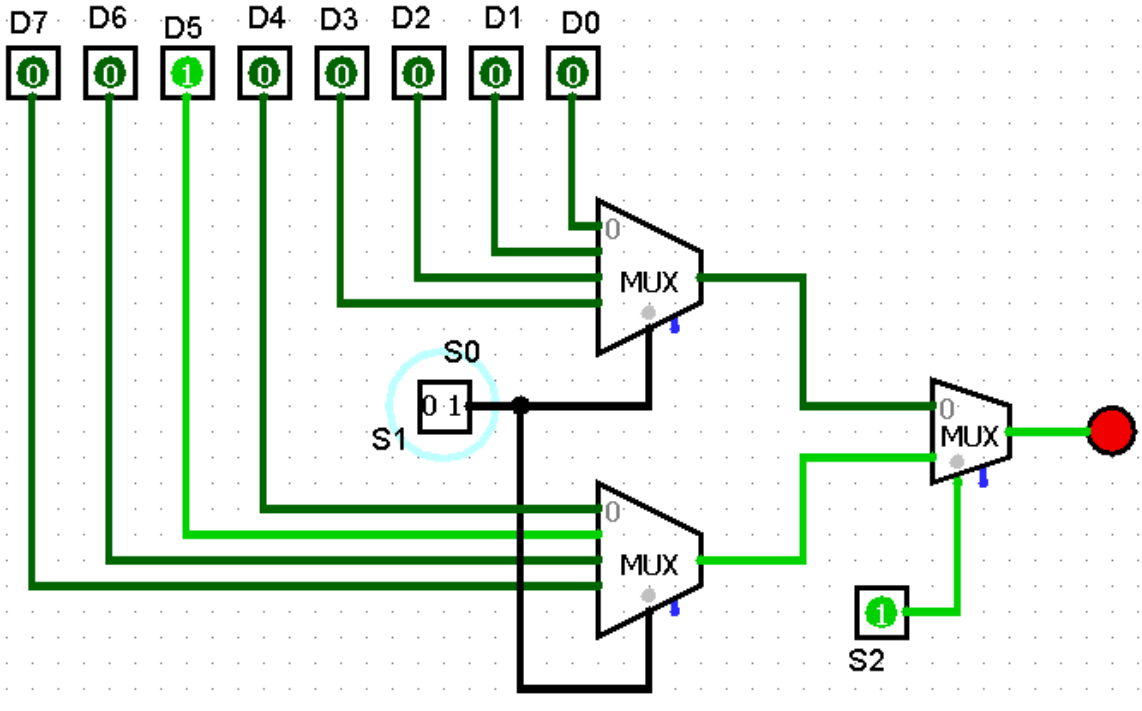
MUX
S0
0 0
S1
1
S2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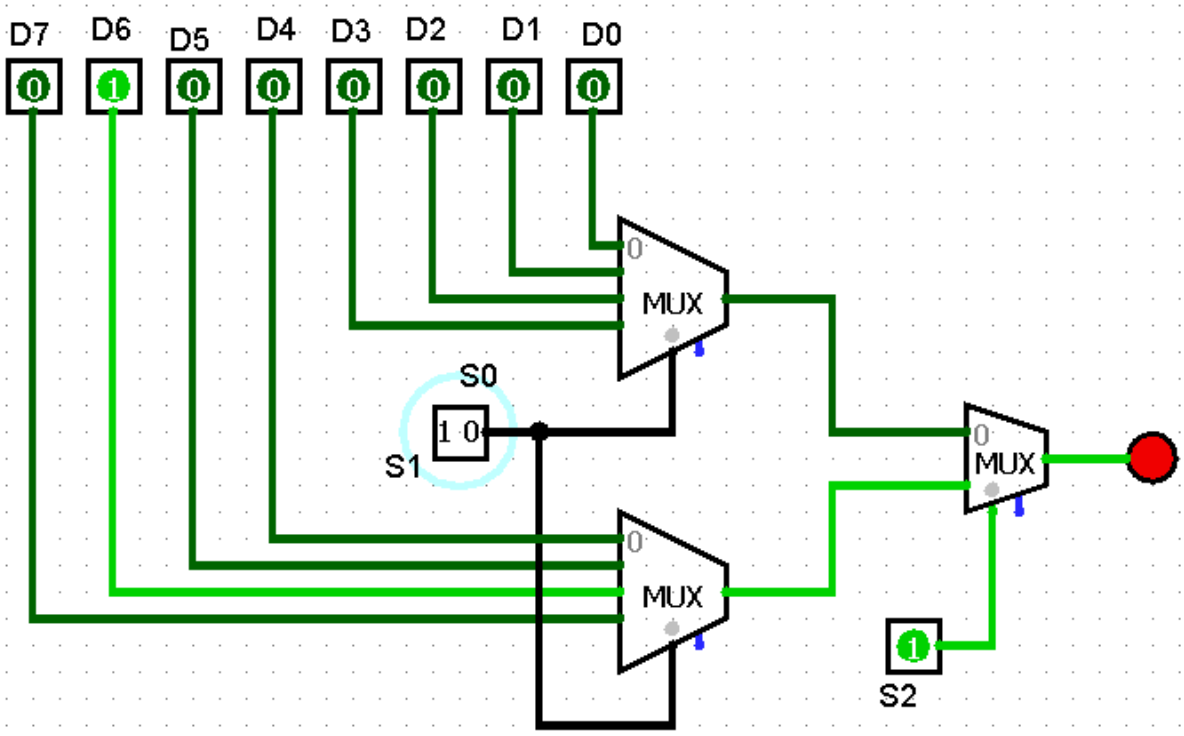
S1
1
S2


D7
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MUX
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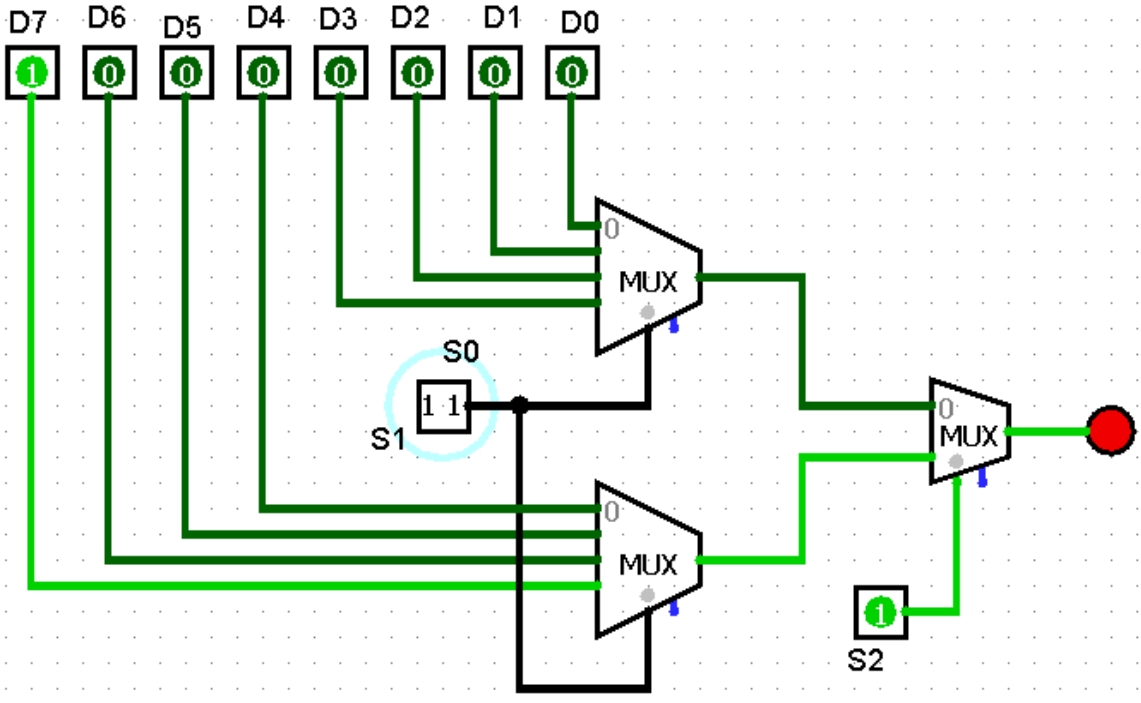
MUX
S0
S1
1 0
S2
1


D7
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0
MUX
MUX
MUX
S0
S1
1 1
S2
1

TRUTH TABLE:

S2	S1	S0	OUTPUT
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

4