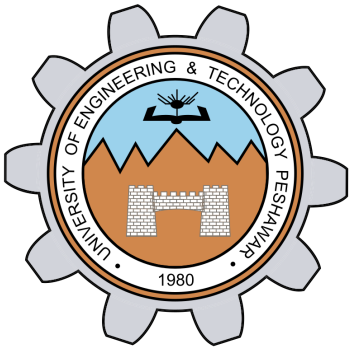
Assignment # 1



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CSE-420 Embedded Systems

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1 Timing Parameters

The timing parameters of DRAM (Dynamic Random Access Memory) are essential characteristics that define the latency and data transfer performance of DRAM modules. DRAM timing dictates how quickly memory cells can be accessed and refreshed and how fast data can be transferred to the processor. These parameters are especially crucial in DDR (Double Data Rate) DRAM technologies, where timing impacts the overall system performance. These timing parameters are measured in clock cycles and can be seen in figure 1 below.

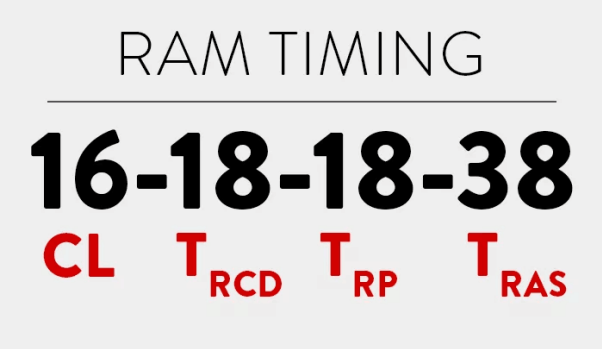

Figure 1: RAM Timing on a DRAM Stick

1.1 CAS Latency (CL)

CAS Latency (Column Access Strobe Latency), also known as "Access Time," is the most important memory parameter and is the first of the series of numbers. It is the delay time between the moment a memory controller tells the memory module to access a particular memory column on a RAM memory module, and the moment the data from given array location is available on the module's output pins. In DDR SDRAM it is specified in clock cycles, while in asynchronous DRAM it is specified in nanoseconds[1].

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 1, 2 or 3 clocks. If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n+m as shown in figure [2,3,4]

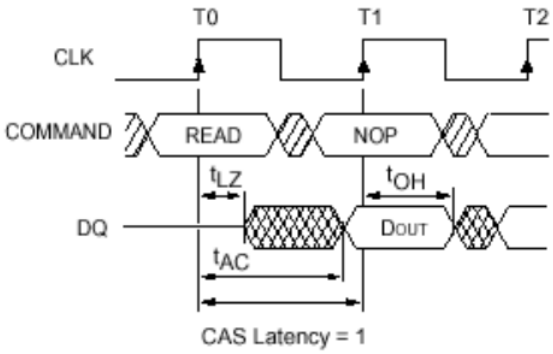

Figure 2: CAS Latency = 1

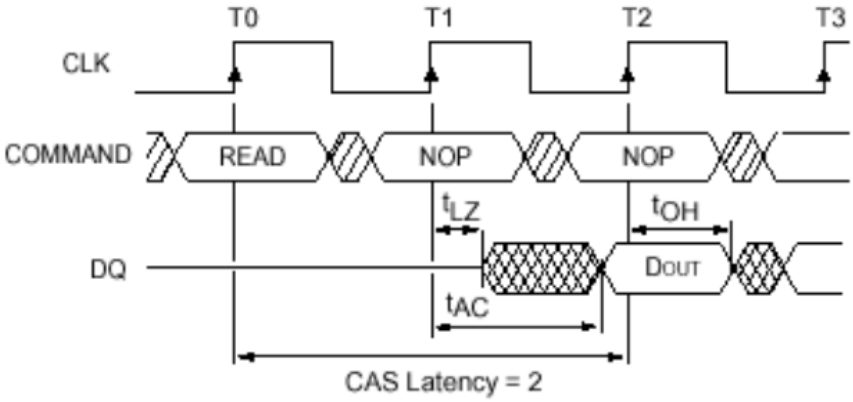

Figure 3: CAS Latency = 2

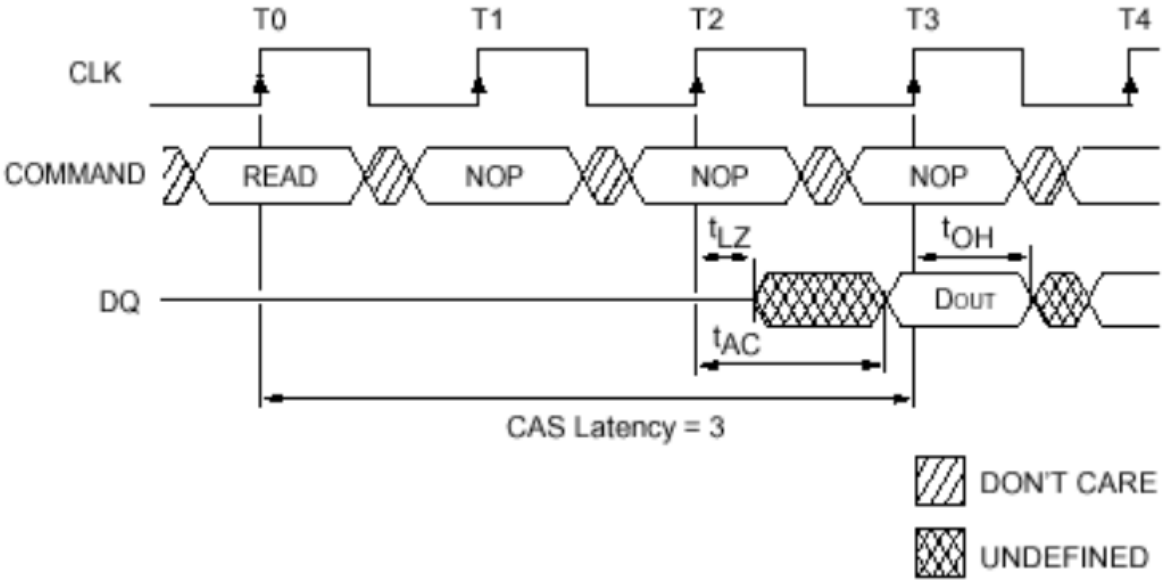

Figure 4: CAS Latency = 3

1.2 RAS to CAS Delay (tRCD)

tRCD stands for row address to column address delay time. Inside the memory, the process of accessing the stored data is accomplished by first activating the row then the column where it is located. tRCD is the time required between the memory controller asserting a row address strobe (RAS), and then asserting a column address strobe (CAS) during the subsequent read or write command. The lesser this time, the better it is, as the data will be read sooner.

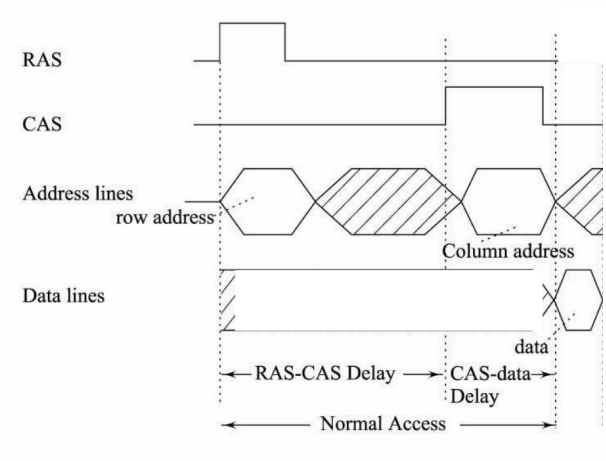

Figure 5: tRCD shown as RAS to CAS delay

1.3 RAS Precharge (tRP)

Whenever a new row is to be activated for the purpose of accessing a data bit, a command called "Precharge" needs to be issued to close the already activated row. RAS Precharge time, tRP is the number of clock cycles needed to terminate access to an open row of memory, and open access to the next row. In simple words, tRP, specifies the time required to complete one row access, deactivate that row, reactivate the next row, and begin the next row access. A simple graphical explanation of RAS Precharge (tRP) can be seen in figure 6.

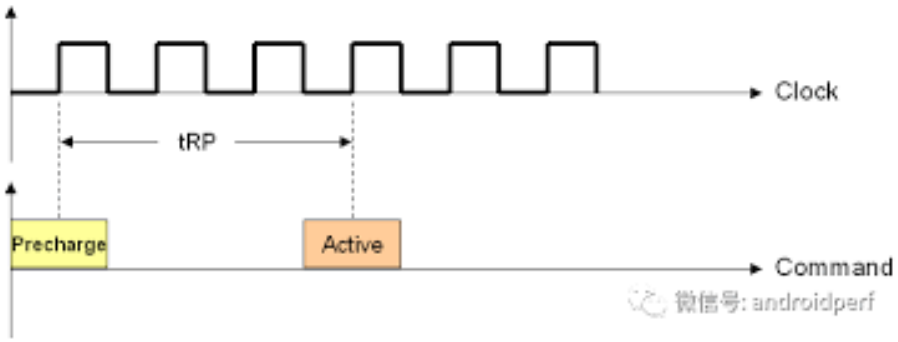

Figure 6: tRP delay [2]

1.4 Active to Precharge Delay (tRAS)

After an "Active" command is issued, another "Precharge" command cannot be issued until tRAS has elapsed. So, tRAS is the minimum number of clock cycles needed to access a certain row of data in the memory between the data request (Active) and the Precharge command. Basically, this parameter limits when the memory can start reading (or writing) a different row.

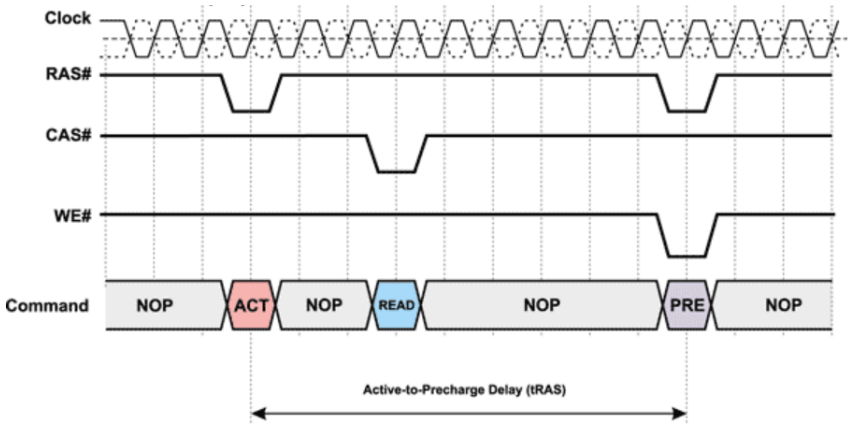

Figure 7: tRAS delay [3]

References

[1] F. Semiconductor, "Understanding ddr sdram timing parameters," https://www.eetimes.com/understanding-ddr-sdram-timing-parameters/, accessed: 2024-10-01.

[2] C. Tencent, "Understanding ram timings," https://cloud.tencent.com/developer/article/2003206.

[3] https://compress.ru/article.aspx?id=16737.