Emerging Computing Architectures

Asif Ali Khan

Fall Semester 2024

Department of Computer Systems Engineering

UET Peshawar

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- Computer Architecture and/or Digital System Design

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What to expect from this course:

- Introduction to the state-of-the-art research in computing systems
- The landscape of novel methods in computing
- A lot of self-reading (mostly research articles)

Von Neumann Architecture and the Main Memory Subsystem

Fixed program vs. stored program computers

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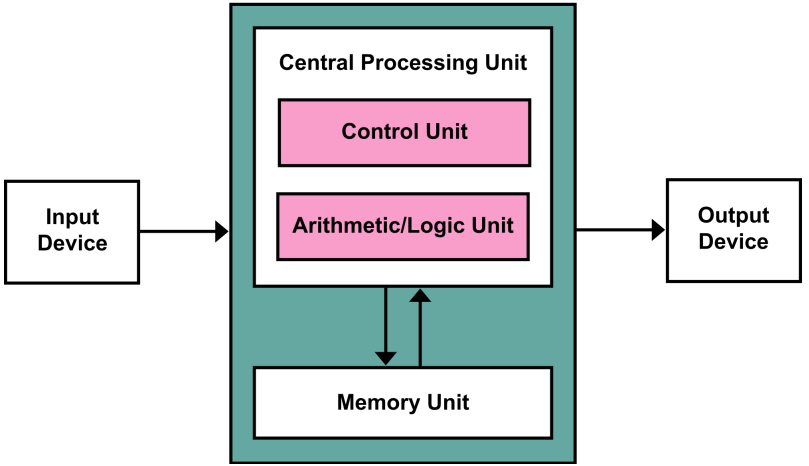
- Modern systems are based on stored-program concept
  - Introduced by John Von Neumann

Von-Neumann architecture

- Consists of three basic components:
  1. CPU
  2. Memory
  3. I/O interfaces



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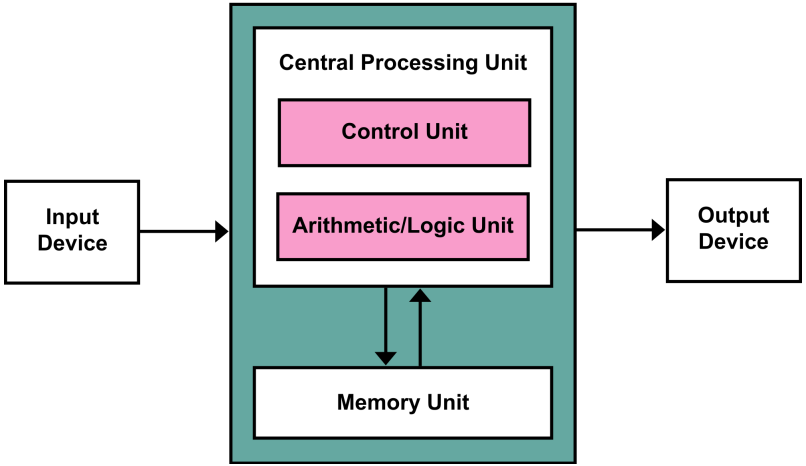

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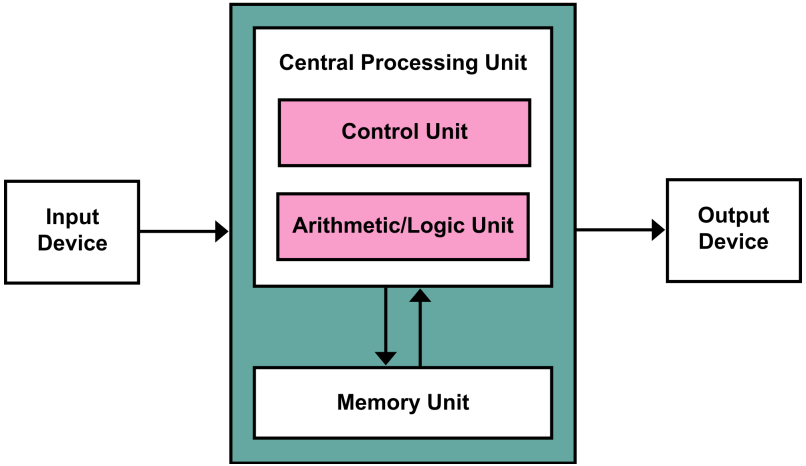

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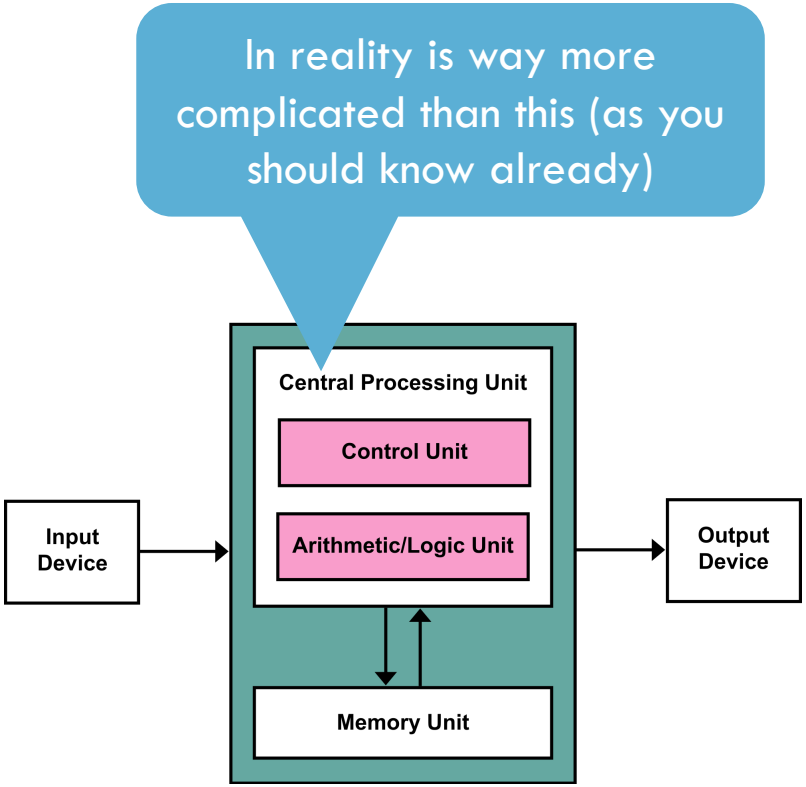

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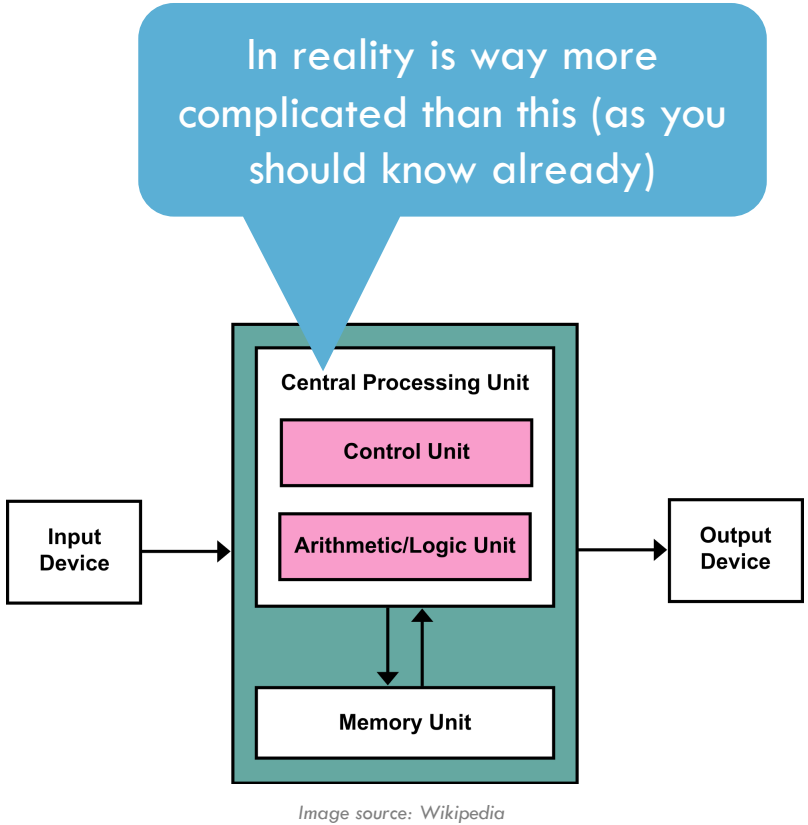
- Buses, represented with arrows, work as data/instruction carrying pathways



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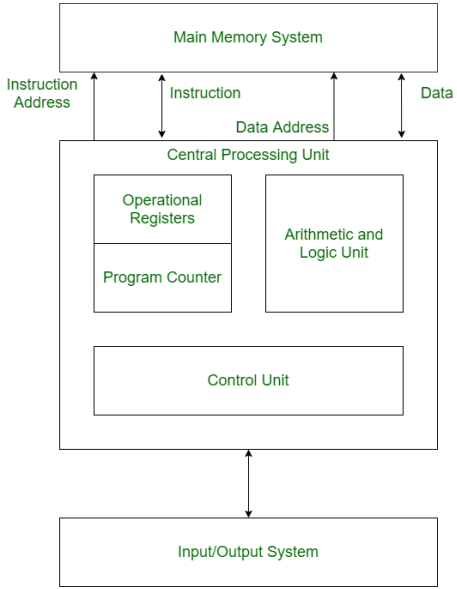
Alternative architectures

Harvard architecture

- Separates data and instruction memory and their buses
- Both can be accessed simultaneously
- Used in embedded systems and digital signal processors
- Limitations: Complexity, non-flexibility, limited code size



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Dataflow (DF) architecture

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- In DF architectures, instructions are executed in data-flow order
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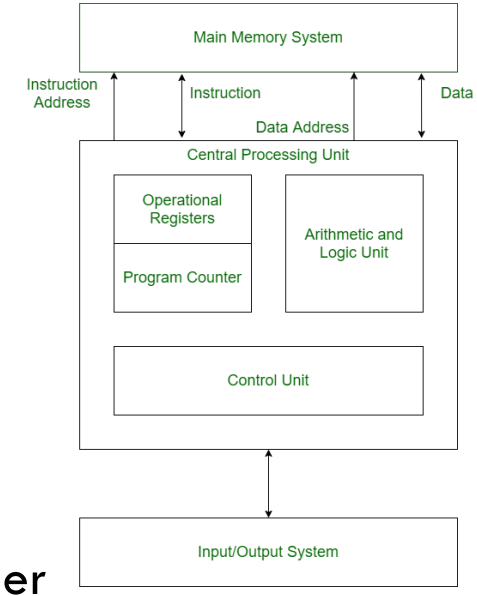
- In a DF machine, a program consists of DF nodes



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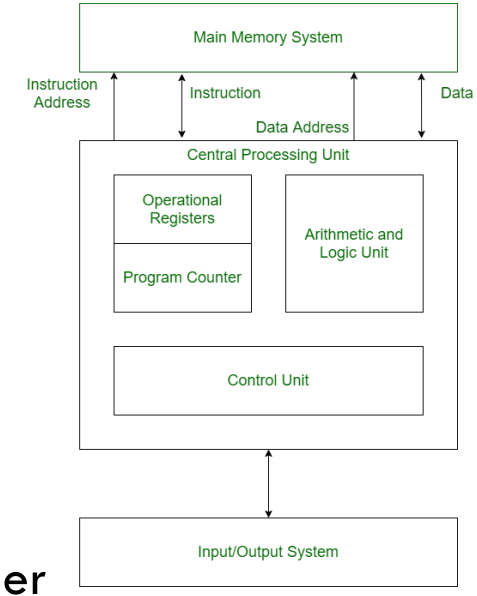

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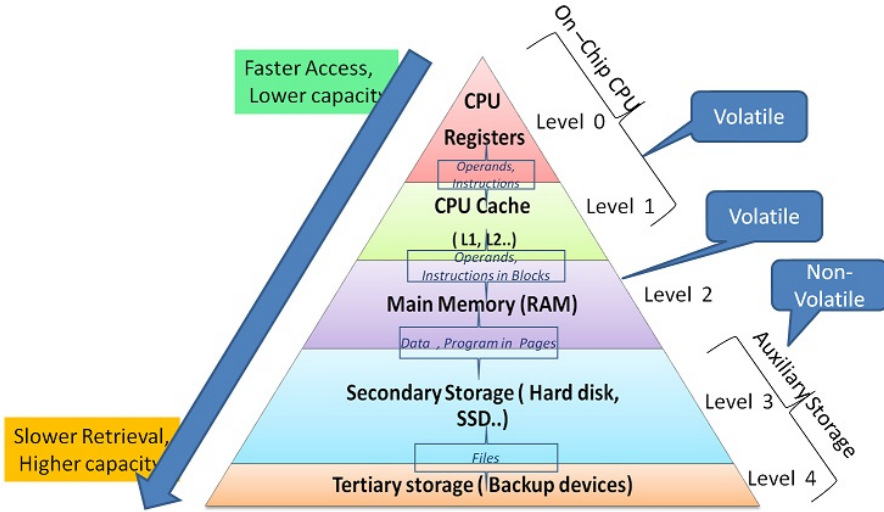
The memory hierarchy



Bill Dally, MICRO, 2019

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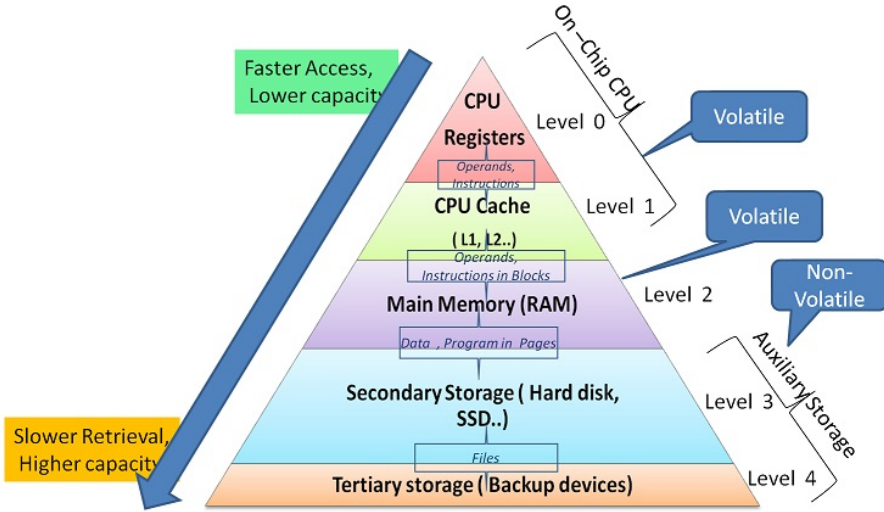

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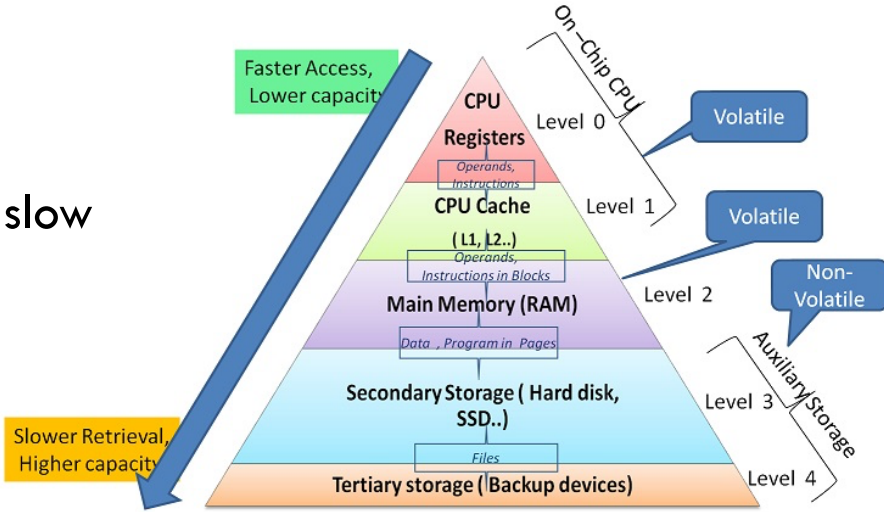

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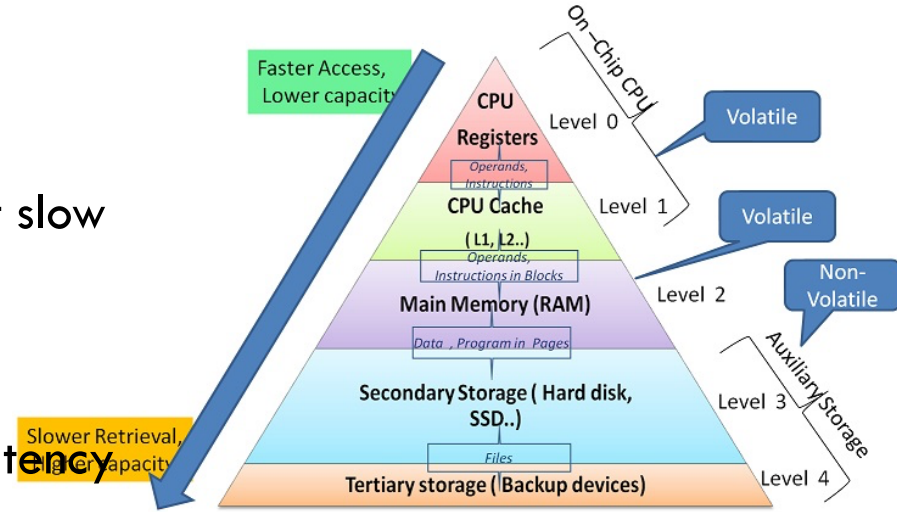

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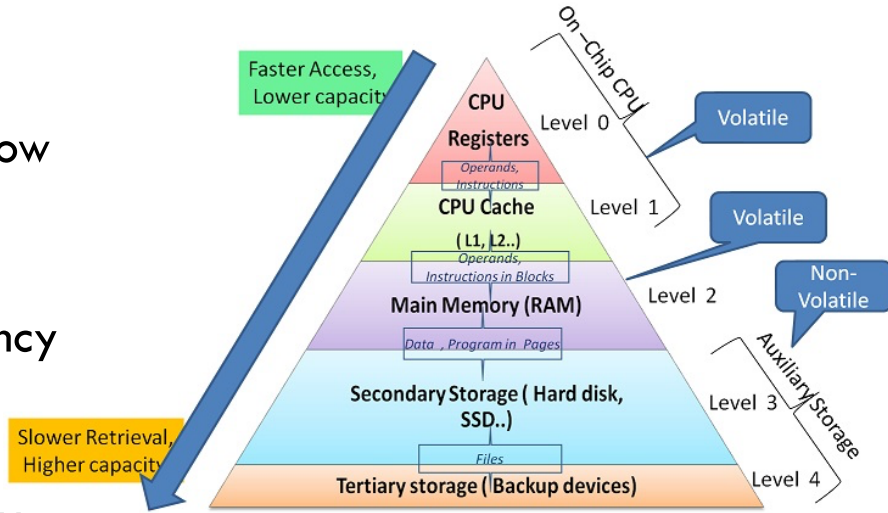
- Caches hide the main memory access latency
  - Typically in kilo/mega byte ranges
  - Access latency in nanoseconds



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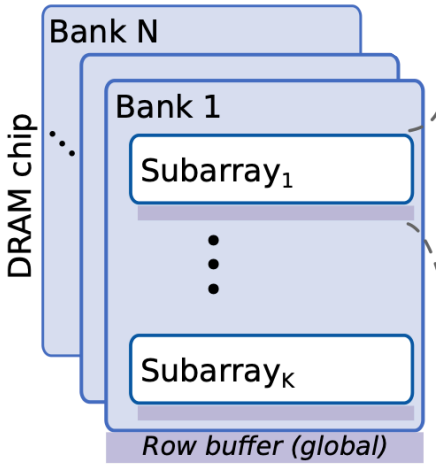
- Memory locality is the principle that consecutive memory accesses are closed to each other
  - Temporal locality: Close in time
  - Spatial locality: Close in space
- Cache contents depend on the cache structure and its management policies
  - Reading material: *Jaleel et al, Achieving Non-Inclusive Cache Performance with Inclusive Caches: Temporal Locality Aware (TLA) Cache Management Policies, MICRO 2010*

Main memory organization

- Consists of channels, ranks, and banks

- Each bank can have one or more subarrays



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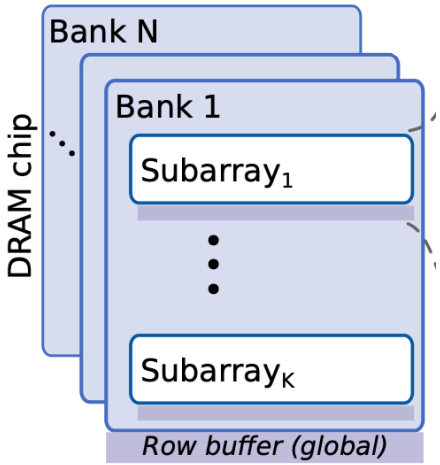

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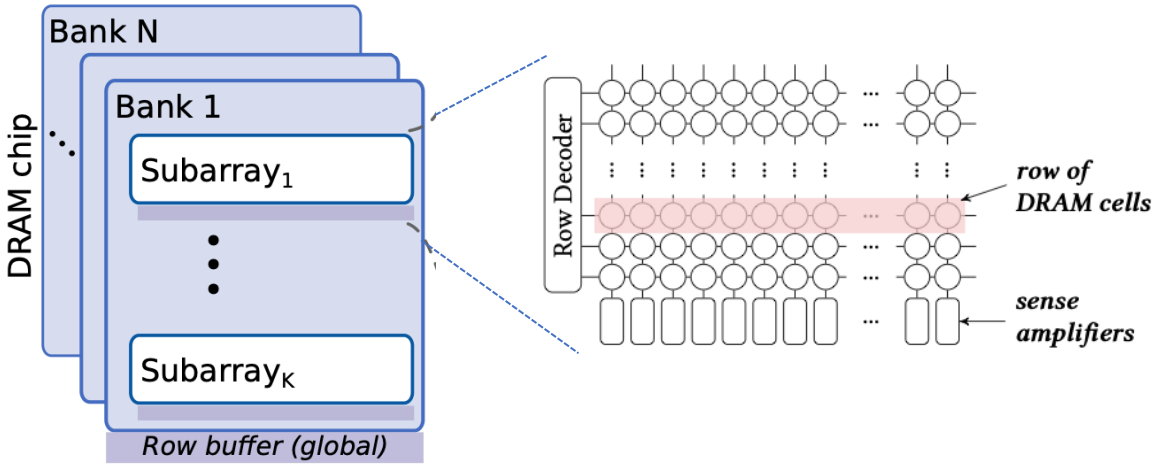

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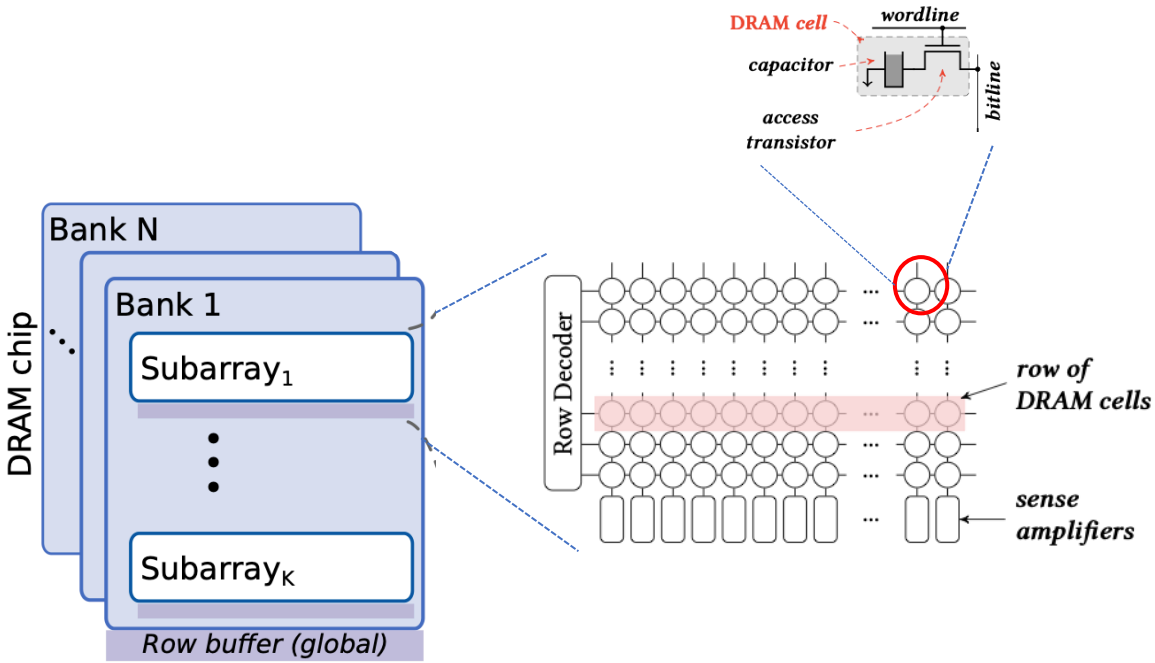
- Each row-col intersection has a memory cell



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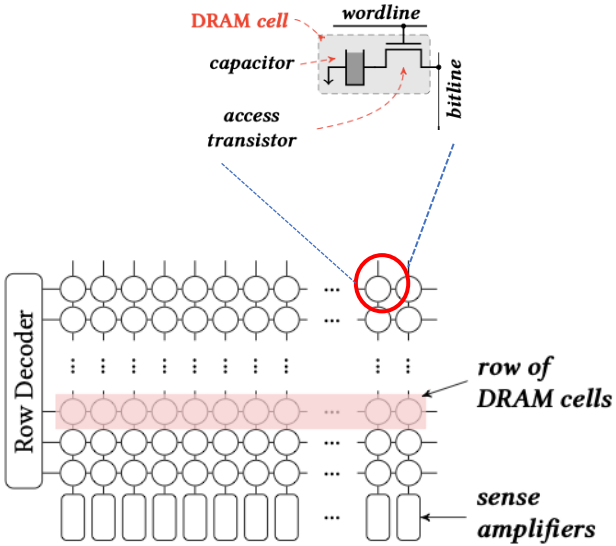

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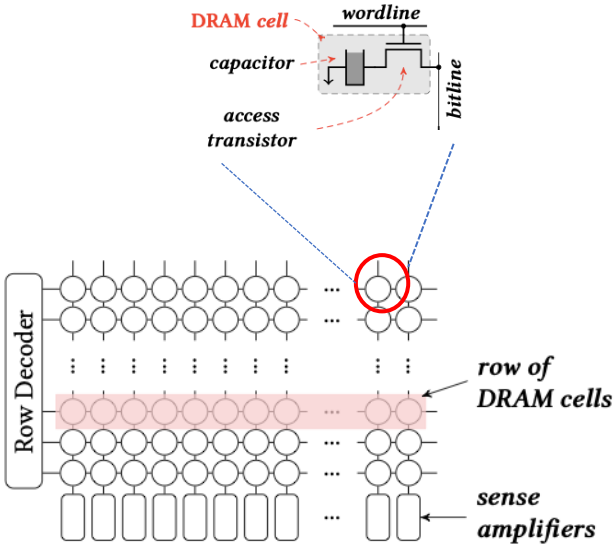

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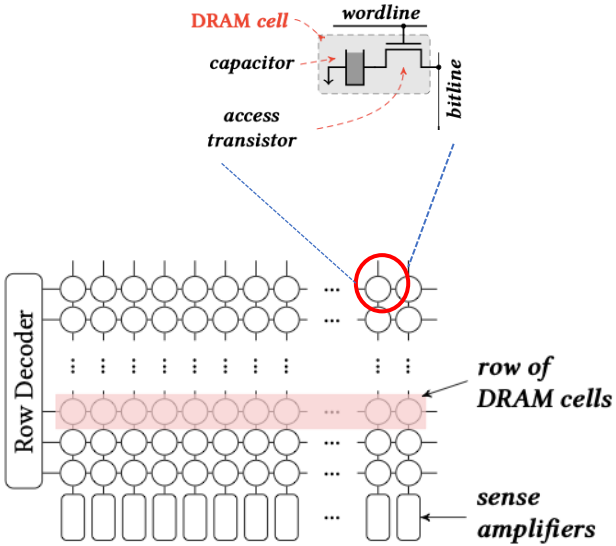
- The senseamp is also referred to as the row-buffer



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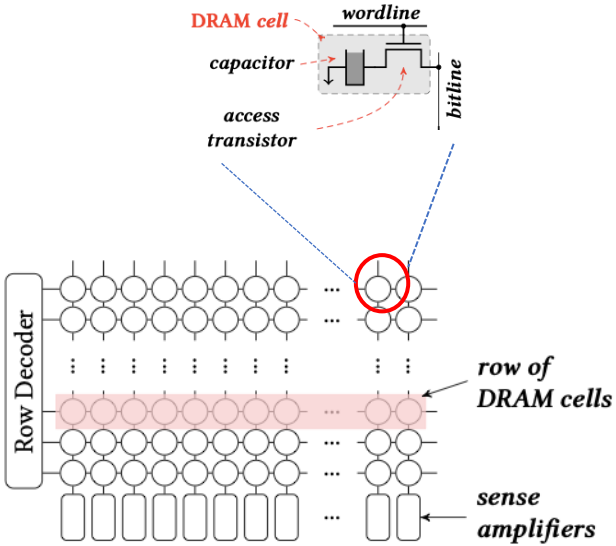

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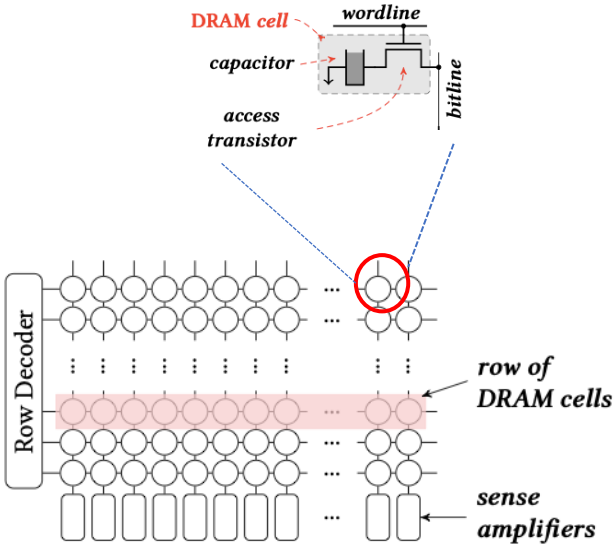

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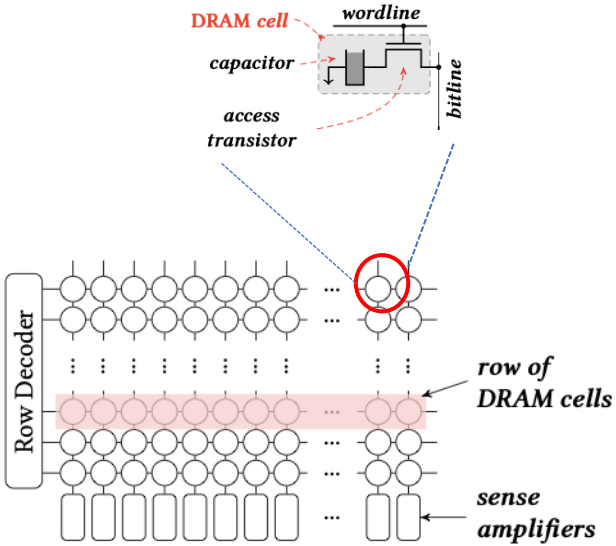

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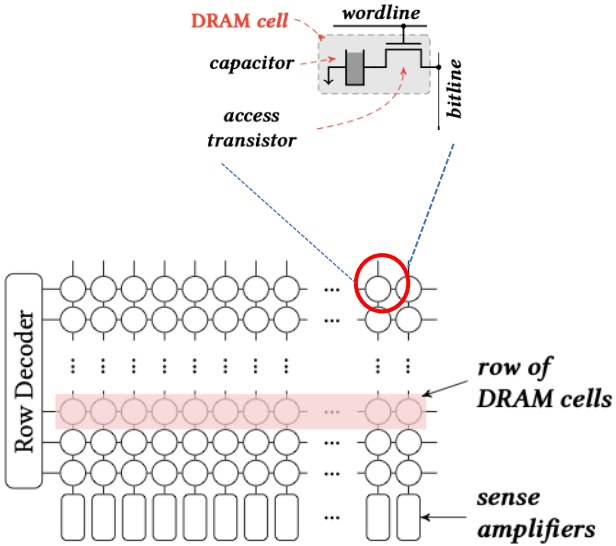
  - If the data is found, it is return to the CPU (ns range)
  - If not, it is fetched from the main memory
    - The memory controller receives the request, including request type, and address
    - The address decoder decode the address to find channel rank, bank, subarray, etc.
    - The row decoder decodes the row address
    - That row is activated, data comes to the row buffer
    - The column address decoder decodes the column address
    - Data is eventually put on the bus and the row is closed (precharged)



Reading material

- Kim et al., “A case for exploiting subarray-level parallelism (SALP) in DRAM”, ISCA 2012

- Backes et al, “The Impact of Cache Inclusion Policies on Cache Management Techniques”, Memsys 2019

- Escuin et al, “Compression-Aware and Performance-Efficient Insertion Policies for Long-Lasting Hybrid LLCs”, HPCA 2023

Thank you!

asif.ali@uetpeshawar.edu.pk