Computing in/using memory -- II

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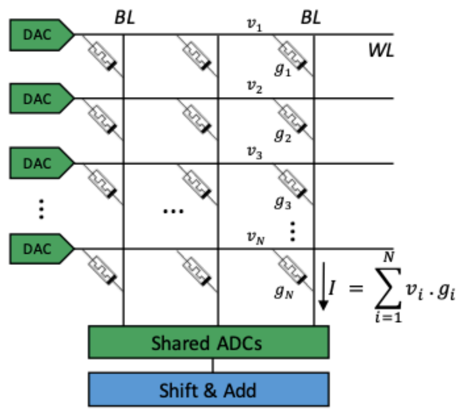
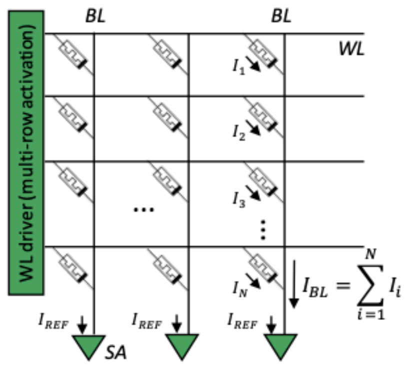
Recap: Compute-in-memory (CIM)

- ❑ The CIM paradigm aims to completely eliminate the data movement
- ❑ The fundamental idea is to exploit the physical properties of the memory devices to perform computations
- ❑ Not every computation can be performed with every technology





WL driver (multi-row activation)
BL
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I_1
I_2
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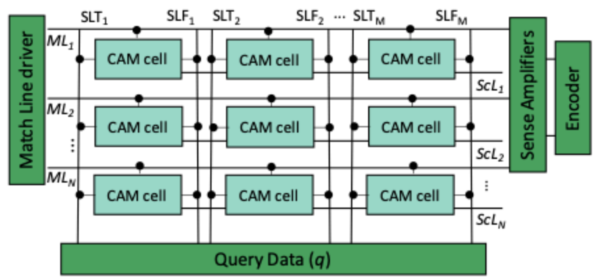
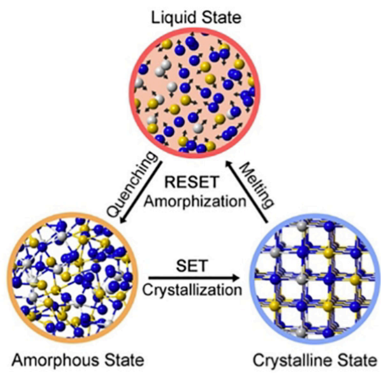
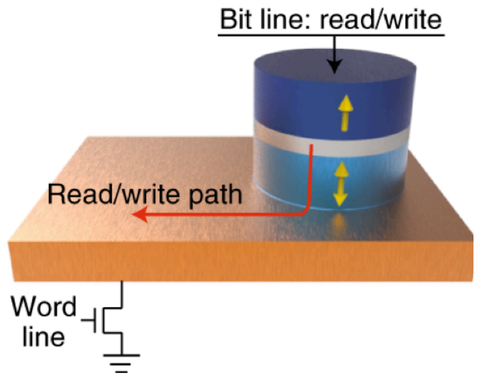
...
$I_{BL} = \sum_{i=1}^{N} I_i$
I_{REF}
SA



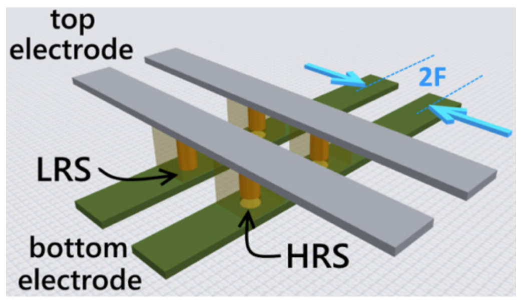
Recap: Emerging nonvolatile memories (NVMs)



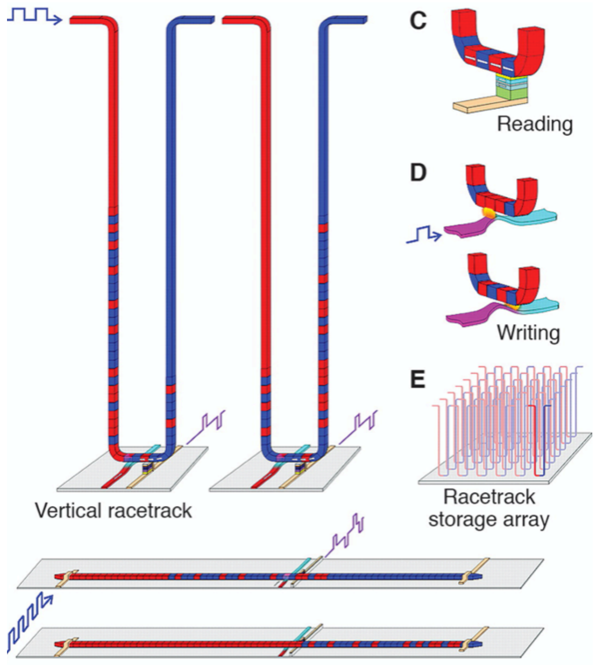
Zhang et al., 2020



G. Yu, 2020



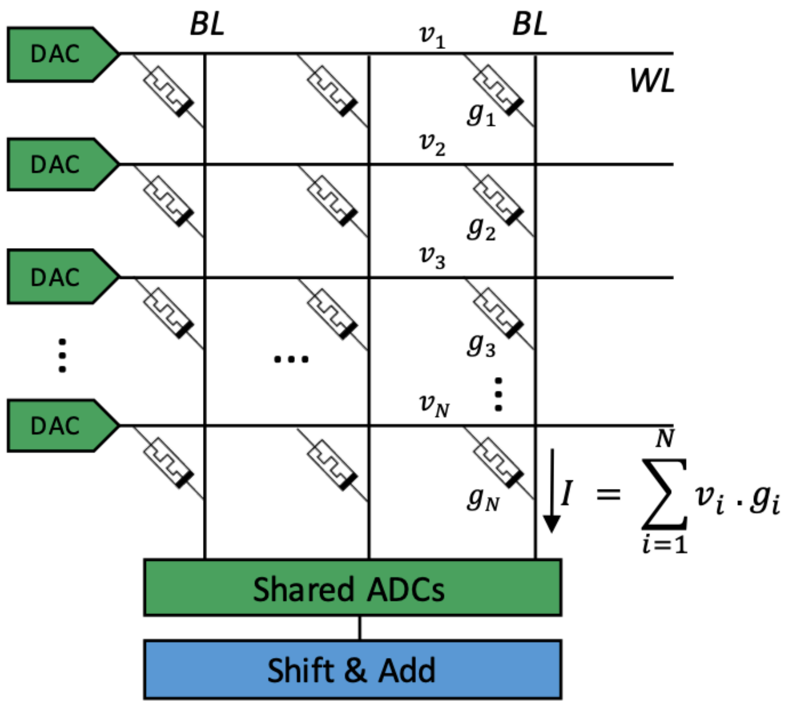
Lim et al, 2015



Parkin et al, 2008

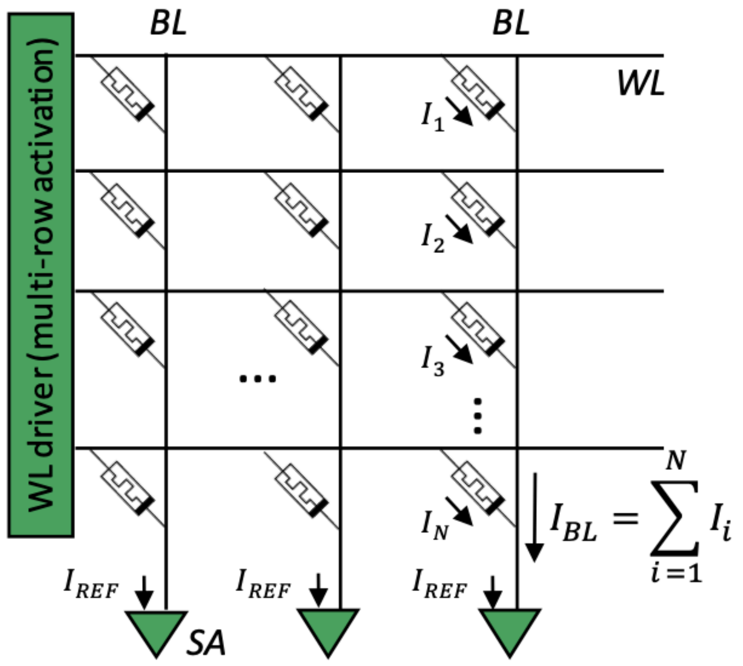
- ❑ Other options: FeFET, FeRAM etc
- ❑ Each technology has its strengths and challenges
- ❑ PCM and MRAM receive a lot of traction in industry

Recap: CIM crossbar



- ❑ Program one operand into memristors devices (conductance)
- ❑ Enable all wordlines simultaneously and apply another operand as input
- ❑ The accumulated current at the bitlines using Kirchoff's law produces the outcome of dot product
- ❑ Analog domain computation – results are approximate

CIM logic



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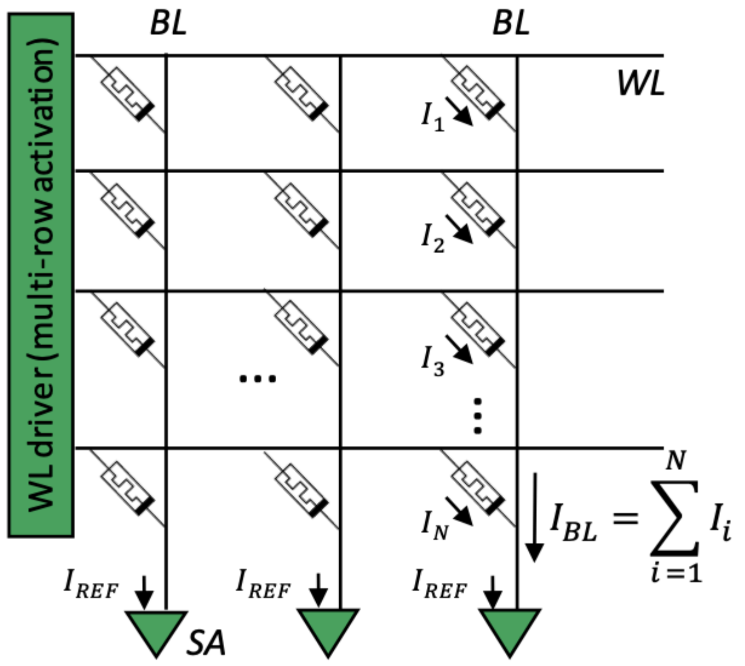

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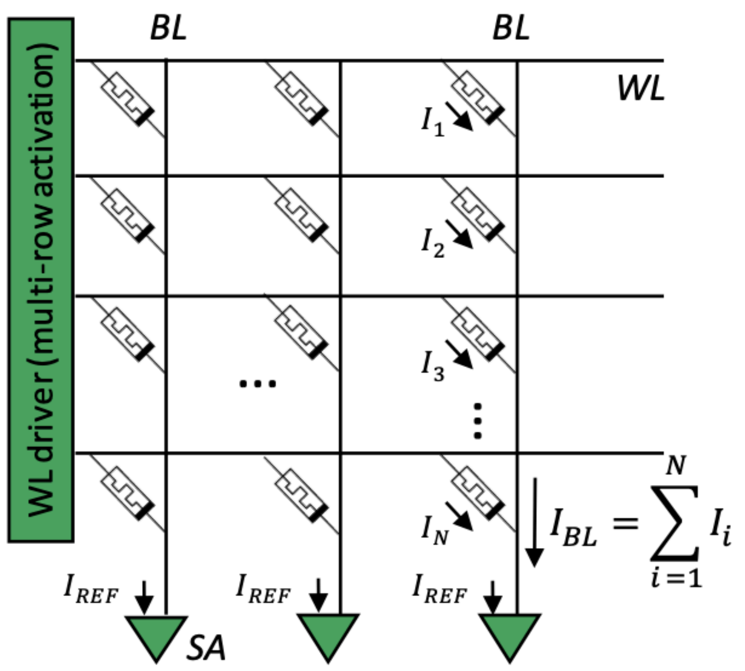
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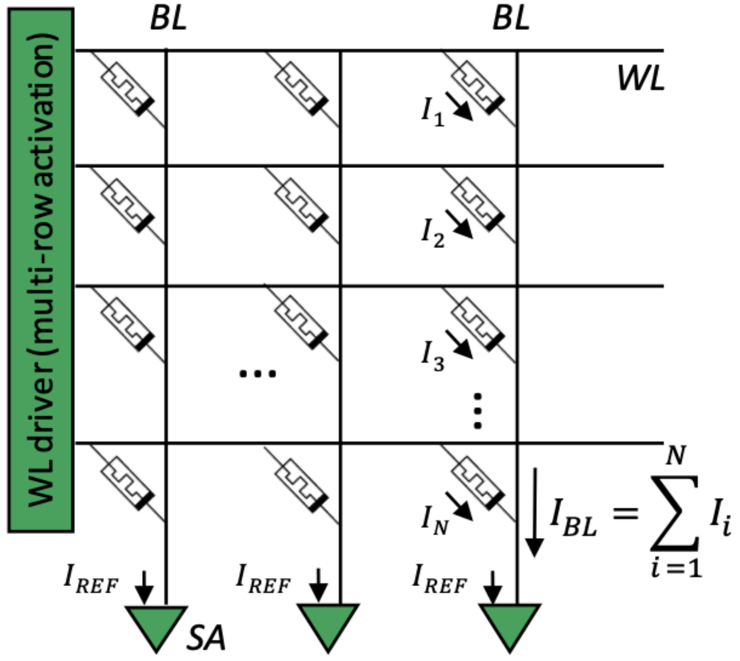
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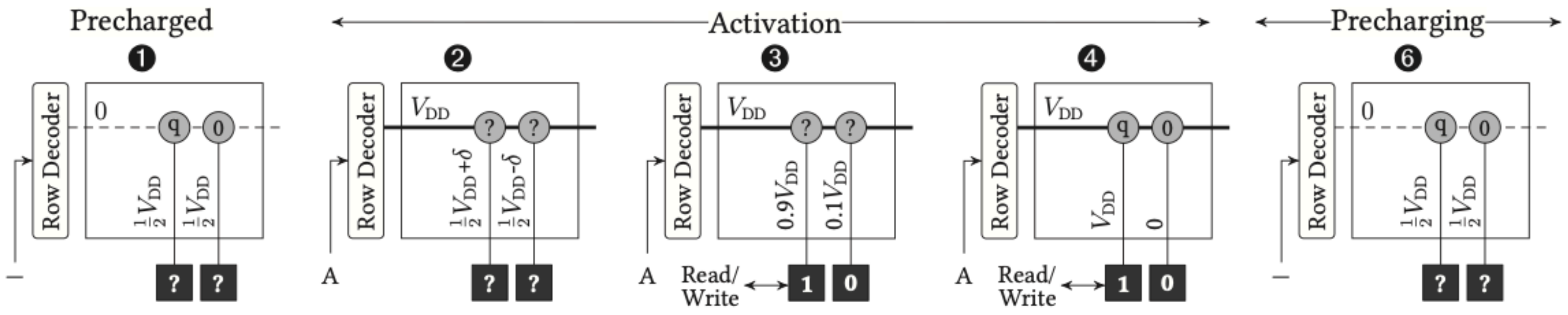
- Have applications in cryptography, databases and other domains
- The fundamental idea is still current/charge sharing
- The exact implementation depends on the specific technology

CIM-logic using DRAM



Sishadri et al., MICRO 2013

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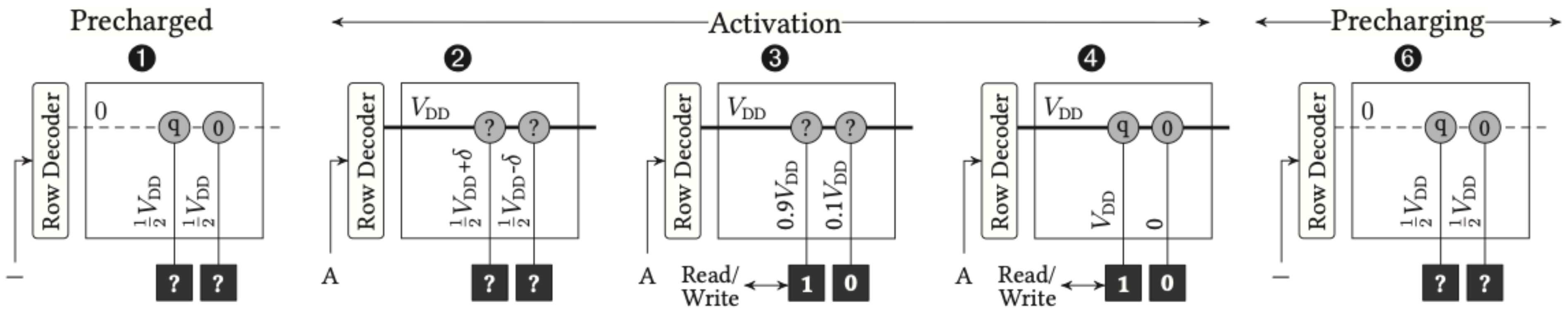

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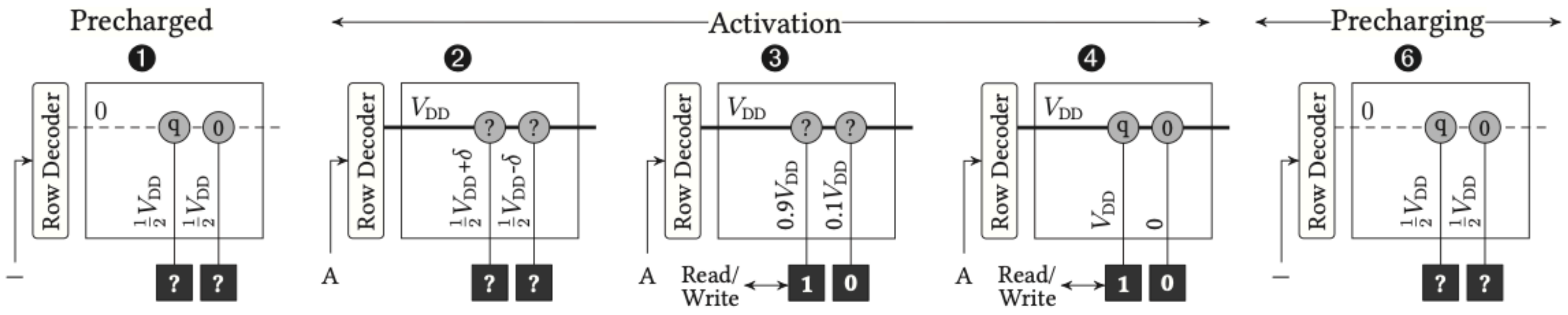

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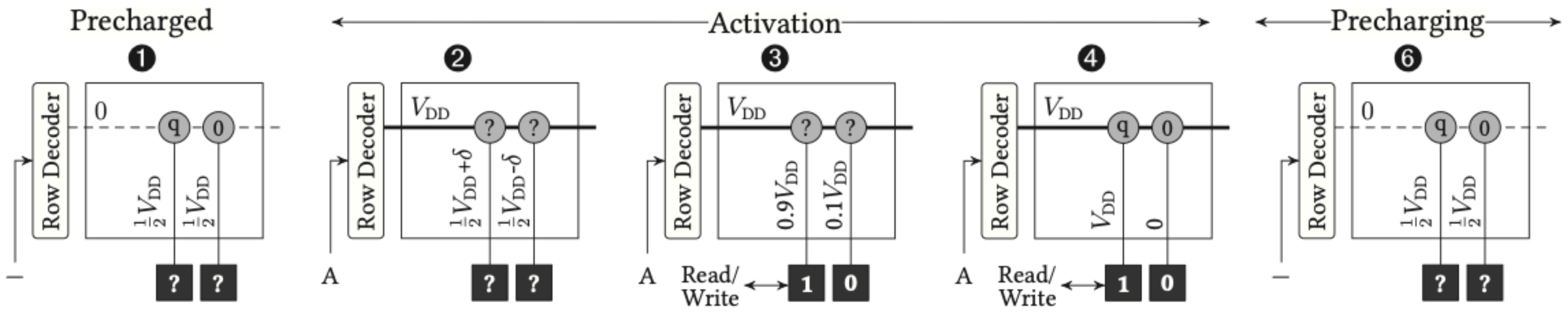
If a DRAM cell is connected to a bitline that is at a stable state (either V_{DD} or 0) instead of the equilibrium state ($\frac{1}{2}V_{DD}$), then the data in the cell is overwritten with the data (voltage level) on the bitline.

CIM-logic using DRAM



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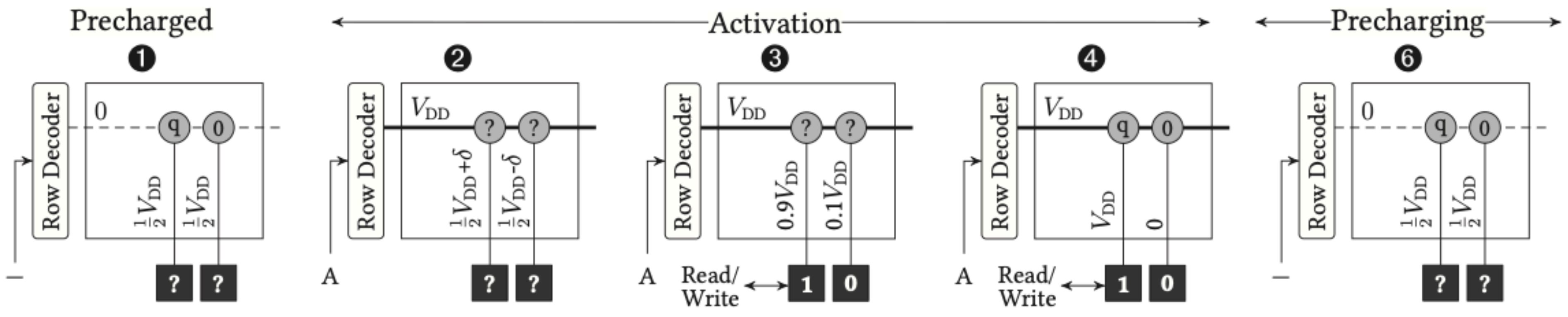

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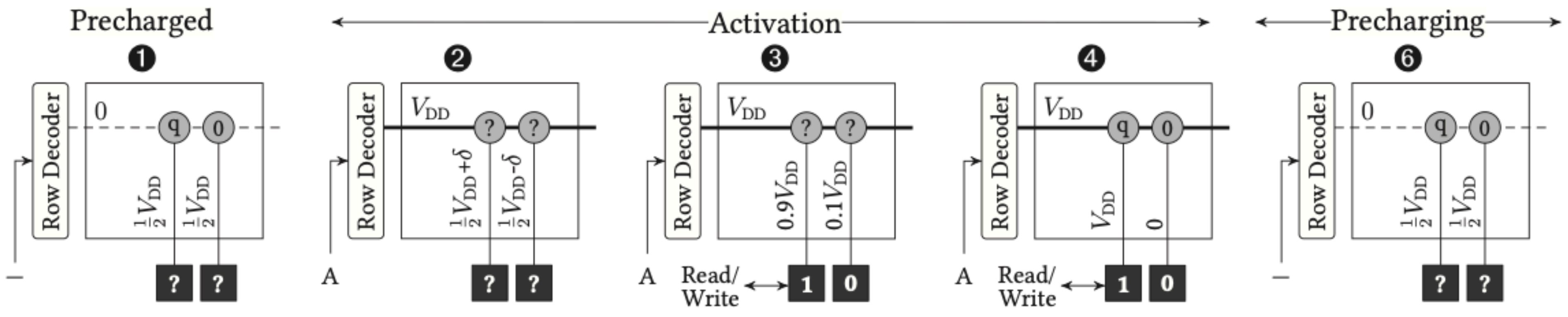

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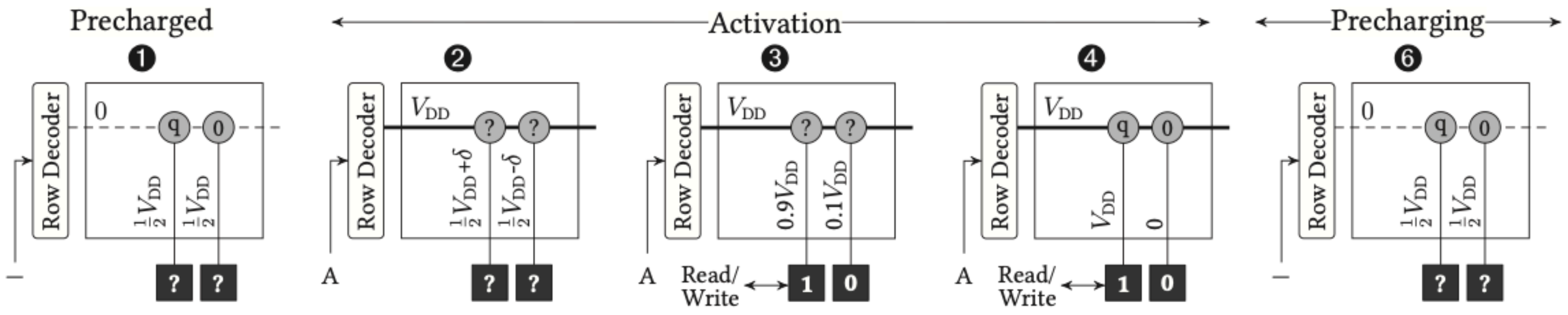

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  - A PRECHARGE command brings the bitline to the equilibrium state (VDD/2)

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  - At least two cells have to be 1, for the output to be 1
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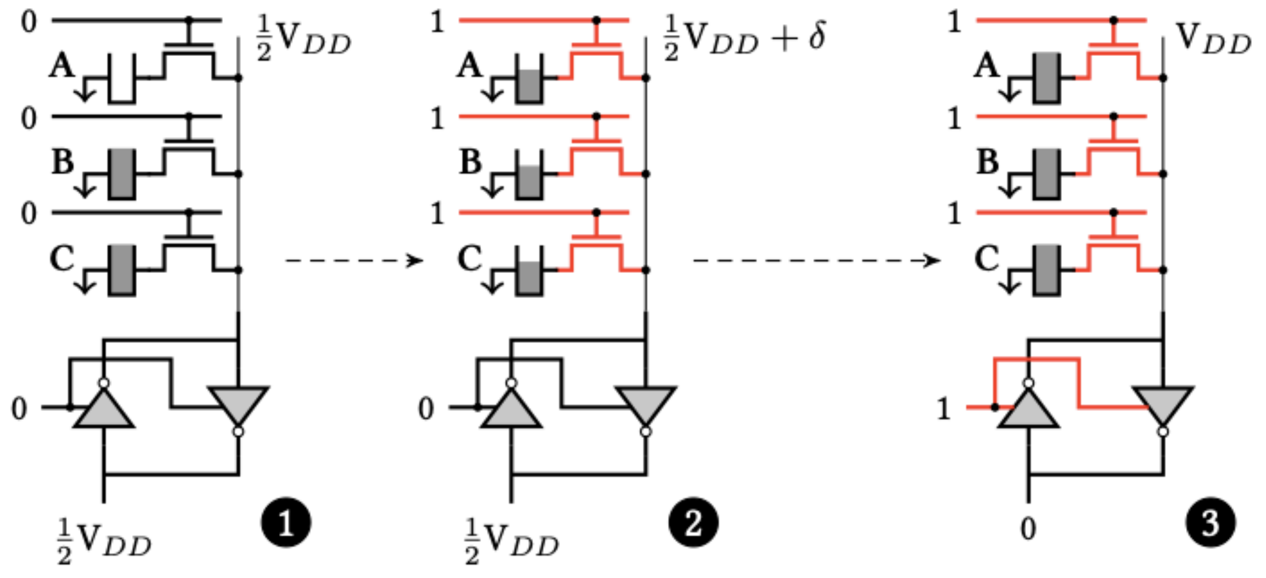

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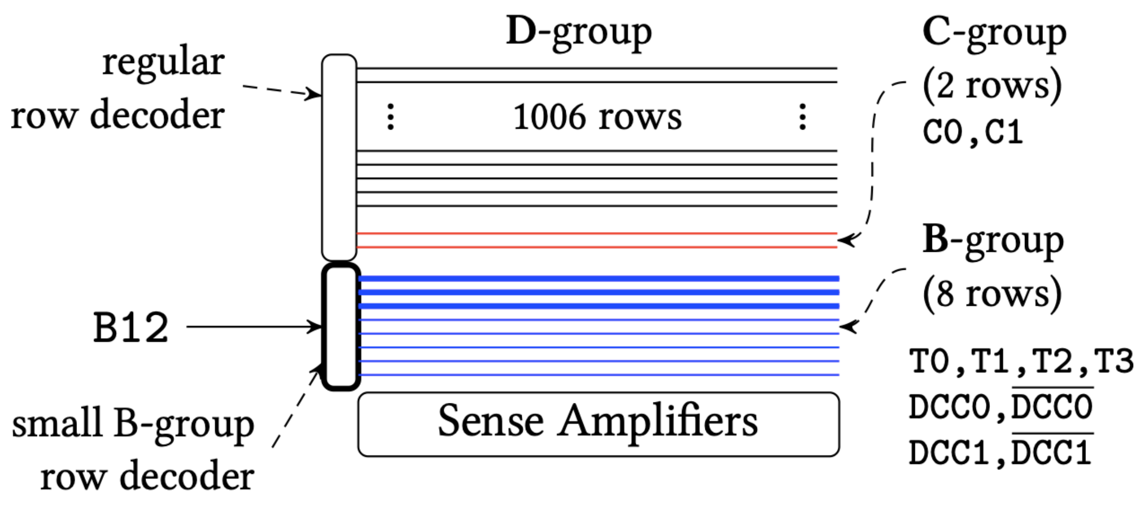
- Important: TRA destroys contents of the involved cells
  - Contents need to be copied to a different place first, if important/needed

Ambit -- CIM-logic using DRAM



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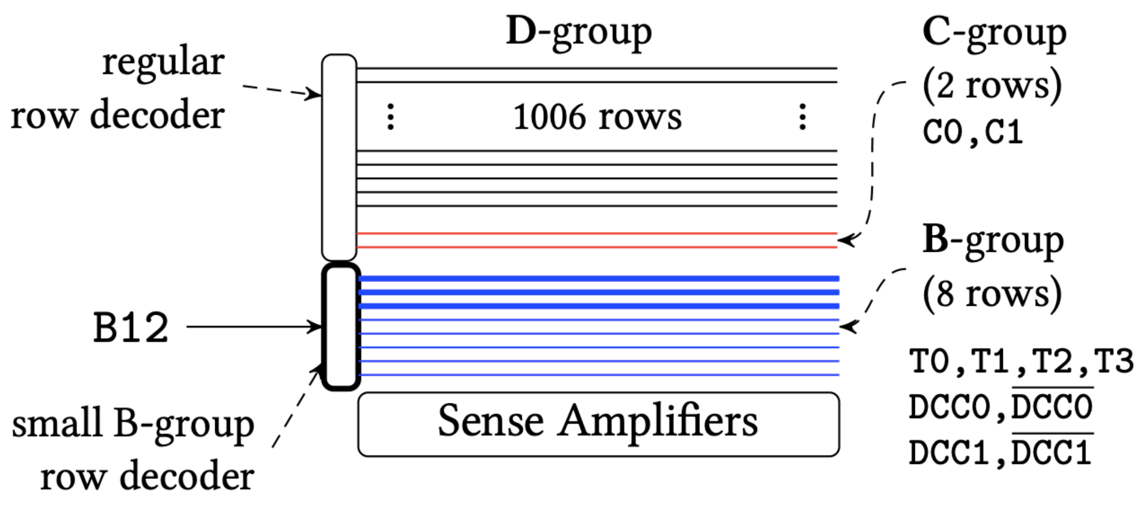

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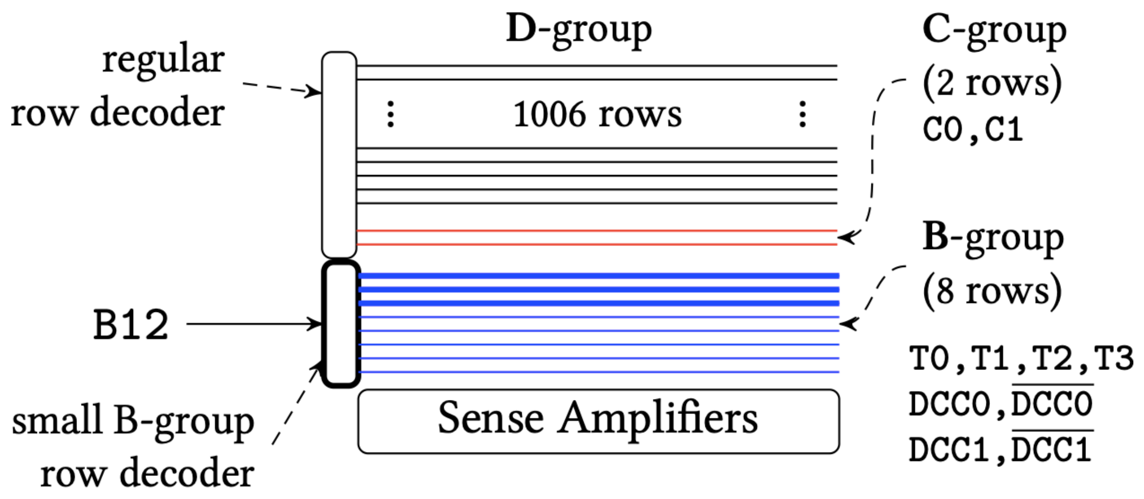

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- ❑ The two control/constants rows (C-group) have constant 0 (C0) and 1 (C1)
- ❑ Majority of the rows are data rows (D-group), as in a typical DRAM array

Ambit -- CIM-logic using DRAM

- To perform a logic AND using Ambit:
  1. Copy A to T0
  2. Copy B to T1
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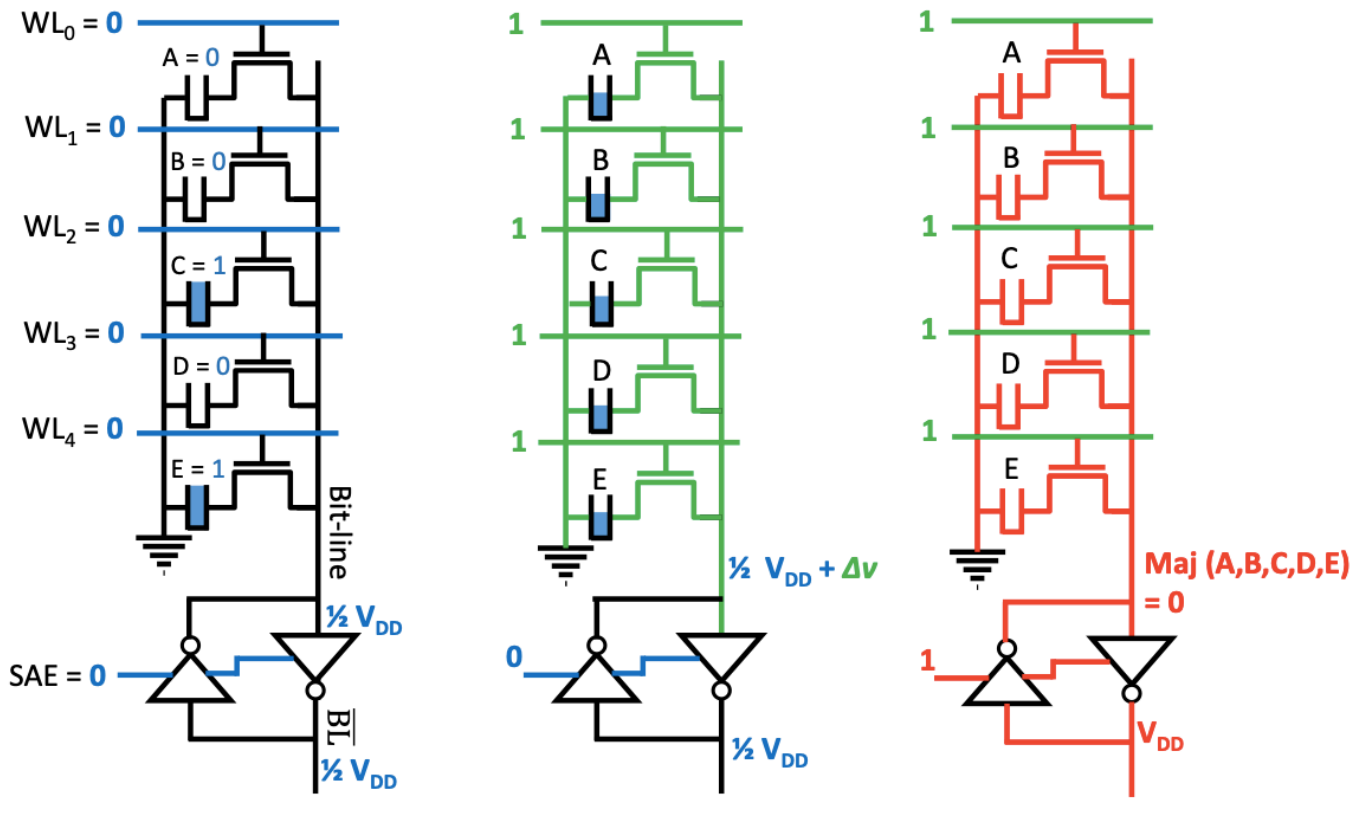
- The NOT operation is implemented using inverted bitline, and specialized DRAM cells

In-DRAM addition

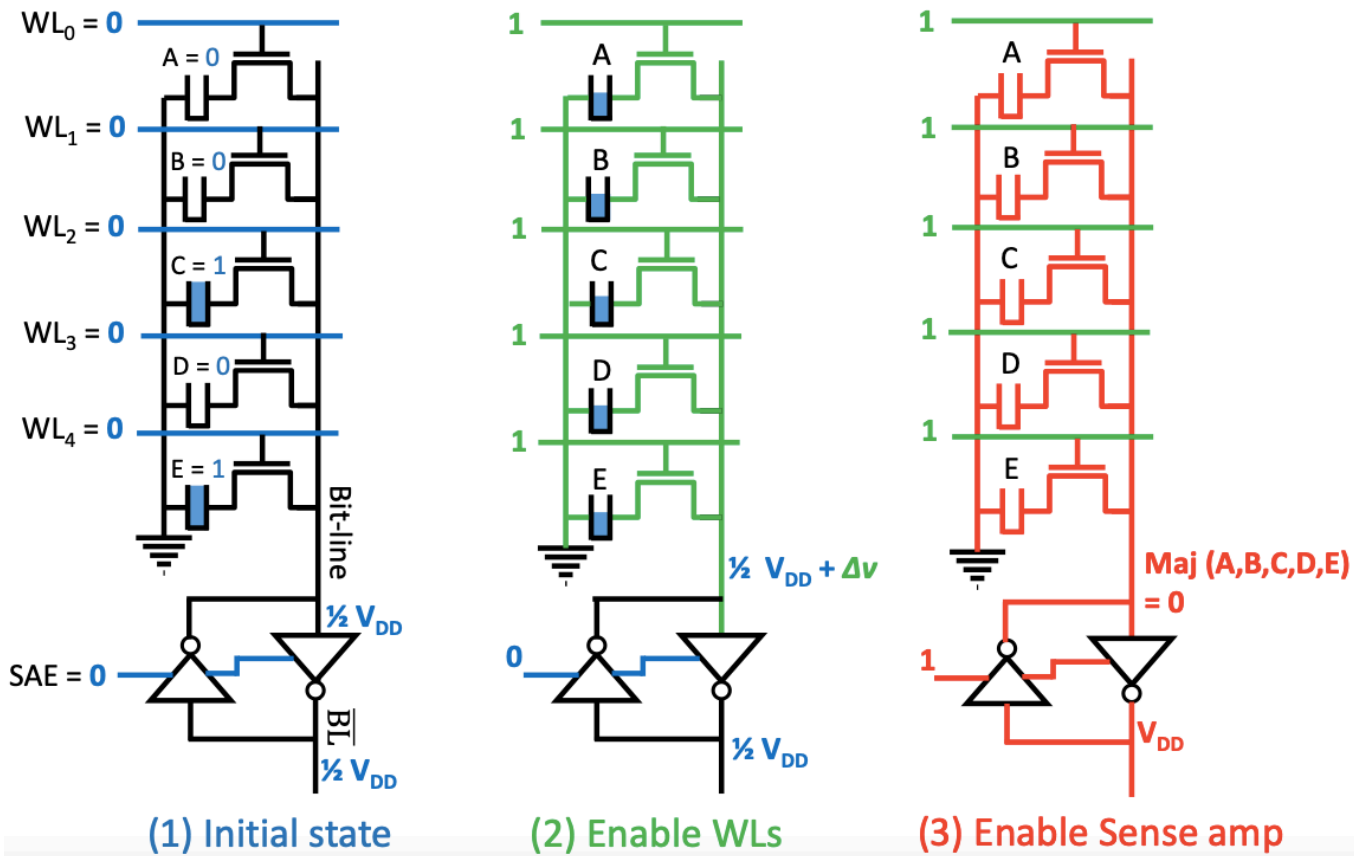


(1) Initial state (2) Enable WLs (3) Enable Sense amp

In-DRAM addition

$$Cout = Majority(A, B, Cin)$$

$$Sum = Majority(A, B, Cin, \overline{Cout}, \overline{Cout})$$



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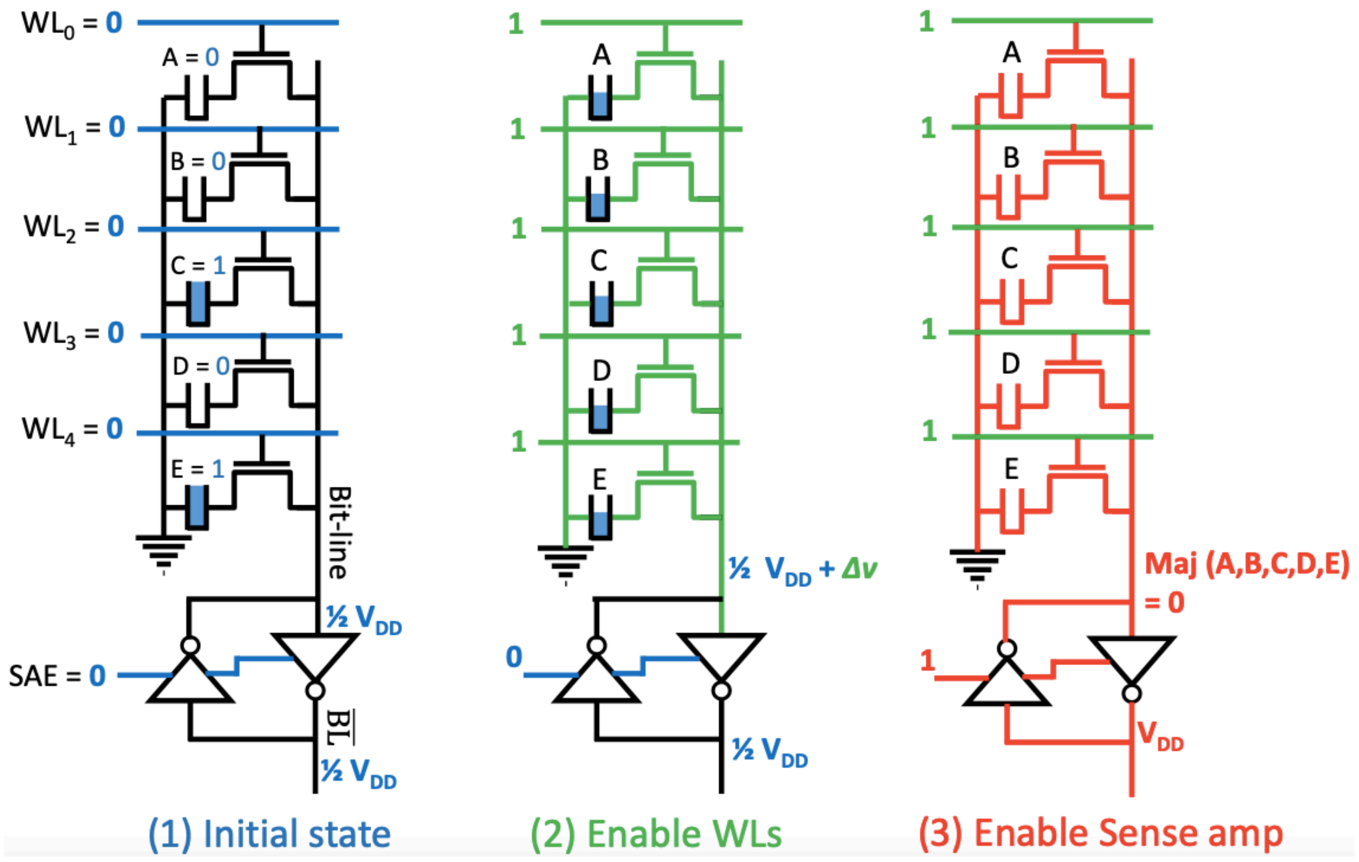

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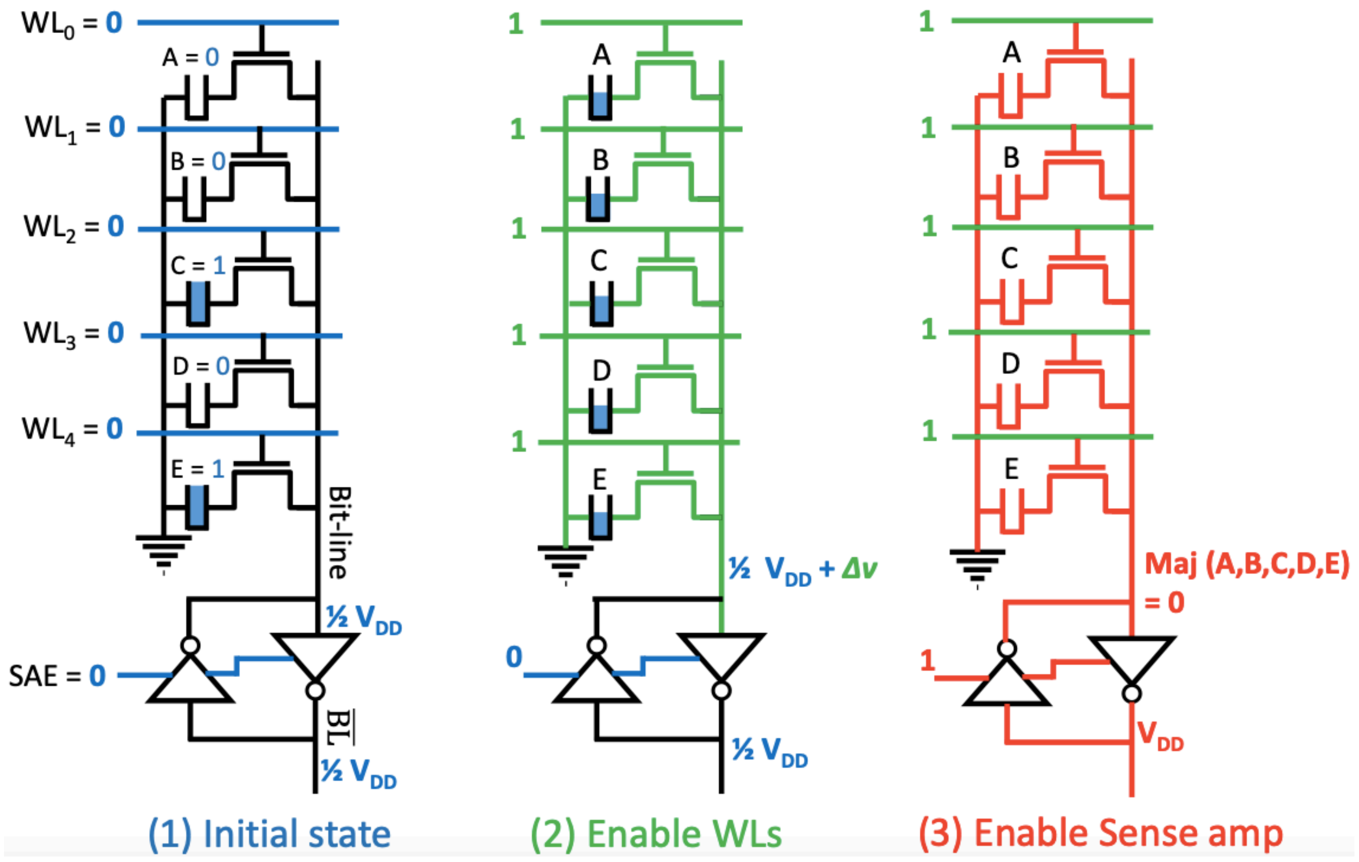

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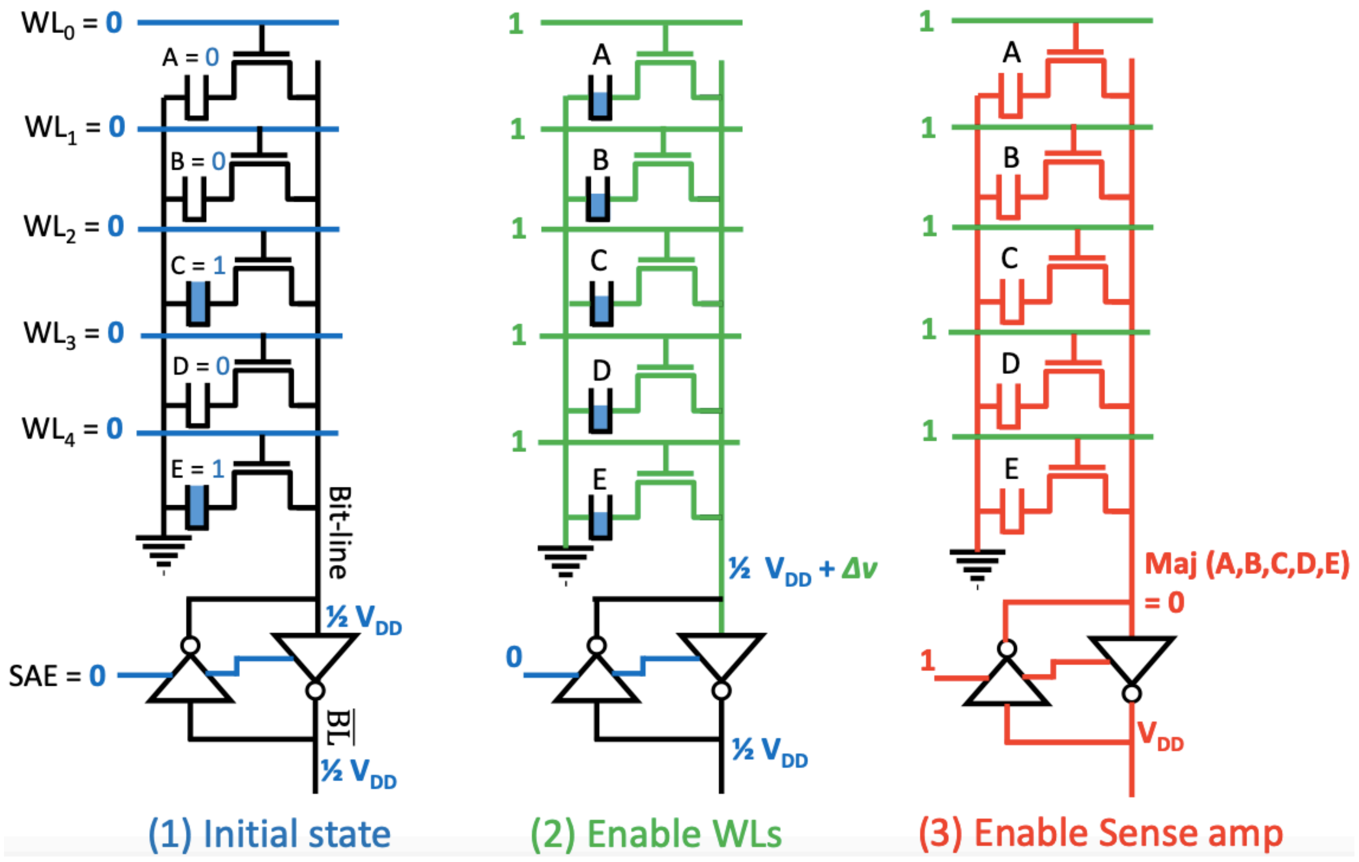
- ❑ Particularly useful for bulk additions on low-precision numbers



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$$b_i = (b_i \wedge \overline{m}) \vee (b_{i-1} \wedge m), \quad \text{where } i \in \{n, n-1, \ldots, 2\}$$

$$b_1 = (b_1 \wedge \overline{m}) \vee (\overline{b_n} \wedge m)$$

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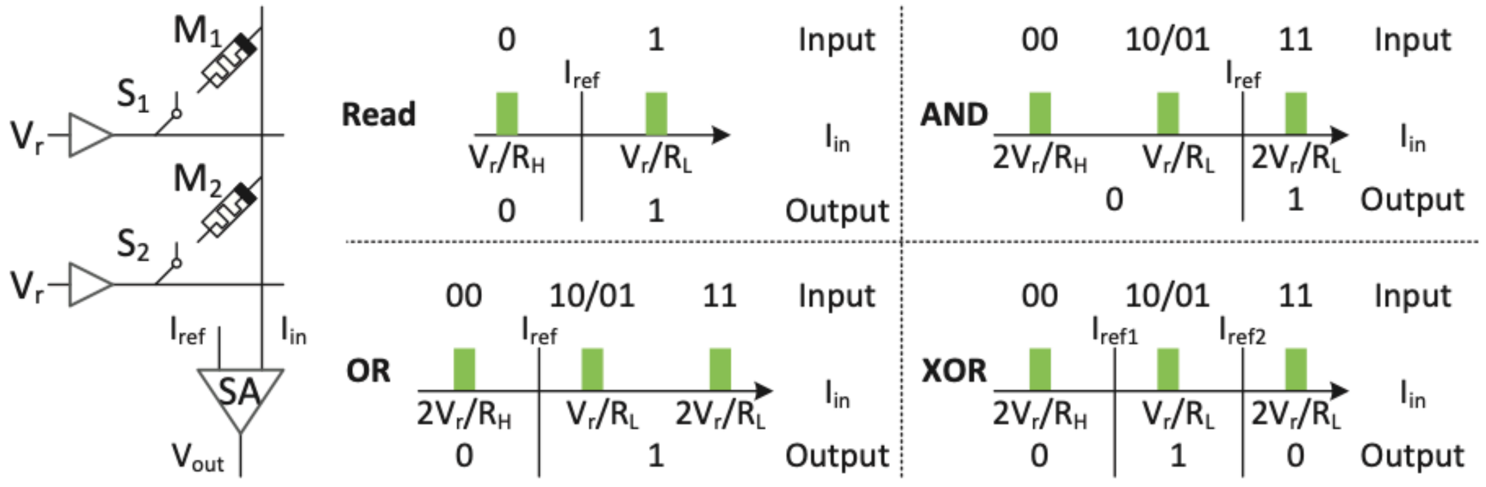

(a) Memory (b) References of Primitive Operations

Thank you!

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