



Department of Computer Systems Engineering,  
University of Engineering and Technology Peshawar,  
Pakistan

Final term Exam (Fall 2018)

Time: 2 Hours

Paper: CSE-304 Computer Organization and Architecture

Marks: 50

Note: Attempt all questions on answer sheet. Be precise and do your best!

**✓ Question No. 1 (Marks=10):**

- i. What are the parts of an instruction? Briefly explain it with examples.
- ii. Implement the following equation using 0-Address format instructions (using mnemonics)?  
 $16+20+24+28-32$

**✓ Question No. 2 (Marks=10)**

- i. If the size of the program counter is 16 bits, what can be the maximum size of the memory in computer architecture provided the data width is 8 bits?
- ii. What flags represent in computer architecture? Explain at least four flags briefly with examples?  
*O, sign, parity, carry*

**✓ Question No. 3 (Marks=10)**

- i. How the carry bit act as an extension to the arithmetic and logic unit (ALU)? Explain briefly with examples?
- ii. What is the difference between displacement, relative, base-register and index addressing schemes? Explain briefly with examples?

**✓ Question No. 4 (Marks=10) (CLO-1; C2-Comprehension; PLO1-Engineering Knowledge)**

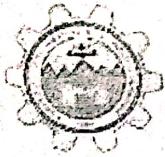
You have to design an instructions set architecture (ISA), whose characteristics are;

- ✓ 16 different operations (ADD, SUB, OUT, HLT etc.)
- ✓ 12-bit address (program counter (PC), a memory address register (MAR) etc.)
- ✓ 16-bit data registers (accumulators, B, Temp etc.)
- ✓ 16-bit instruction register (IR)
- i. What will be the instruction size?
- ii. Opcode size?
- iii. Operand size?
- iv. A number of locations in memory?
- v. Memory data size?

**✓ Question No. 5 (Marks=10) (CLO-2; C2-Comprehension; PLO1-Engineering Knowledge)**

- i. How scoreboard algorithm resolves the structural, data and control hazards? Explain it with the four cycles of the algorithm.
- ii. What is the difference between;
  - Read after write hazard
  - Write after write hazard
  - Write after read hazardExplain it with examples?

assign out = \$2? (S1? (S0? I<sub>7</sub> : I<sub>6</sub>) : (S0? I<sub>5</sub> : I<sub>4</sub>)) :



Department of Computer Systems Engineering,  
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Midterm Exam (Spring 2019)

Time: 2 Hours

Paper: CSE-308 Digital System Design

Marks: 25

Note: Attempt all questions on answer sheet.

Question No. 1 (Marks=15) (CLO-1):

- ✓ I. Write a Verilog statement for 8x1 multiplexer using a conditional operator.
- II. Briefly explain how a wand differs from wor.

- ✓ III. Convert the following behavioral code to explicit structural code.

```
module btos(x, a, b);
    input a, b;
    output x;
    wire a, b;
    reg x;
    always @ (a or b) if(a) x = b; else x = ~b;
endmodule
```

(data flow level)

always @ (a or b)  
if(a)  
x = b;  
else  
x = ~b;

assign x = (a || b) ? b : ~b;

- ✓ IV. How to declare a Verilog constant? Give examples.

- ✓ V. Give the result of each Verilog expression (in binary) for the following inputs: A=4'b0011, B=3'b011 and C=3'b101. Assume A is a 4-bit wire and B and C are each 3-bit wires. Show your results using Verilog notation, such as 3'b101.

- a. A + (B | C); \_\_\_\_\_
- b. ~& A; \_\_\_\_\_
- c. (A == B) ? B : C; \_\_\_\_\_
- d. {A, {2{C}}}; \_\_\_\_\_

- ✓ VI. Write Verilog statement that declares an 8-bit register, myReg, and initially assigns it the hexadecimal value 29.

- ✓ VII. Write a Verilog statement that declares 8192 x 16-bit memory (myMem).

- ✓ VIII. What is the difference between the design module and the test bench module?

- ✓ IX. Write a Verilog design module for 3 x 8 decoder using behavioural level modelling.

- X. What is the difference between blocking and non-blocking statement? Give examples.

- ✓ XI. Write Verilog code for D flip flop having set and reset ports. The D flip flop should trigger on the negative edge of the clock.

- ✓ XII. What is the difference between positional association and explicit association in specifying ports connectivity? Give examples.

- ✓ XIII. What is the difference between relational operators and bitwise operators in Verilog? Give examples.

- ✓ XIV. Draw the logic circuit diagram that is described by the Verilog code.

```
module M(Q, S, A, B, C);
    output Q;
    input S, A, B, C;
    reg Q;
    always @(posedge C)
        Q <= (S) ? A : B;
endmodule
```

- ✓ XV. What is the difference between initial and always block in Verilog? Give examples.

011  
101  
|||  
011  
1010  
0011  
A = 1100  
0000

A = 0011  
B = 011  
C = 101

001 A + (111)

B | C  
0 11  
1 01  
-----  
1 11

**Question No. 2 (Marks=5)      Required**

Write the Verilog code for a 4-bit adder/subtractor. An adder/subtractor is a piece of hardware that can give the result of addition or subtraction of the two numbers based on a control signal. Assume that the numbers are in 2's complement notation. Please keep in mind that this is a combinatorial circuit. Also, write a test bench module for the design.

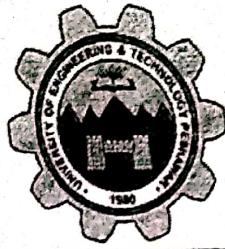
**Question No. 3 (Marks=5) (CLO-3)**

In this module, design a 3-bit gray counter with positive reset. When reset, the count value becomes "000". Recall that a gray counter changes only one bit at a time. For example, a 2-bit gray counter has a count sequence 00, 01, 11, 10 corresponding to decimal count values of 0, 1, 2, and 3 respectively. In the gray count sequence, only one-bit changes between adjacent count values, and the right-most bit is changed as long as it does not result in a code word that has been visited earlier. Also, write a test bench module for the design.

The following are the ports of the module:

CLK	1-bit clock input, all actions must be on the positive edge
RESET	1-bit reset, causes reset on the positive edge
GRAY_OUT	3-bit result

gray  
0, 1, 3, 2, 6, 7, 5, 4, 1



Department of Computer Systems Engineering  
University of Engineering & Technology  
Peshawar, PAKISTAN

Subject: Digital Signal Processing (5<sup>th</sup> Semester)

Exam: Mid Term (Fall 2018)

Max Marks: 25

Attempt All Questions.

Time allowed : **2 hours**

✓ **Question 1:**

- ✓ 1) What are the steps involved in converting an analog signal into digital signal? Explain each step and how the error in these steps can be avoided or reduced? (3 Marks)
- 2) What is power and energy signals? Are finite duration signals power signals or energy signals? What about infinite duration signals? (1+1 Marks)
- 3) Given the discrete time signal  $x(n)$  shown in Figure 1, find and sketch the even and odd parts of the signal  $x(n-2)$ . (3 Marks)

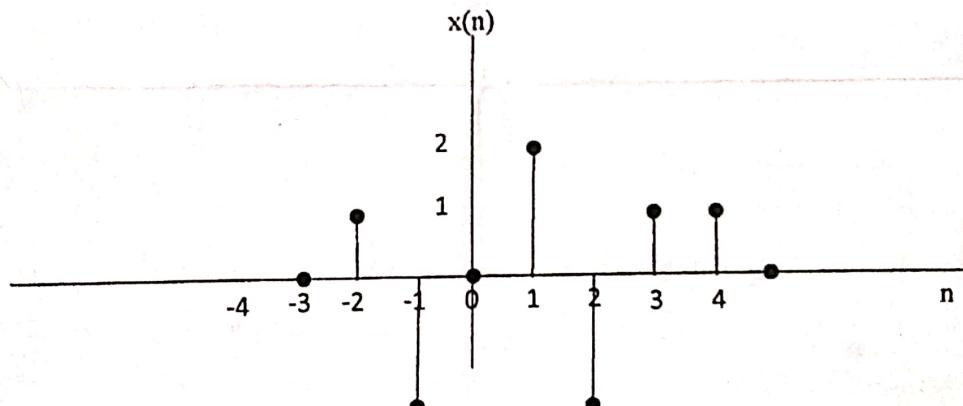


Figure 1

✓ **Question 2:**

- ✓ 1) Find the convolution of  $x[n]$  and  $h[n]$  given below, (2+2+1 Marks)
- Analytically
  - Graphically

$$h[n] = 2\delta(n+1) - \delta(n) + 2\delta(n-1)$$

1/2

P.T.O

$$x[n] = \begin{cases} 1, & n = 0, 2 \\ 2, & n = 1, 3 \\ 0, & \text{otherwise} \end{cases}$$

Is the system given by  $h[n]$  a stable system? Is  $h[n]$  a causal or non-causal system?

- ✓ 2) Find the overall impulse response  $h[n]$  of the interconnection of systems shown in Figure 2, bellow. (3+1 Mark)

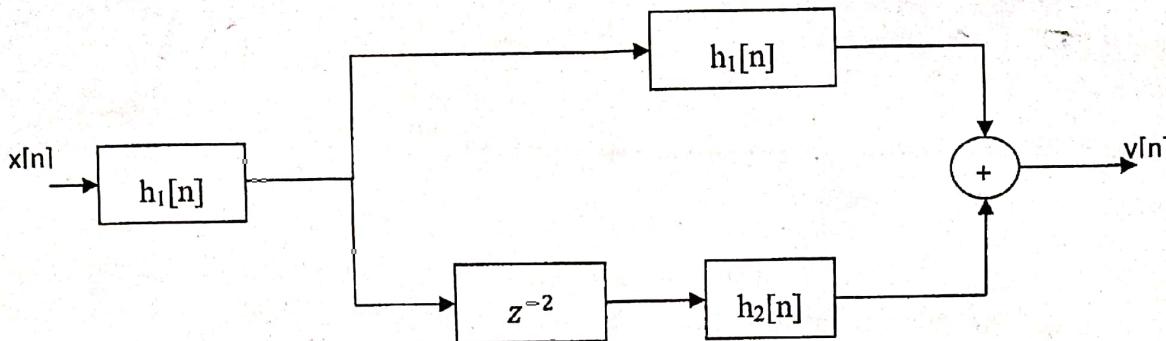


Figure 2

Where,

$$h_1[n] = 1\delta(n) - 2\delta(n-1) + 1\delta(n-2)$$

$$h_2[n] = 2\delta(n+1) - \delta(n) + 2\delta(n-1)$$

Are systems  $h_1[n]$  and  $h_2[n]$  causal systems? What about the equivalent system  $h[n]$ ?

### Question 3:

- ✓ 1) Draw the Direct Form 1 and Direct Form 2 structure for the LTI System described by the following difference equation. (2 Mark)

$$2y[n] - 5y[n-1] - 4y[n-2] = 3x[n] + 2x[n-1]$$

- ✓ 2) Find the homogeneous solution of the system given by the following difference equation with given initial condition. (2 Mark)

$$y[n] - 3y[n-1] - 4y[n-2] = x[n] + 2x[n-1]$$

$$y[0] = 1, \quad y[1] = 5$$

- ✓ 3) Find the z-transform of the following signals using the properties of z-transform. State clearly the property used in each step. (4 Marks)

$$x_1[n] = \left(\frac{1}{2}\right)^n [u(n) - u(n-5)]$$

$$x_2[n] = n \left(\frac{1}{3}\right)^{n-1} [u(n-1) - u(n-5)]$$



Department of Computer Systems Engineering  
University of Engineering & Technology  
Peshawar, PAKISTAN

Subject: Signal and Systems (4<sup>th</sup> Semester)

Exam: Mid Term (Spring 2018)

Max Marks: 25

Attempt All Questions.

Time allowed

**2 hours**

**✓ Question 1:**

- 1) What are the three main differences between continuous-time and discrete-time sinusoidal on the basis of periodicity? Are the following sinusoidal signals periodic? If yes, find their time period and if no, state the reason. (CLO1) (5 Marks)
- a)  $x(t) = 5 \cos(300\pi t + \frac{\pi}{6})$   
b)  $x(t) = 2 \cos(200t + \frac{\pi}{8})$   
c)  $x[n] = \cos(150\pi n + \frac{\pi}{4})$   
d)  $x[n] = 3 \cos(100n + \frac{\pi}{3})$
- 2) For the signals  $x(t)$  and  $x[n]$  given in Figure 1 below, find; (CLO1) (4 Marks)

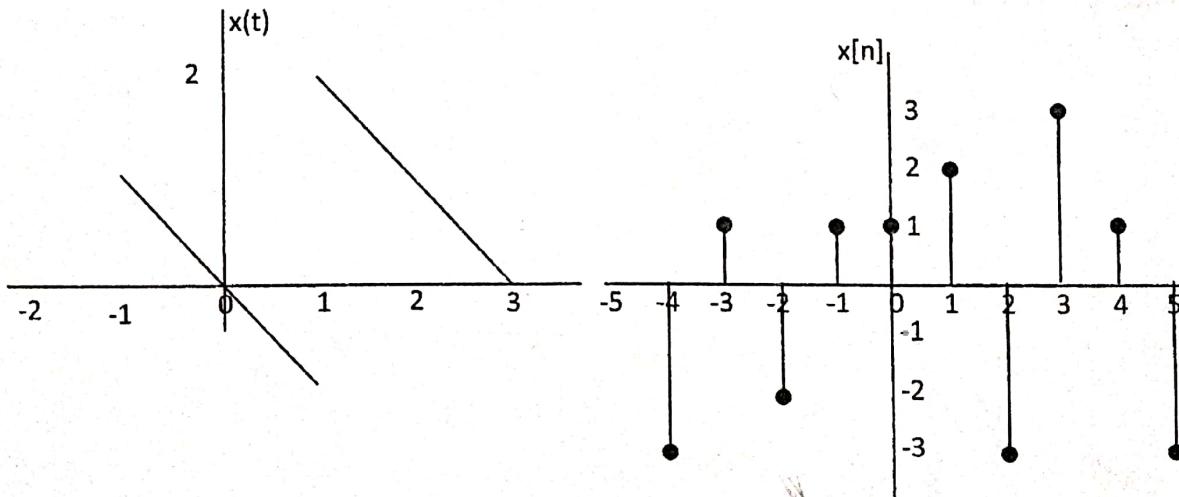


Figure 1

- ✓a)  $x(2t - 1)$   
✓b)  $-2x(-2t + 3)$   
✓c)  $x[2n - 2]$   
✓d)  $x[-\frac{1}{2}n + 1]$

(P.T.O)

**Question 2:**

- 1) What is impulse response of a system? How the impulse response  $h[n]$  of an LTI system can be used to find the response  $y[n]$  for any arbitrary signal  $x[n]$  (Hint: express  $x[n]$  in terms of  $x[k]\delta(n - k)$ ). How  $h[n]$  of LTI system can be used to find if the system is (i) with or without memory, (ii) causal or non-causal, (iii) stable or unstable? (0.5+2+1.5 Marks)

- ✓ 2) Use the convolution sum to find the response  $y[n]$  of the LTI system with impulse response  $h[n]$  to the input  $x[n]$ , given in Figure 2. Also sketch your results. (CLO2) (3+1 Marks)

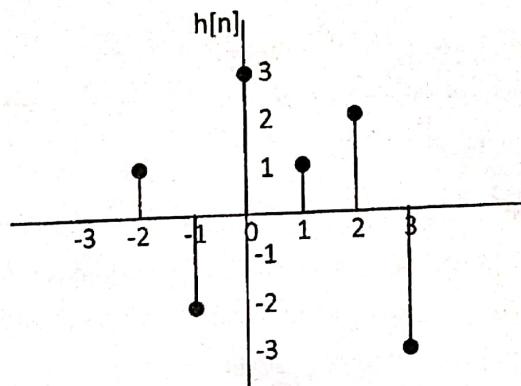
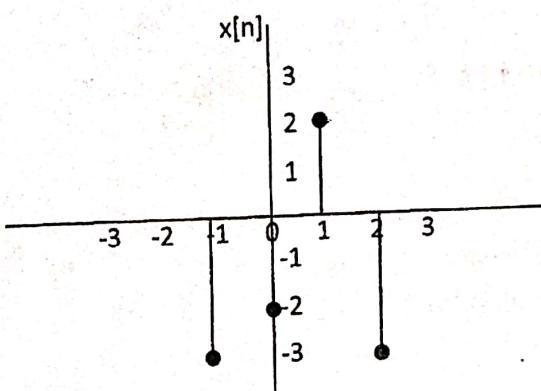


Figure 2

Also find if the system given by  $h[n]$  is stable or unstable.

✓ **Question 3:**

- ✓ 1) Using convolution integral, find the response  $y(t)$  of the LTI system with impulse response  $h(t)$  when the input signal  $x(t)$  is passed through it. Also sketch the resultant signal  $y(t)$ . (CLO2) (5 Marks)

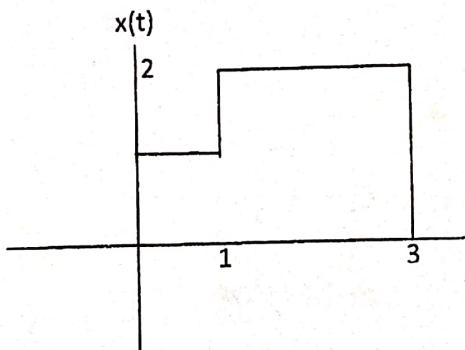
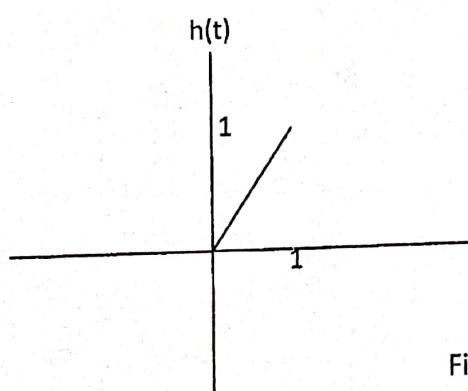


Figure 3

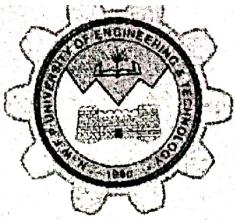
- ✓ 2) Find the response  $y(t)$  when signal  $x(t)$  is passed through the LTI system described by the following difference equations. (CLO2) (3 Marks)

$$\frac{dy(t)}{dt} + 3y(t) = 2x(t)$$

Where,  $y(0) = 3$  and  $x(t) = e^{2t}u(t)$

2 | Page

$$\begin{aligned} \frac{1}{2} (2)(8) \\ \frac{2 \times 1}{2 + 1} = 2 \cdot (2) - (\frac{1}{2})(1)(1) \\ 2 - \frac{1}{2} = \cancel{2} + \frac{1}{2} \end{aligned}$$



Department of Computer Systems Engineering  
University of Engineering & Technology  
Peshawar, Pakistan

Dated: January 11, 2019

Subject:	Engineering Economics
Exam:	Final Term
Weightage:	50 %
Time Allowed:	2 Hrs (Part A: 30 minutes, Part B: 1 hour and 30 minutes)

**Part B [Marks 60]**

**Read the following instructions:**

1. Be clear and precise in your answers. Do NOT include unnecessary details.
2. You are expected to have brought calculator and necessary stationary only, anything else found in possession would be tantamount to cheating. No sharing of calculators is allowed during exam.
3. Consider 1dollar = 130 Rupees wherever required. Draw cash flows wherever required.
4. Pages are numbered from 5 of 8 to 8 of 8. Make sure you have all of them
5. You can use the interest table attached for help in some questions; still you have to write the formula used for getting the factor value.

**Question 01 [Marks 10]**

[CLO-3]

✓ Mrs. Akhtar is planning to place her savings earned by selling her jewelry in a bank account. She earns an amount of Rs. 19,69,000 from the sale. She has to choose among four different offers provided by the saving institutions i.e. nominal interest rates of **6.35% compounded annually**, **6.45% compounded quarterly**, **6.55% compounded monthly**, **6.325% compounded daily** and **6.255% compounded continuously**. She wishes to select the savings institution that will give her the highest return on this money. Which option should she select and why?

**Question 02 [Marks 10]**

[CLO-2]

✓ Pakistan International Airways has recently conducted a survey on its services and revenues. The surveys show that there was revenue of Rs. 1,460,000 the first three years since 2001 and it reduced with constant rate of Rs. 135,000 every year for next 12 years (i.e 2015). PIA wants to calculate what cumulative sum would be equivalent to these revenues in 2000 if the budget had an interest rate of 9% compounded annually.

**Question 03 [Marks 15]**

[CLO-2]

✓ Microsoft lends \$10,000,000 for small projects in rural areas of India. The loan has to be refunded at **8% interest rate compounded annually**. Repayment should be made in such a way that an amount **A must be paid for the first 8 years**, amount **3A for next 5 years** and amount **5A for remaining years**, keeping the interest rate **8%**. Total time period for which the loan is allotted is **20 years**. What sum of annuities still remains to be paid just after the **12<sup>th</sup> payment is made**? (Hint: Take \$10,000 equivalent to the present worth of all these annuities)

✓ **Question 04 [Marks 10]**

[CLO-3]

Mr. Cod is opening its restaurant near cantt area. It is expecting initial revenue of \$72,000 per year with an annual increase of about \$400 as per statistics. The initial investment required for the restaurant is \$170,000 and MARR per year is 8%. The yearly expenses are expected to reach around \$35,000. Find out if this income is large enough to cover the investment for a study period of 15 years.

✓ **Question 05 [Marks 15]**

[CLO-3]

Nike is constructing a mall near industrial estate. The initial investment includes land costs \$400,000, working capital \$560,000, building costs \$600,000 and other materials required costs \$250,000. It is expected that the sales of the mall will reach up to \$750,000 per year for 12 years at which time the land can be sold for \$500,000, the building for \$350,000, the materials for \$50,000 and all the working capital will be recovered (Hint: Salvage values). The annual expenses for labor and other items will sum up to \$475,000 per year. If the company requires an MARR of 9% on return, determine if it should invest in this mall? Use AW method to support your argument.

Good Luck

$$\left\{ \begin{array}{l} CR = 20.8127 \\ E = 475000 \\ R = 750000 \\ \text{put in} \\ CR = R - E - CR \\ \downarrow \\ \text{you w/o get answer} \end{array} \right.$$



**Maximum Time Allowed: 2 Hours**

**Maximum Weightage: 50%**

- Be precise and concise in your answers. Attempt all questions on the answer sheet.
- Please indent and comment your code properly. Un-indented/commented code will not be checked
- All questions carry equal points

✓ **Q1. Please check the following statements and fix if you see issues. If no issue, say the statement is correct.**

- ✓ i) All signals can be ignored using the signal handler routines.
- ✓ ii) Pipes performs interprocess communication through sockets.
- ✓ iii) A virtual time (ITIMER\_VIRTUAL) when it expires generate SIGALRM signal.
- ✓ iv) TCB is stored in Operating System memory area and is shared by all threads.
- ✓ v) Threads belonging to the same process share the stack memory, but not the heap memory.

✓ **Q2. Write method signatures for the following system calls. Method signatures include function name, list of parameters and return type.**

e.g. int read (int fd, char \* buf, int size);

- ✓ i) times()
- ✓ ii) gettimeofday()
- ✓ iii) sigaction()
- ✓ iv) mkfifo()
- ✓ v) sysconf()
- ✓ vi) pthread\_attr\_getstack()
- ✓ vii) pthread\_create()
- ✓ viii) setitimer()
- ✓ ix) kill()
- ✓ x) pthread\_join()

✓ **Q3. Write a system program that creates a child process whenever SIGUSR2 is received.**

✓ **Q4. Write a set of system programs that implements the client-server communication model between two processes using fifos. The communication is terminated when character '\$' is received by the server process. [PLO3/CLO3-Cognitive-Application]**

✓ **Q5. Compare and contrast the use of multi-threading and multi-processing for matrix multiplication. Discuss from the point of view of memory overhead, cpu load and execution time. Justify your reasoning with example matrices. [PLO2/CLO2-Cognitive-Analysis]**