**ASSIGNMENT # 01**



**Fall 2024**

**CSE-420 Embedded Systems**

Submitted by: **Ali Asghar**

Registration No.: **21PWCSE2059**

Class Section: **C**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

**Dr. Asif Ali Khan**

Date:

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**Department of Computer Systems Engineering**

**University of Engineering and Technology, Peshawar**

**Q: Write 20 DRAM commands.**

**Ans:**

1. **PRECHARGE (PRE):**
   * Description: Closes an active row in the specified bank of DRAM, allowing the next command to access a different row.
   * Purpose: Precharging is essential to prepare the memory bank for the next operation and helps prevent data corruption.
2. **ACTIVATE (ACT):**
   * Description: Opens a specific row within a selected bank, making it accessible for read or write operations.
   * Purpose: This command sets the row address that will be accessed for subsequent read or write commands.
3. **READ (RD):**
   * Description: Initiates a read operation from the currently active row and retrieves data from the specified column address.
   * Purpose: This command is critical for fetching data stored in the memory and involves transferring the data from the DRAM to the memory controller.
4. **WRITE (WR):**
   * Description: Initiates a write operation to the currently active row, sending data to a specified column address.
   * Purpose: This command allows the CPU or memory controller to store data in the DRAM, essential for maintaining program state.
5. **REFRESH (REF):**
   * Description: Periodically refreshes all rows in the DRAM to prevent data loss due to charge leakage.
   * Purpose: Refreshing is crucial for dynamic RAM, as data stored in DRAM cells can dissipate over time.
6. **BANK SELECT:**
   * Description: Selects one of the multiple memory banks available in DRAM.
   * Purpose: By specifying a bank, the memory controller can efficiently manage multiple simultaneous operations.
7. **COLUMN ADDRESS (COL):**
   * Description: Specifies the column address within the currently activated row for read or write operations.
   * Purpose: This is necessary for pinpointing the exact location of data within the row.
8. **ROW ADDRESS (ROW):**
   * Description: Specifies the row address that needs to be activated for access.
   * Purpose: This address is required before reading or writing data to access the desired location in the memory.
9. **MODE REGISTER SET (MRS):**
   * Description: Configures the operational parameters of the DRAM, such as latency, burst length, and timing.
   * Purpose: Setting the mode register is important for optimizing performance based on the specific application.
10. **WRITE MASK (WM):**
    * Description: Allows selective writing of bits by applying a mask during write operations.
    * Purpose: This enables partial updates to the data in a given row without affecting other bits.
11. **READ MODIFY WRITE (RMW):**
    * Description: Reads data from a specific location, modifies it, and writes it back in one atomic operation.
    * Purpose: This command is useful for ensuring data integrity when performing operations that require reading and modifying data.
12. **POWER DOWN (PD):**
    * Description: Puts the DRAM device into a low-power state to save energy when not in use.
    * Purpose: Power-down modes help reduce overall power consumption, particularly in mobile and embedded systems.
13. **AUTO REFRESH (AR):**
    * Description: Automatically refreshes all active banks in the DRAM without requiring individual precharge commands.
    * Purpose: This command simplifies refresh management by allowing the controller to handle multiple banks at once.
14. **WRITE LEVELING:**
    * Description: Adjusts the timing of write signals to align them with the clock signal for improved data integrity.
    * Purpose: This helps to ensure that data is written correctly, especially in high-speed memory operations.
15. **READ LEVELING:**
    * Description: Adjusts the timing of read signals to ensure that data is read in sync with the clock signal.
    * Purpose: Like write leveling, this command improves data integrity and reliability during read operations.
16. **BURST READ:**
    * Description: Initiates a read operation that retrieves multiple consecutive data elements in a single command.
    * Purpose: This increases throughput by minimizing the overhead of multiple read commands.
17. **BURST WRITE:**
    * Description: Initiates a write operation that sends multiple consecutive data elements in a single command.
    * Purpose: Similar to burst read, this improves efficiency and throughput during write operations.
18. **READ DQS (Data Strobe):**
    * Description: Adjusts the timing of the Data Strobe signal used during read operations to synchronize data transfer.
    * Purpose: Proper DQS timing is crucial for reliable data retrieval from the memory.
19. **WRITE DQS:**
    * Description: Adjusts the timing of the Data Strobe signal during write operations.
    * Purpose: Ensuring accurate timing helps maintain data integrity during writing.
20. **TERMINATE (TERM):**
    * Description: Ends an ongoing read or write operation before it completes.
    * Purpose: This command can be used to halt operations that are no longer needed, allowing for better resource management.