VIA Labs, Inc.

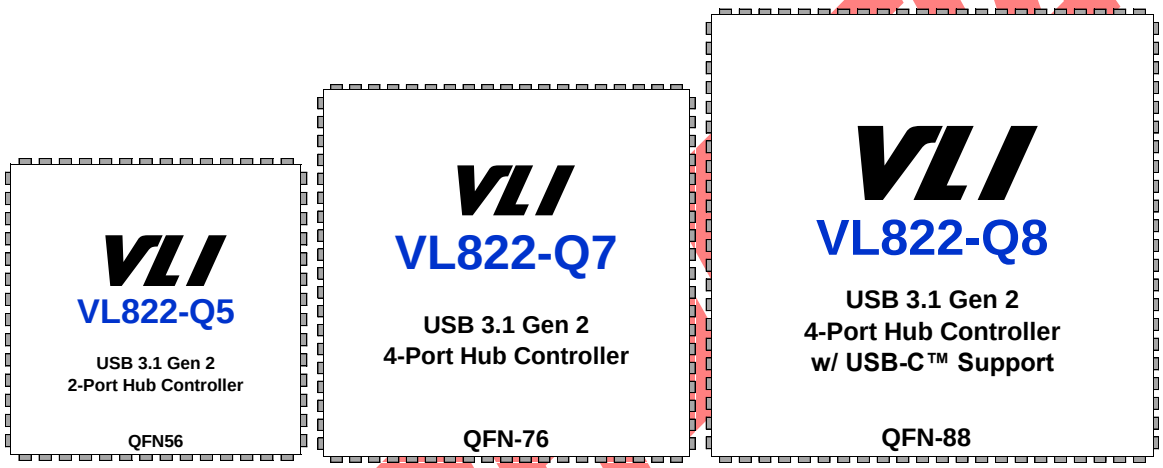
Data Sheet

VL822

USB 3.1 Gen2 Hub Controller

December 26th, 2018

Revision 0.90



Revision History

Rev	Date	Note	Initial
0.90	12/26/2018	First Preliminary Release	EC

Contents

List of Figures

Product Features

VL822-Q8 / VL822-Q7 / VL822-Q5

USB 3.1 Gen2 SuperSpeed Plus 4/2-Port USB Hub Controller

■ USB 3.1 Compliant
– Compliant to Universal Serial Bus 3.1 Specification
– SuperSpeed Plus USB (USB 3.1 Gen2)
– Compliant to Universal Serial Bus 2.0 Specification
– USB 2.0 Hub Supports MTT
– Supports Simultaneous Operation of Any Combination of SuperSpeed Plus, SuperSpeed, High-Speed, Full-Speed, and Low-Speed Devices
– Supports USB Power Saving Features such as Link Power Management, Ux States, Selective Suspend, and Function Suspend
– In-house USB PHY employs advanced CMOS process for low power consumption

■ **USB Type-C 1.0 Rev 1.2 Compliant**
– Compliant to USB Type-C Specification Rev 1.3
– VL822-Q8: Integrated 10Gbps Mux for UFP and 2x DFP
– Requires External CC Logic Controller for Orientation Detection/Vconn (Such as VP246 or VP225)
– Additional USB-C DFP support requires separate CC Logic and Mux

■ **Integrated USB Devices**
– USB Billboard Class 1.21 Device
Implemented as a USB 2.0 Virtual Device
Configurable Behavior – Expose When Necessary / Always Present / Disabled
– USB HID Class Device
Implemented as a USB 2.0 Virtual Device, Facilitates FW Update or Media Control Buttons
Configurable Behavior – Always Present / Disabled

■ **Full Sideband Signal Support**
– Supports Any Combination of Individual or Ganged Mode Over-Current for All Ports
– Supports PWM LED Status Lights
– SPI Interface for Firmware.
– Firmware Upgradable over USB

■ **Comprehensive USB Battery Charging Support**
– Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
– Support for Vendor Specific Charging Modes eg. Apple 2.4A, Samsung, etc.
– Supports YD/T 1591-2009
– Supports Stand-Alone Charging when System is Suspend, Shut Down, or Disconnected
– Any Combination of DFPs can be Configured to Support USB Battery Charging

■ **Power and Package**
– Requires 3.3V and 1.05V Inputs
– VL822-Q8: QFN 88L green package (10x10x0.85 mm)
– VL822-Q7: QFN 76L green package (9x9x0.85 mm)
– VL822-Q5: QFN 56L green package (7x7x0.85 mm)
– Pin Compatibility with VL820
– 25MHz Xtal

VL822 System Overview

VIA Lab's VL822 is USB 3.1 Gen2 Hub Controller and it features highly integrated, application specific design. VL822 features 1x upstream port and 4x/2x downstream ports, all of which support 10Gbps USB 3.1 Gen2 operation. The downstream ports can support any combination of SuperSpeed Plus (10Gbps), SuperSpeed (5Gbps), High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) devices. VL822's integrated USB 2.0 hub features Multiple Transaction Translators, providing increased bandwidth and performance when multiple Full Speed devices are simultaneously used.

VL822 comes in three variants: VL822-Q8 utilizes the QFN88 10x10x0.85 mm package while the VL822-Q7 utilizes the smaller QFN76 9x9x0.85mm package and VL822-Q5 utilizes the smaller QFN56 7x7x0.85mm package for two port configure. The larger QFN88 variant features integrated 10Gbps Muxes for the Upstream Facing Port and two Downstream Facings Ports whereas the smaller QFN76/QFN56 variant does not. The integrated 10Gbps Muxes are ideal for Data-Only USB-C applications that would otherwise require an external Mux, with the advantage of potential board area savings and improved signal integrity. If additional USB-C Ports are need, separate CC Logic and Mux solutions.

VL822 features an optionally configurable USB Billboard Device when used in USB-PD Alternate Mode applications, and an optionally configurable USB HID endpoint to support Media Control Buttons such as Play/Pause, Volume Up/Down, etc.

VL822 features flexible firmware architecture, providing a framework for custom functions in addition to in-field updates. Various parameters including USB configuration, Tx equalization setting, and GPIO behavior are changeable via firmware. VL822 also features an optionally configurable USB Charging Controller for charging various devices such as smartphones and tablets that can be configure on a per-port basis.

VL822-based hub devices work under Windows, Mac OS X, and various Linux kernels without additional drivers. VL822-based hub devices are also compatible with non-x86 devices and platforms that support USB hub functions such as smart phones, tablets, and set-top boxes. It is well suited for all USB hub applications such as standalone USB hubs, Notebook/Ultrabook docking stations/port-replicators, desktop PC front panel, motherboard on-board hub, and USB hub compound devices.

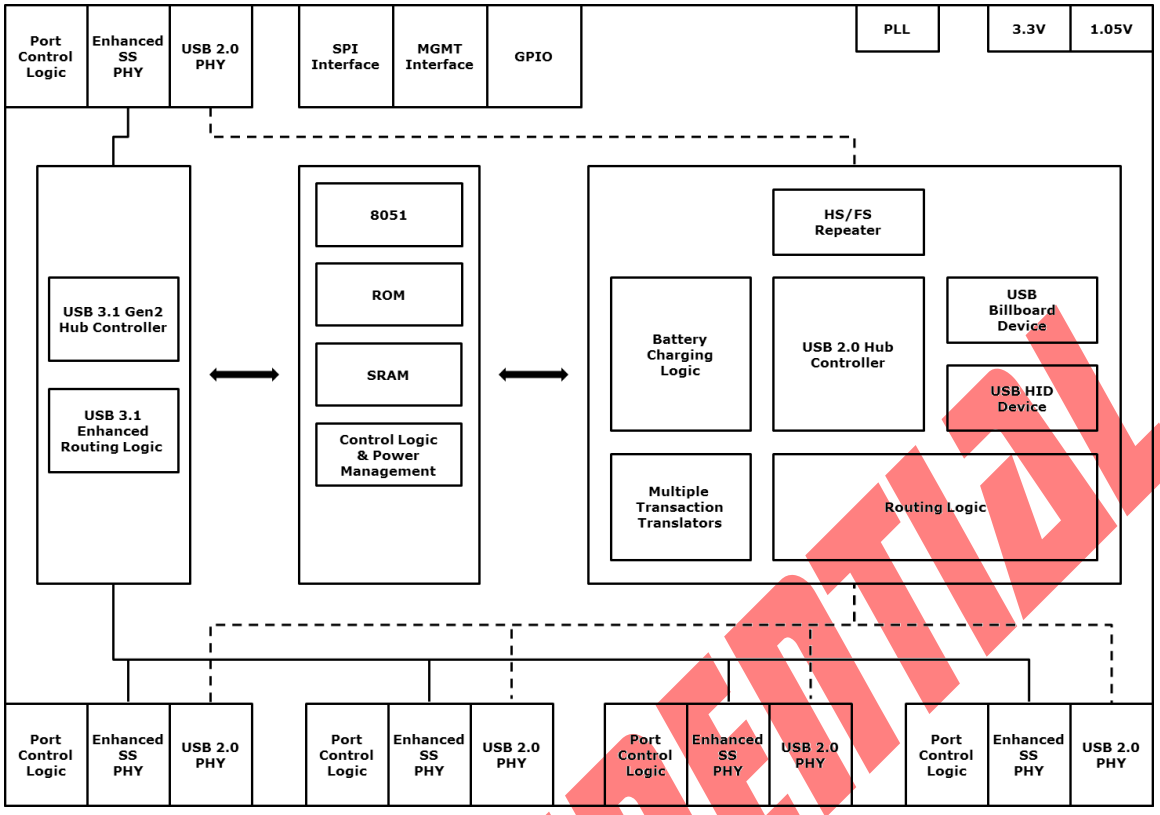


Figure 1 – VL822-Q7 Block Diagram

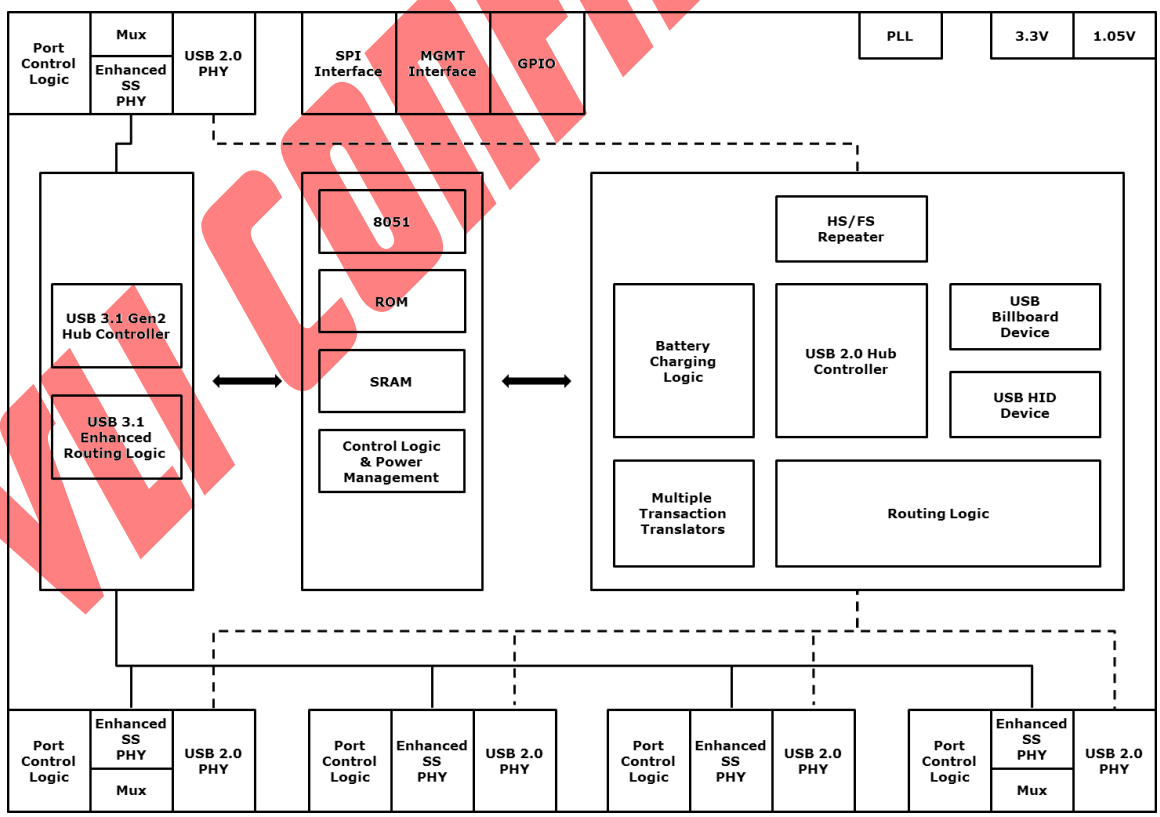


Figure 2 – VL822-Q8 Block Diagram

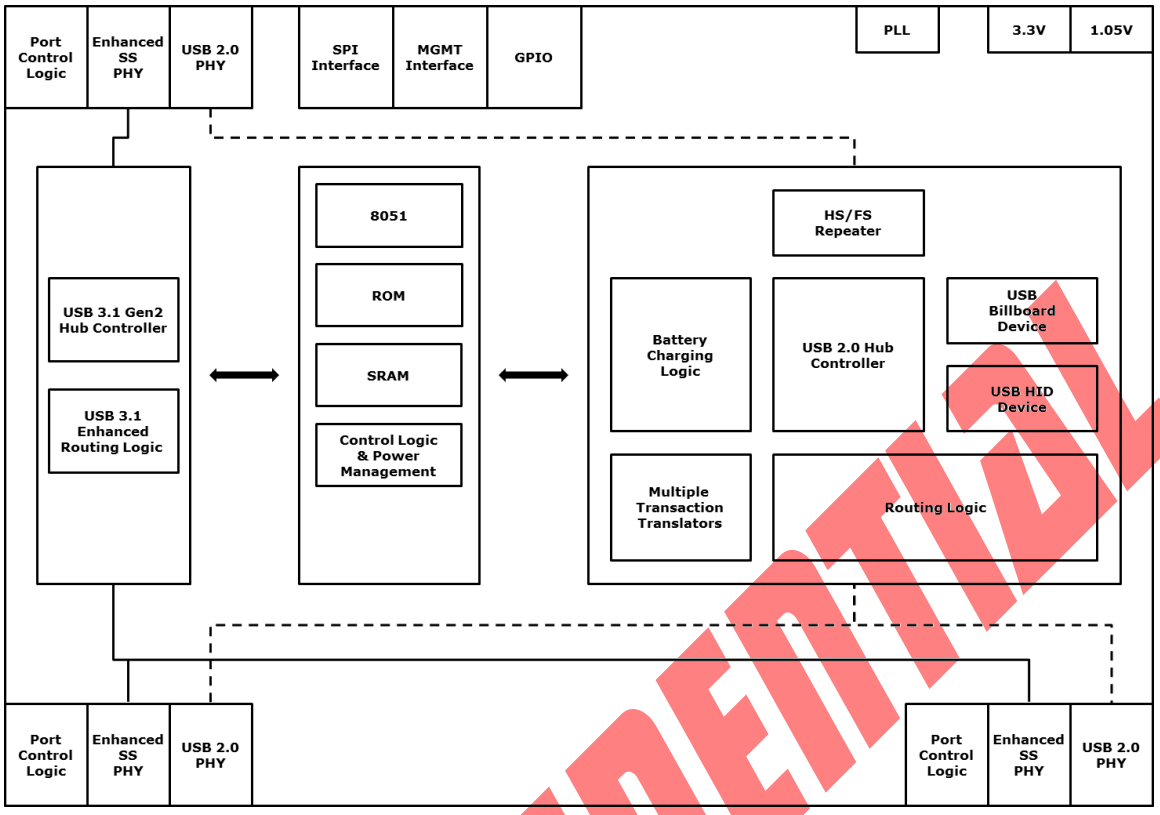


Figure 3 – VL822-Q5 Block Diagram

USB Battery Charging Behavior

3 Concepts of Rapid Charging over USB:

- **Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.**

  The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.0 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 1000mA to 2400mA.

- **It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine those capabilities.**

  Rapid Charging over USB enables charging at rates in excess of baseline USB specifications, so in order to prevent a situation where a device sinks more current than what a port is rated for, different manufacturers employ various charging schemes in an attempt to ensure safe and reliable operation with their respective device and charger. It goes without saying that Rapid Charging will only occur when both Host/Hub and Device supports it.

- **The rate at which a device charges is dependent upon the device.**

  This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port

This is a typical USB 2.0 or USB 3.0 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.0 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.0 modes.

CDP – Charging Downstream Port

CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

DCP – Dedicated Charging Port

DCP is defined in the USB Battery Charging Specification 1.2 and has been in use on an unofficial basis prior to the official USB Battery Charging Specification. DCP is a dedicated charging mode, so when a device is charging under DCP, regular USB operations such as data transfer to the device are not supported.

Special Modes

Various vendors such as Apple, RIM, Motorola, etc. may employ different detection mechanisms compared to other USB devices and thus, may enter Rapid Charging under the previously mentioned charging modes. VL822 supports an auto detection mechanism that provides charging for the majority of devices.

Pinout (VL822-Q7)

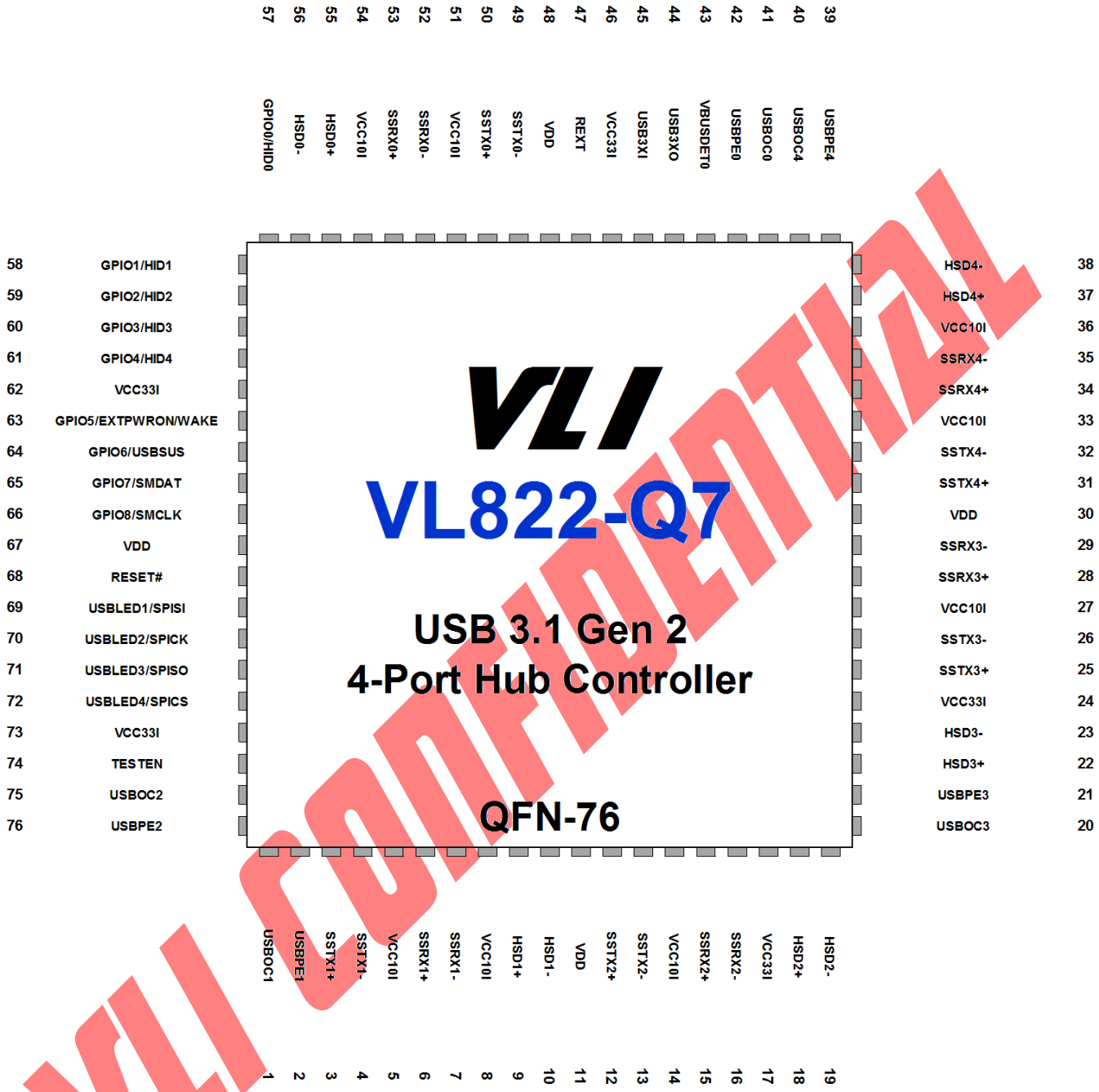


Figure 4 – VL822-Q7 Pin Diagram

Pin List (VL822-Q7)

Table 1 – VL822-Q7 Pin List

Pin	Pin Name	Pin	Pin Name
1	USBOC1	39	USBPE4
2	USBPE1	40	USBOC4
3	SSTX1+	41	USBOC0
4	SSTX1–	42	USBPE0
5	VCC10I	43	VBUSDET0
6	SSRX1+	44	USB3XO
7	SSRX1–	45	USB3XI
8	VCC10I	46	VCC33I
9	HSD1+	47	REXT
10	HSD1–	48	VDD
11	VDD	49	SSTX0–
12	SSTX2+	50	SSTX0+
13	SSTX2–	51	VCC10I
14	VCC10I	52	SSRX0–
15	SSRX2+	53	SSRX0+
16	SSRX2–	54	VCC10I
17	VCC33I	55	HSD0+
18	HSD2+	56	HSD0–
19	HSD2–	57	GPIO0/HID0
20	USBOC3	58	GPIO1/HID1
21	USBPE3	59	GPIO2/HID2
22	HSD3+	60	GPIO3/HID3
23	HSD3–	61	GPIO4/HID4
24	VCC33I	62	VCC33I
25	SSTX3+	63	GPIO5/EXTPWRON/WAKE
26	SSTX3–	64	GPIO6 / USBSUS
27	VCC10I	65	GPIO7 / SMDAT
28	SSRX3+	66	GPIO8 / SMCLK
29	SSRX3–	67	VDD
30	VDD	68	RESET#
31	SSTX4+	69	USBLED1 / SPISI
32	SSTX4–	70	USBLED2 / SPICK
33	VCC10I	71	USBLED3 / SPISO
34	SSRX4+	72	USBLED4 / SPICS
35	SSRX4–	73	VCC33I
36	VCC10I	74	TESTEN
37	HSD4+	75	USBOC2
38	HSD4–	76	USBPE2

Pin Descriptions (VL822-Q7)

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/ Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0-	49	O	USB 3.1 UFP Differential TX–
SSTX0+	50	O	USB 3.1 UFP Differential TX+
SSRX0-	52	I	USB 3.1 UFP Differential RX–
SSRX0+	53	I	USB 3.1 UFP Differential RX+
SSTX1+	3	O	USB 3.1 DFP1 Differential TX+
SSTX1-	4	O	USB 3.1 DFP1 Differential TX–
SSRX1+	6	I	USB 3.1 DFP1 Differential RX+
SSRX1-	7	I	USB 3.1 DFP1 Differential RX–
SSTX2+	12	O	USB 3.1 DFP2 Differential TX+
SSTX2-	13	O	USB 3.1 DFP2 Differential TX–
SSRX2+	15	I	USB 3.1 DFP2 Differential RX+
SSRX2-	16	I	USB 3.1 DFP2 Differential RX–
SSTX3+	25	O	USB 3.1 DFP3 Differential TX+
SSTX3-	26	O	USB 3.1 DFP3 Differential TX–
SSRX3+	28	I	USB 3.1 DFP3 Differential RX+
SSRX3-	29	I	USB 3.1 DFP3 Differential RX–
SSTX4+	31	O	USB 3.1 DFP4 Differential TX+
SSTX4-	32	O	USB 3.1 DFP4 Differential TX–
SSRX4+	34	I	USB 3.1 DFP4 Differential RX+
SSRX4-	35	I	USB 3.1 DFP4 Differential RX–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
USB3XO	44	O	25M Crystal Output
USB3XI	45	I	25M Crystal Input
REXT	47	I	Connect to External Reference Resistor (12.4K+/- 1%)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	74	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO7 / SMDAT	65	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus data with Proprietary Data Format. (Open Drain)
GPIO8 / SMCLK	66	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus clock with Proprietary Data Format. (Open Drain)

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	55	I/O	USB 2.0 UFP Differential D+
HSD0–	56	I/O	USB 2.0 UFP Differential D–
HSD1+	9	I/O	USB 2.0 DFP1 Differential D+
HSD1–	10	I/O	USB 2.0 DFP1 Differential D–
HSD2+	18	I/O	USB 2.0 DFP2 Differential D+
HSD2–	19	I/O	USB 2.0 DFP2 Differential D–
HSD3+	22	I/O	USB 2.0 DFP3 Differential D+
HSD3–	23	I/O	USB 2.0 DFP3 Differential D–
HSD4+	37	I/O	USB 2.0 DFP4 Differential D+
HSD4–	38	I/O	USB 2.0 DFP4 Differential D–

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VDD	11, 30, 48, 67	PWR	1.05V Core Power
VCC10I	5, 8, 14, 27, 33, 36, 51, 54	PWR	1.05V Analog Power
VCC33I	17, 24, 46, 62, 73	PWR	3.3V Analog Power

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC0	41	I or I/O	UFP Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE0	42	O	UFP USB PE USB Power Enable Mode High: Enable Low: Off
USBOC1	1	I or I/O	DFP1 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE1	2	O	DFP1 USB PE USB Power Enable Mode High: Enable Low: Off

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC2	75	I or I/O	DFP2 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE2	76	O	DFP2 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC3	20	I or I/O	DFP3 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE3	21	O	DFP3 USB PE USB Power Enable Mode High: Enable Low: Off
USBPE4	39	I or I/O	DFP4 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC4	40	O	DFP4 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
GPIO0 / HID0	57	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO1 / HID1	58	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO2 / HID2	59	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO3 / HID3	60	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO4 / HID4	61	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO5 / EXTPWRON / WAKE	63	I/O	GPIO / External Power Status / Wake Shared pin. Available for GPIO Use, Config via Firmware Setting. DC Jack Power Source Insert Detection (3.3V Max) Available for Connected Standby use, Config via Firmware Setting.
GPIO6 / USBSUS	64	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
RESET#	68	I	Reset Input of Hub Controller Low: Reset High: Normal Operation Power On sequence, Refer to Appendix-1.
USBLED1 / SPISI	69	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
USBLED2 / SPICLK	70	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
USBLED3 / SPISO	71	I/O	DFP3 LED Indicator / SPISO shared pin. Active High Output for LED Use.
USBLED4 / SPICS	72	I/O	DFP4 LED Indicator / SPICS shared pin. Active High Output for LED Use
VBUSDET0	43	I	UFP Vbus Detection (3.3V Max)

Pinout (VL822-Q8)

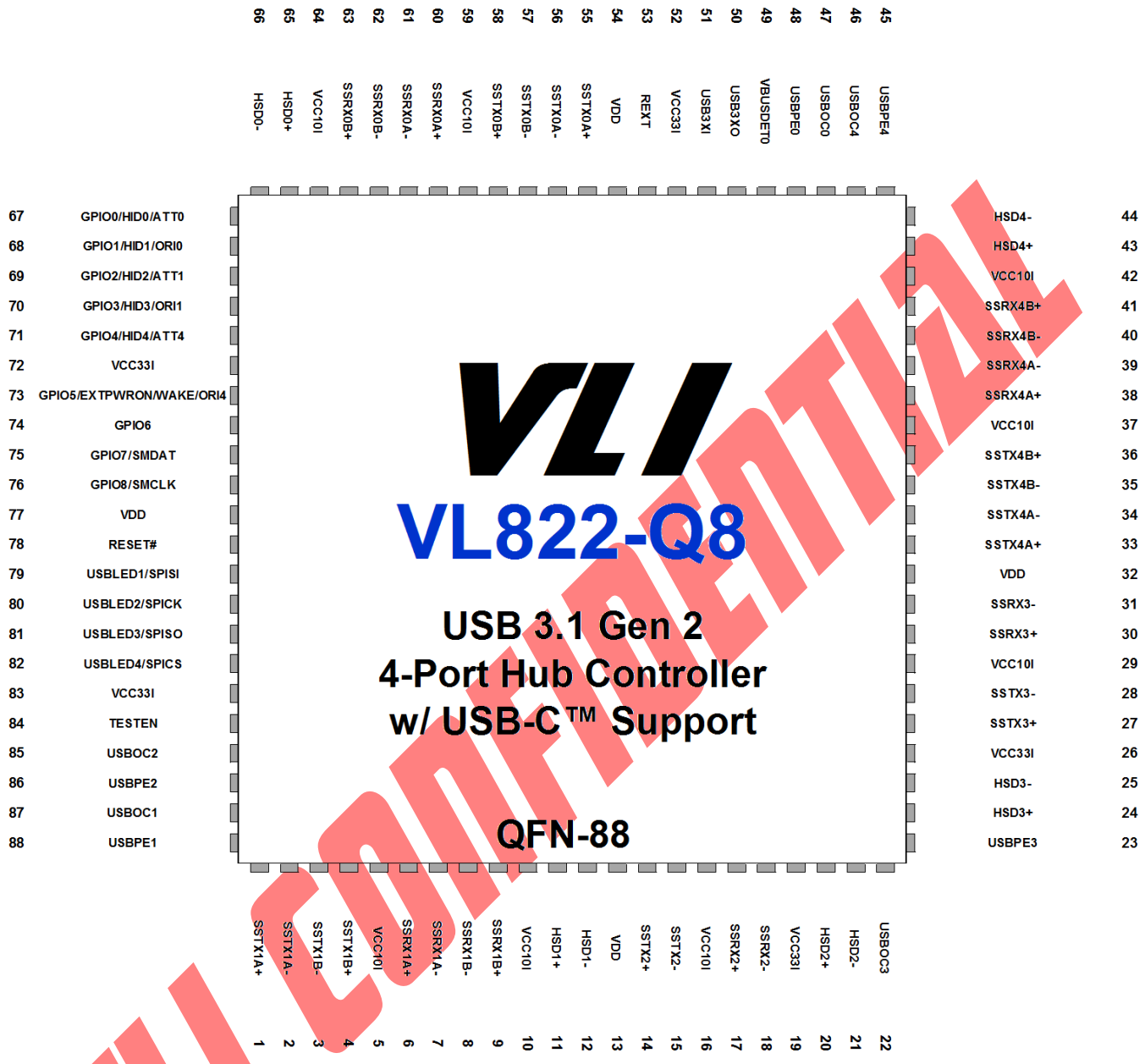


Figure 5 – VL822-Q8 Pin Diagram

Pin List (VL822-Q8)

Table 2 – VL822-Q8 Pin List

Pin	Pin Name	Pin	Pin Name
1	SSTX1A+	45	USBPE4
2	SSTX1A–	46	USBOC4
3	SSTX1B–	47	USBOC0
4	SSTX1B+	48	USBPE0
5	VCC10I	49	VBUSDET0
6	SSRX1A+	50	USB3XO
7	SSRX1A–	51	USB3XI
8	SSRX1B–	52	VCC33I
9	SSRX1B+	53	REXT
10	VCC10I	54	VDD
11	HSD1+	55	SSTX0A+
12	HSD1–	56	SSTX0A–
13	VDD	57	SSTX0B–
14	SSTX2+	58	SSTX0B+
15	SSTX2–	59	VCC10I
16	VCC10I	60	SSRX0A+
17	SSRX2+	61	SSRX0A–
18	SSRX2–	62	SSRX0B–
19	VCC33I	63	SSRX0B+
20	HSD2+	64	VCC10I
21	HSD2–	65	HSD0+
22	USBOC3	66	HSD0–
23	USBPE3	67	GPIO0/HID0/ATT0
24	HSD3+	68	GPIO1/HID1/ORI0
25	HSD3–	69	GPIO2/HID2/ATT1
26	VCC33I	70	GPIO3/HID3/ORI1
27	SSTX3+	71	GPIO4/HID4/ATT4
28	SSTX3–	72	VCC33I
29	VCC10I	73	GPIO5/EXTPWRON/WAKE/ORI4
30	SSRX3+	74	GPIO6
31	SSRX3–	75	GPIO7 / SMDAT
32	VDD	76	GPIO8 / SMCLK
33	SSTX4A+	77	VDD
34	SSTX4A–	78	RESET#
35	SSTX4B–	79	USBLED1 / SPISI
36	SSTX4B+	80	USBLED2 / SPICK
37	VCC10I	81	USBLED3 / SPISO
38	SSRX4A+	82	USBLED4 / SPICS
39	SSRX4A–	83	VCC33I
40	SSRX4B–	84	TESTEN
41	SSRX4B+	85	USBOC2
42	VCC10I	86	USBPE2
43	HSD4+	87	USBOC1
44	HSD4–	88	USBPE1

Pin Descriptions (VL822-Q8)

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/ Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0A+	55	O	USB 3.1 UFP Differential TX+; Side A
SSTX0A-	56	O	USB 3.1 UFP Differential TX–; Side A
SSTX0B-	57	O	USB 3.1 UFP Differential TX–; Side B
SSTX0B+	58	O	USB 3.1 UFP Differential TX+; Side B
SSRX0A+	60	I	USB 3.1 UFP Differential RX+; Side A
SSRX0A-	61	I	USB 3.1 UFP Differential RX–; Side A
SSRX0B-	62	I	USB 3.1 UFP Differential RX–; Side B
SSRX0B+	63	I	USB 3.1 UFP Differential RX+; Side B
SSTX1A+	1	O	USB 3.1 DFP1 Differential TX+; Side A
SSTX1A-	2	O	USB 3.1 DFP1 Differential TX–; Side A
SSTX1B-	3	O	USB 3.1 DFP1 Differential TX–; Side B
SSTX1B+	4	O	USB 3.1 DFP1 Differential TX+; Side B
SSRX1A+	6	I	USB 3.1 DFP1 Differential RX+; Side A
SSRX1A-	7	I	USB 3.1 DFP1 Differential RX–; Side A
SSRX1B-	8	I	USB 3.1 DFP1 Differential RX–; Side B
SSRX1B+	9	I	USB 3.1 DFP1 Differential RX+; Side B
SSTX2+	14	O	USB 3.1 DFP2 Differential TX+
SSTX2-	15	O	USB 3.1 DFP2 Differential TX–
SSRX2+	17	I	USB 3.1 DFP2 Differential RX+
SSRX2-	18	I	USB 3.1 DFP2 Differential RX–
SSTX3+	27	O	USB 3.1 DFP3 Differential TX+
SSTX3-	28	O	USB 3.1 DFP3 Differential TX–
SSRX3+	30	I	USB 3.1 DFP3 Differential RX+
SSRX3-	31	I	USB 3.1 DFP3 Differential RX–
SSTX4A+	33	O	USB 3.1 DFP4 Differential TX+; Side A
SSTX4A-	34	O	USB 3.1 DFP4 Differential TX–; Side A
SSTX4B-	35	O	USB 3.1 DFP4 Differential TX–; Side B
SSTX4B+	36	O	USB 3.1 DFP4 Differential TX+; Side B
SSRX4A+	38	I	USB 3.1 DFP4 Differential RX+; Side A
SSRX4A-	39	I	USB 3.1 DFP4 Differential RX–; Side A
SSRX4B-	40	I	USB 3.1 DFP4 Differential RX–; Side B
SSRX4B+	41	I	USB 3.1 DFP4 Differential RX+; Side B

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	65	I/O	USB 2.0 UFP Differential D+
HSD0–	66	I/O	USB 2.0 UFP Differential D–
HSD1+	11	I/O	USB 2.0 DFP1 Differential D+
HSD1–	12	I/O	USB 2.0 DFP1 Differential D–
HSD2+	20	I/O	USB 2.0 DFP2 Differential D+
HSD2–	21	I/O	USB 2.0 DFP2 Differential D–
HSD3+	24	I/O	USB 2.0 DFP3 Differential D+
HSD3–	25	I/O	USB 2.0 DFP3 Differential D–
HSD4+	43	I/O	USB 2.0 DFP4 Differential D+
HSD4–	44	I/O	USB 2.0 DFP4 Differential D–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
USB3XO	50	O	25M Crystal Output
USB3XI	51	I	25M Crystal Input
REXT	53	I	Connect to External Reference Resistor (12.4K+/- 1%)

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VDD	13,32,54, 77	PWR	1.05V Core Power
VCC10I	5, 10, 16, 29, 37, 42, 59. 64,	PWR	1.05V Analog Power
VCC33I	19, 26, 52, 72, 83	PWR	3.3V Analog Power

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	84	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO7 / SMDAT	75	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus data with Proprietary Data Format. (Open Drain)
GPIO8 / SMCLK	76	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus clock with Proprietary Data Format. (Open Drain)

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC0	47	I or I/O	UFP Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE0	48	O	UFP USB PE USB Power Enable Mode High: Enable Low: Off
USBOC1	87	I or I/O	DFP1 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE1	88	O	DFP1 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC2	85	I or I/O	DFP2 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE2	86	O	DFP2 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC3	22	I or I/O	DFP3 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE3	23	O	DFP3 USB PE USB Power Enable Mode High: Enable Low: Off
USBPE4	45	I or I/O	DFP4 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC4	46	O	DFP4 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
GPIO0 / HID0 / ATT0	67	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting. UFP Host Attach Status Input Pin, Refer to Appendix-2.
GPIO1 / HID1 / ORI0	68	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting. UFP Mux Orientation Setting Input Pin, Refer to Appendix-2.
GPIO2 / HID2 / ATT1	69	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting. DFP1 Device Attach Status Input Pin, Refer to Appendix-2.
GPIO3 / HID3 / ORI1	70	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting. DFP1 Mux Orientation Setting Input Pin, Refer to Appendix-2.
GPIO4 / HID4 / ATT4	71	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting. DFP4 Device Attach Status Input Pin, Refer to Appendix-2.
GPIO5 / EXTPWRON / WAKE / ORI4	73	I/O	GPIO / External Power Status / Wake Shared pin. Available for GPIO Use, Config via Firmware Setting. DC Jack Power Source Insert Detection (3.3V Max). Available for Connected Standby use, Config via Firmware Setting. DFP4 Mux Orientation Setting Input Pin, Refer to Appendix-2.
GPIO6	74	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
RESET#	78	I	Reset Input of Hub Controller Low: Reset High: Normal Operation Power On sequence, Refer to Appendix-1.
USBLED1/SPISI	79	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
USBLED2/SPICLK	80	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
USBLED3/SPISO	81	I/O	DFP3 LED Indicator / SPISO shared pin. Active High Output for LED Use.
USBLED4/SPICS	82	I/O	DFP4 LED Indicator / SPICS shared pin. Active High Output for LED Use
VBUSDET0	49	I	UFP Vbus Detection (3.3V Max)

Pinout (VL822-Q5)

Figure 6 – VL822-Q5 Pin Diagram

Pin List (VL822-Q5)

Table 3 – VL822-Q5 Pin List

Pin	Pin Name	Pin	Pin Name
1	SSTX1+	29	VCC33I
2	SSTX1–	30	REXT
3	VCC10I	31	VDD
4	SSRX1+	32	SSTX0–
5	SSRX1–	33	SSTX0+
6	VCC10I	34	VCC10I
7	HSD1+	35	SSRX0–
8	HSD1–	36	SSRX0+
9	VDD	37	VCC10I
10	SSTX2+	38	HSD0+
11	SSTX2–	39	HSD0–
12	VCC10I	40	GPIO0/HID0
13	SSRX2+	41	VCC33I
14	SSRX2–	42	GPIO6 / USBSUS
15	VCC33I	43	GPIO7 / SMDAT
16	HSD2+	44	GPIO8 / SMCLK
17	HSD2–	45	VDD
18	GPIO/SDA3	46	RESET#
19	GPIO/SCL3	47	USBLED1 / SPISI
20	VCC33I	48	USBLED2 / SPICK
21	VCC10I	49	SPISO
22	VDD	50	SPICS
23	VCC10I	51	VCC33I
24	USB3XI	52	TESTEN
25	USB3XO	53	USBOC2
26	VBUSDET0	54	USBPE2
27	GPIO/SCL4	55	USBOC1
28	GPIO/SDA4	56	USBPE1

Pin Descriptions (VL822-Q5)

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/ Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0-	32	O	USB 3.1 UFP Differential TX–
SSTX0+	33	O	USB 3.1 UFP Differential TX+
SSRX0-	35	I	USB 3.1 UFP Differential RX–
SSRX0+	36	I	USB 3.1 UFP Differential RX+
SSTX1+	1	O	USB 3.1 DFP1 Differential TX+
SSTX1-	2	O	USB 3.1 DFP1 Differential TX–
SSRX1+	4	I	USB 3.1 DFP1 Differential RX+
SSRX1-	5	I	USB 3.1 DFP1 Differential RX–
SSTX2+	10	O	USB 3.1 DFP2 Differential TX+
SSTX2-	11	O	USB 3.1 DFP2 Differential TX–
SSRX2+	13	I	USB 3.1 DFP2 Differential RX+
SSRX2-	14	I	USB 3.1 DFP2 Differential RX–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
USB3XO	25	O	25M Crystal Output
USB3XI	24	I	25M Crystal Input
REXT	30	I	Connect to External Reference Resistor (12.4K+/- 1%)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	52	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO7 / SMDAT	43	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus data with Proprietary Data Format. (Open Drain) Pin must be pulled high if NC.
GPIO8 / SMCLK	44	I/O	Available for GPIO Use, Config via Firmware Setting. SMBus clock with Proprietary Data Format. (Open Drain) Pin must be pulled high if NC.

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	38	I/O	USB 2.0 UFP Differential D+
HSD0–	39	I/O	USB 2.0 UFP Differential D–
HSD1+	7	I/O	USB 2.0 DFP1 Differential D+
HSD1–	8	I/O	USB 2.0 DFP1 Differential D–
HSD2+	16	I/O	USB 2.0 DFP2 Differential D+
HSD2–	17	I/O	USB 2.0 DFP2 Differential D–

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VDD	9, 22, 31, 45	PWR	1.05V Core Power
VCC10I	3, 6, 12, 21, 23, 34, 37	PWR	1.05V Analog Power
VCC33I	15, 20, 29, 41, 51	PWR	3.3V Analog Power

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC1	55	I or I/O	DFP1 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE1	56	O	DFP1 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC2	53	I or I/O	DFP2 Over Current Detection Open Drain (3.3V Max); Pin must be pulled high if NC. High: Normal Low: Port Over Current Event
USBPE2	54	O	DFP2 USB PE USB Power Enable Mode High: Enable Low: Off

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
GPIO0 / HID0	40	I/O	GPIO / HID Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for HID button Use, Config via Firmware Setting.
GPIO6 / USBSUS	42	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
RESET#	46	I	Reset Input of Hub Controller Low: Reset High: Normal Operation Power On sequence, Refer to Appendix-1.
USBLED1 / SPISI	47	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
USBLED2 / SPICLK	48	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
SPISO	49	I/O	SPISO pin.
SPICS	50	I/O	SPICS pin.
VBUSDET0	26	I	UFP Vbus Detection (3.3V Max)
GPIO/SDA3	18	I or I/O	GPIO / I2C Data Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for I2C Use, Config via Firmware Setting. Open Drain (3.3V Max); Pin must be pulled high if NC.
GPIO/SCL3	19	O	GPIO / I2C Clock Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for I2C Use, Config via Firmware Setting.
GPIO/SDA4	28	I or I/O	GPIO / I2C Data Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for I2C Use, Config via Firmware Setting. Open Drain (3.3V Max); Pin must be pulled high if NC.
GPIO/SCL4	27	O	GPIO / I2C Clock Shared Pin. Available for GPIO Use, Config via Firmware Setting. Available for I2C Use, Config via Firmware Setting.

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{33}	3.3V Power Supply Voltage	-0.5	3.63	V	—
V_{10}	1.05V Input Voltage	-0.5	1.1	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{jc}	Thermal resistance between junction and case	TBD		°C/W	4L PCB definitions follow JESD51-7
θ_{ja}	Thermal resistance between junction and ambient	TBD		°C/W	
P_D	Power dissipation	—	TBD	W	

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	70	°C	—
T_j	Junction Temperature	0	125	°C	—
V_{33}	3.3V Power Supply Voltage	3.0	3.6	V	—
V_{10}	1.05V Input Voltage	1.0	1.1	V	—
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.3	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<V_i<V_{33}
I_{OZ}	Tristate Leakage Current	—	+/-20	µA	0<V_o<V_{33}

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW data for VL822. This section specifies the SPI timing requirements for the device.

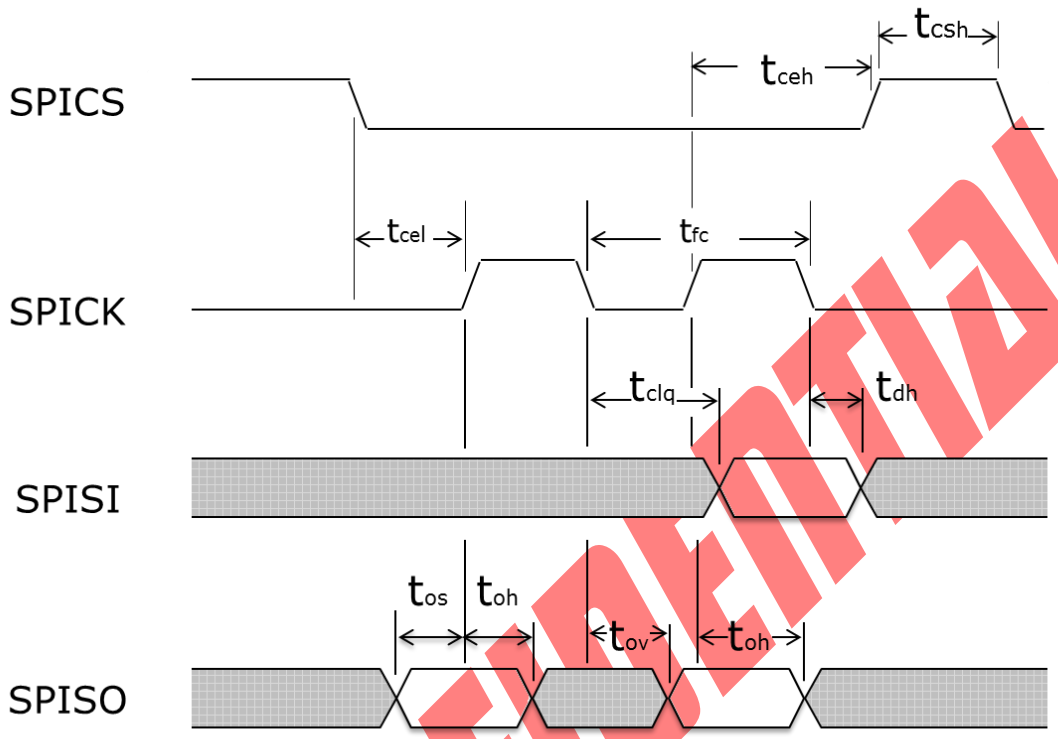


Figure 7 – SPI Timing

SPI Timing (7.8125 MHZ Operation)

Symbol	Parameters	Min	Typ	Max	Units
f_{CT}	Clock frequency		7.8125		MHz
t_{csh}	Chip enable (**SPICS**) high time	800			ns
t_{clq}	Clock to input data			20	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	20			ns
t_{oh}	Output hold time	10			ns
t_{ov}	Clock to output valid	5			ns
t_{cel}	Chip enable (**SPICS**) low to first clock	72			ns
t_{ceh}	last clock to chip enable (**SPICS**) high	72			ns

*Fast read mode must be supported.

General Reflow Profile Guidelines

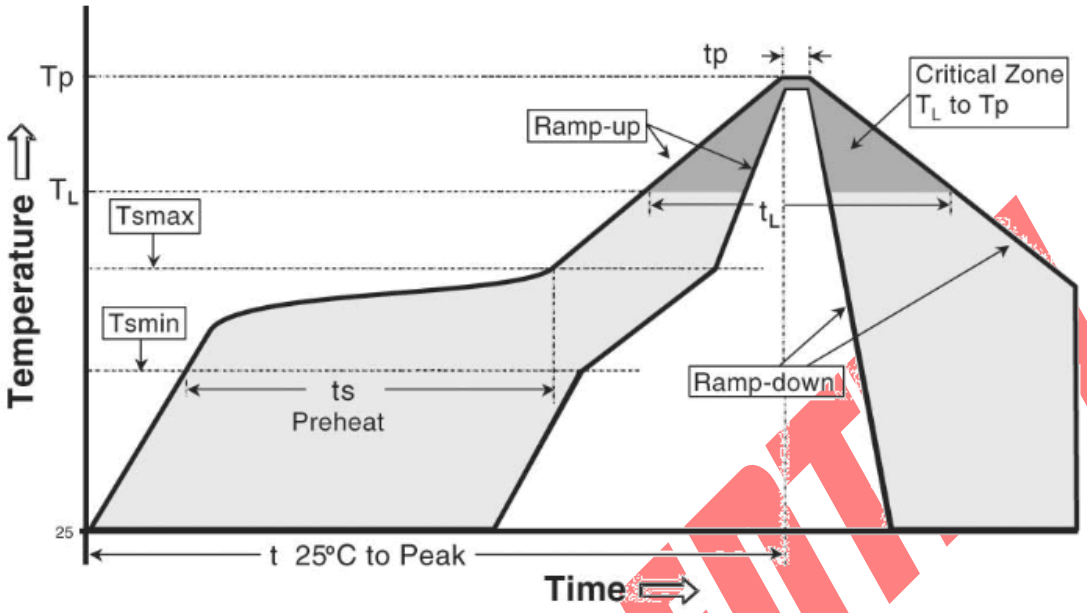
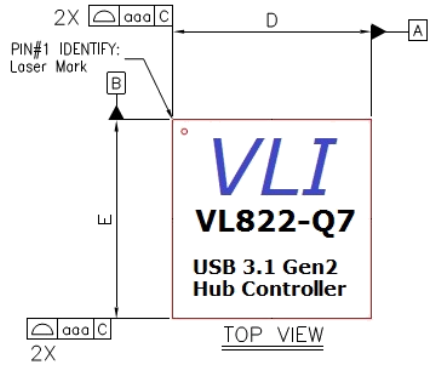


Figure 8 – Reflow

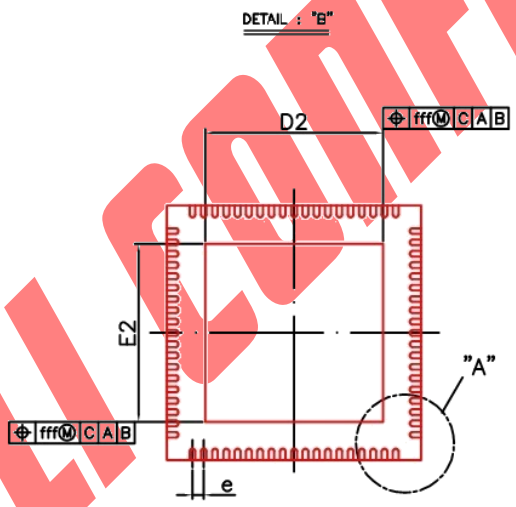
Profile Feature:	Sn-Pb Eutectic	Pb-Free solder
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3°C/second max.	3°C/second max.
Preheat/Soak Temperature Min. (T_{smin}) Temperature Max. (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Ts(max) to Tl -Ramp-up Rate		3°C/second max.
Time maintained above: Temperature (T_L) Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak package body temperature(Tp) Time within 5°C of actual peak temperature(Tp)	225+5/-0°C 20 seconds	255 +5/0°C 30 seconds
Ramp-down rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

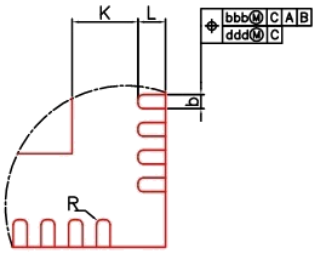
***Note 1:** All temperatures refer to the center of package, measured on package body surface
***Note 2:** The reflow condition may vary with PCB design; pitch; size; reflow; condition; solder and supplier, please contact your solder, reflow and vendors.

Package Mechanical Specifications (VL822-Q7)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	8.90	9.00	9.10
D2/E2	6.15	6.30	6.45
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

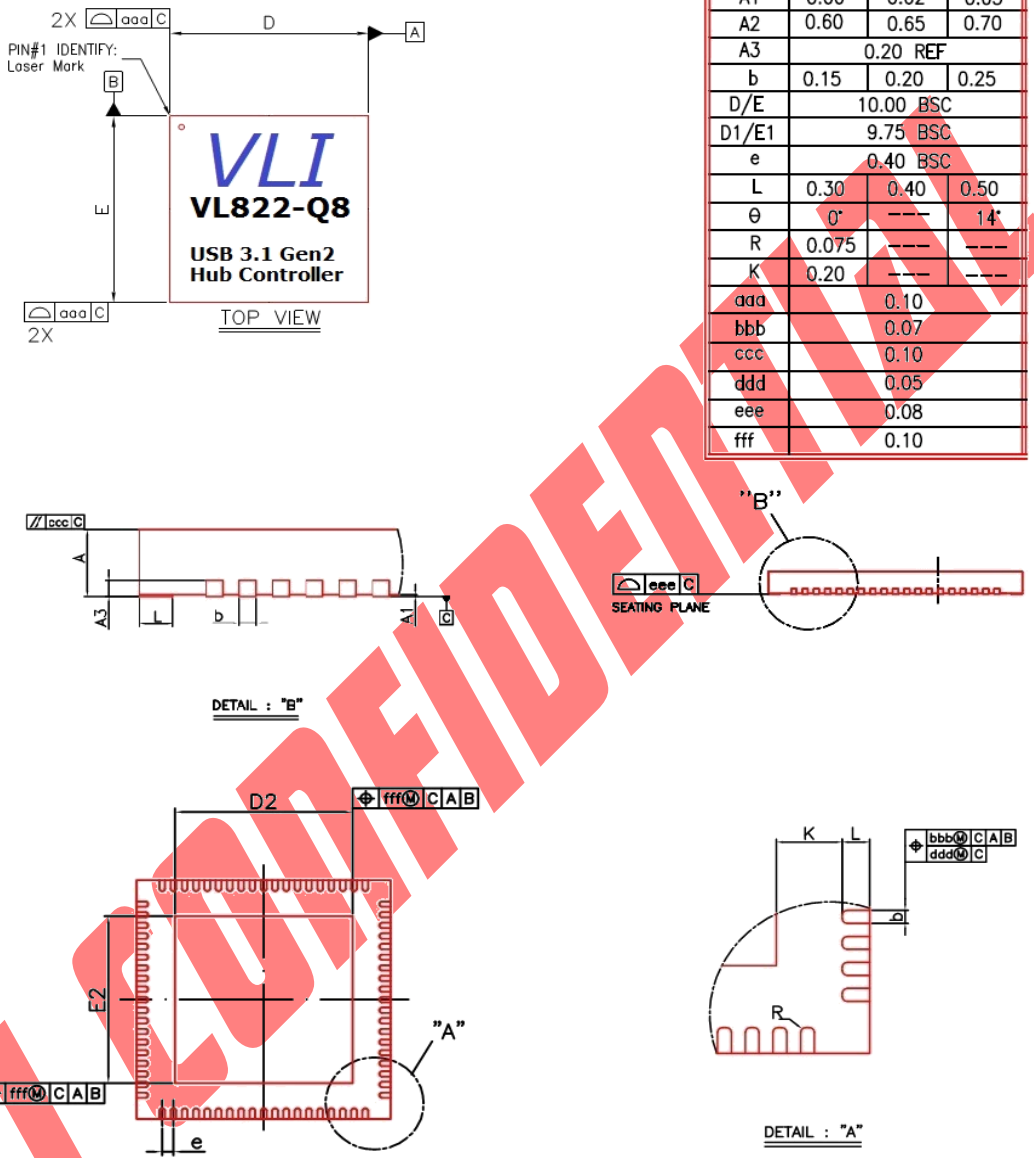




DETAIL : "A"

Figure 9 – Mechanical Specification – Q7 (QFN 76L 9x9x0.85 mm) Package

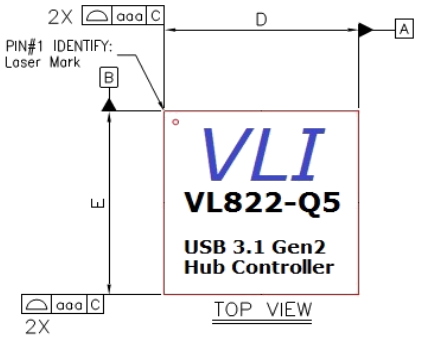
Package Mechanical Specifications (VL822-Q8)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D/E		10.00 BSC	
D1/E1		9.75 BSC	
e		0.40 BSC	
L	0.30	0.40	0.50
θ	0°	---	14°
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 10 – Mechanical Specification – Q8 (QFN 88L 10x10x0.85 mm) Package

Package Mechanical Specifications (VL822-Q5)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.075	---	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

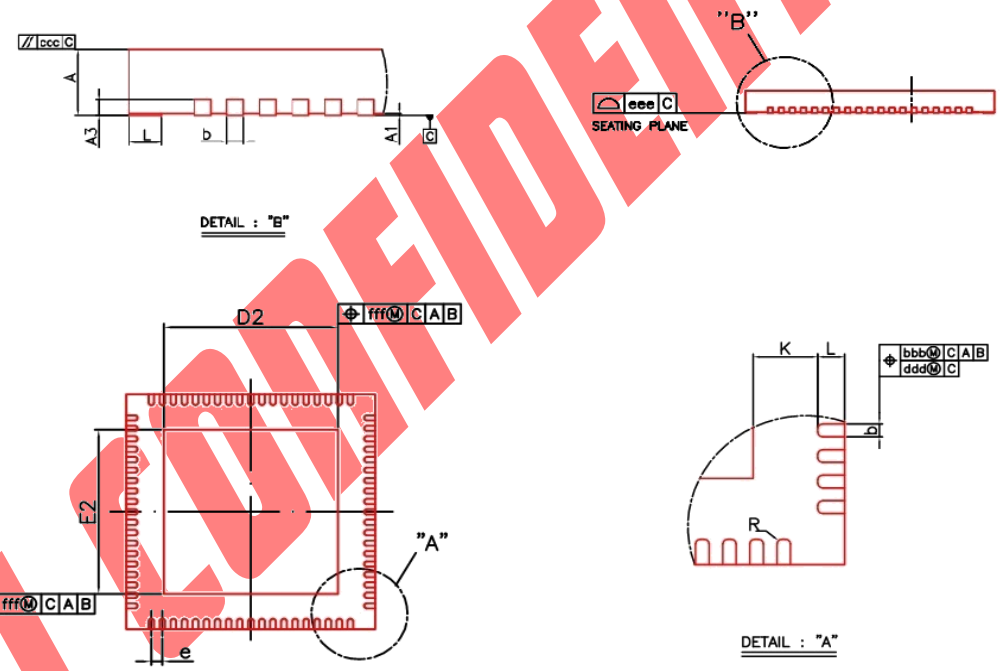


Figure 11 – Mechanical Specification – Q5 (QFN 56L 7x7x0.85 mm) Package

Package Top Side Marking & Ordering Information

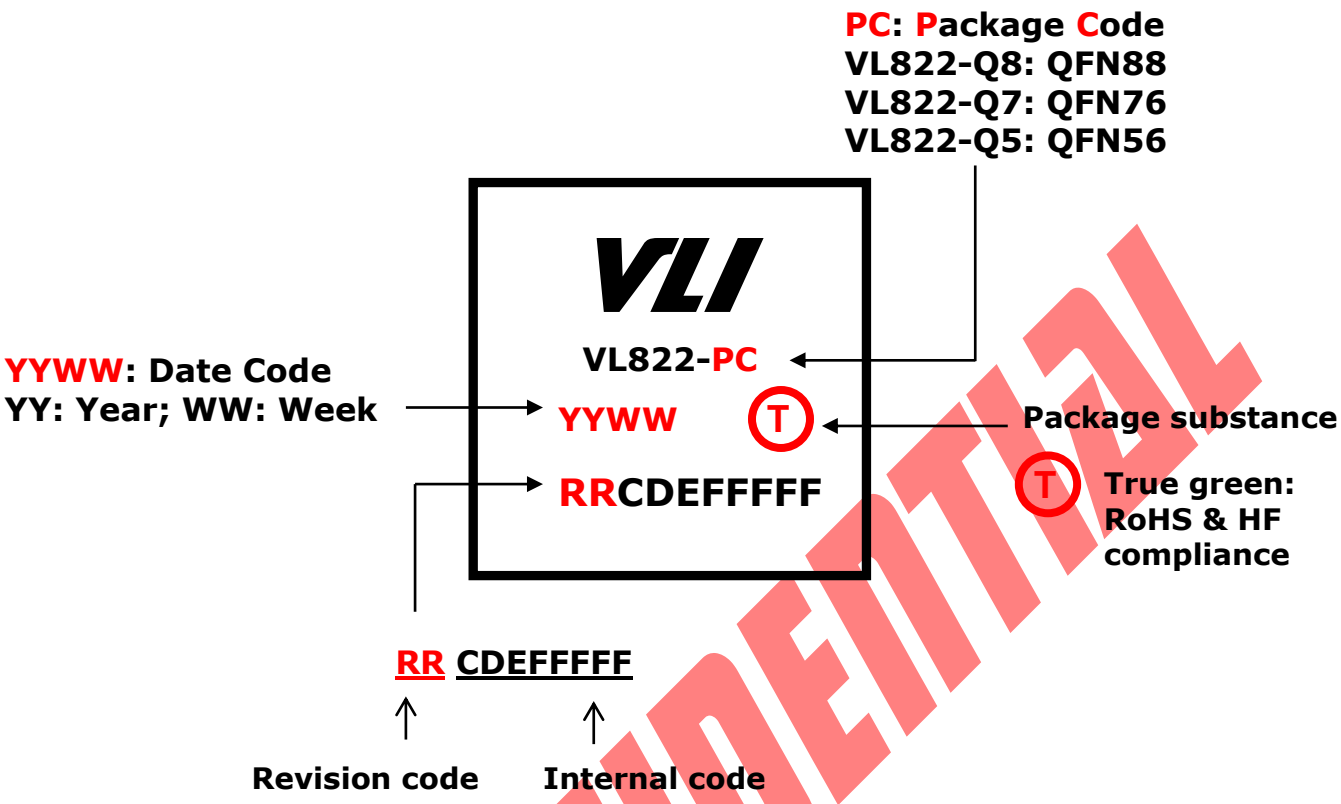


Figure 12 –Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

VIA Labs, Inc.
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