VIA Labs, Inc.

Data sheet

VL171
4x6 USB Type-C Alternate Mode MUX

Aug. 16, 2021

Revision 0.9

Revision History

Rev	Draft Date	History	Initial
0.90	08/16/2021	Preliminary Release	TH

Contents

List of Figures

Product Feature

VL171
4x6 USB Type-C Alternate Mode MUX

- Compatible with 10 Gbps USB3.2 Gen2 and AM all 4Ch Video based on control pin VASEL, including DP1.4 8.1 Gbps
- VCC = 3.3V ± 10% single power supply
- Low power consumption with 2.3mA active and 12.3uA shutdown
- High DC common mode voltage supporting to 2.0V
- 28 pins QFN package
- ESD > 2KV, CDM > 500V

Function Block Diagram

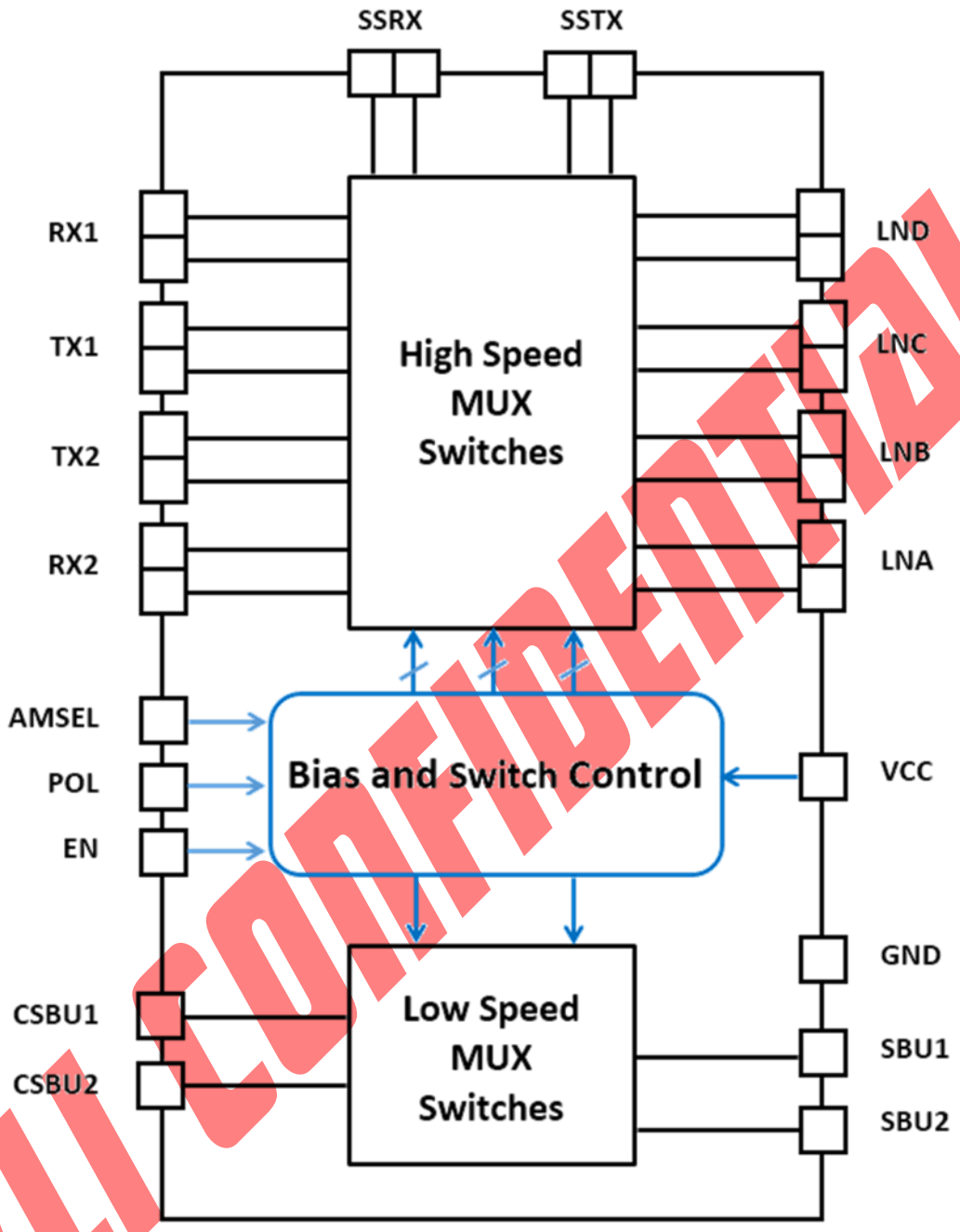


Figure 1 - Block Diagram

Pinout

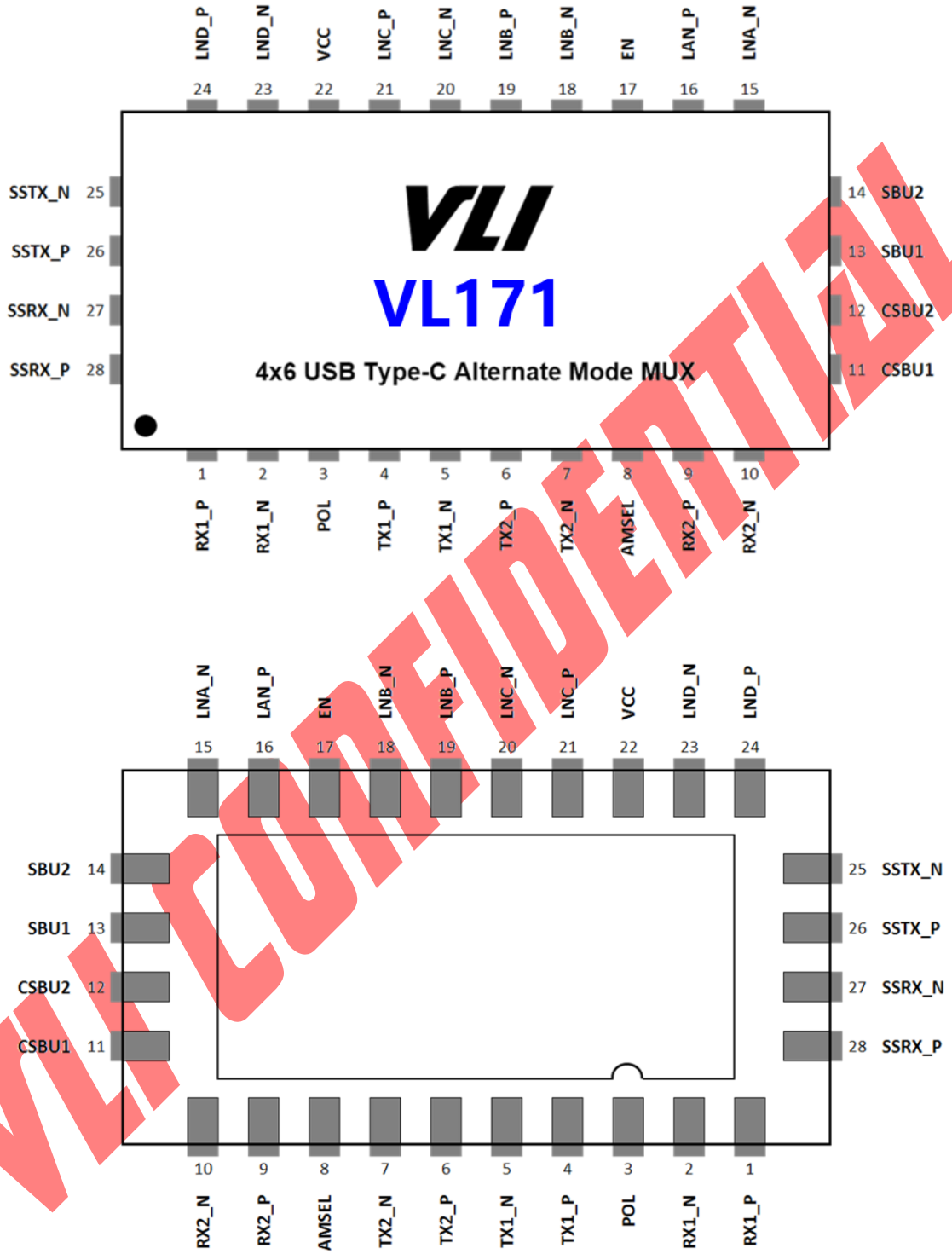


Figure 2 - Pin Diagram (QFN-28)

Pin List

Pin	Pin Name	Pin	Pin Name
1	RX1_P	15	LNA_N
2	RX1_N	16	LNA_P
3	POL	17	EN
4	TX1_P	18	LNB_N
5	TX1_N	19	LNB_P
6	TX2_P	20	LNC_N
7	TX2_N	21	LNC_P
8	AMSEL	22	VCC
9	RX2_P	23	LND_N
10	RX2_N	24	LND_P
11	CSBU1	25	SSTX_N
12	CSBU2	26	SSTX_P
13	SBU1	27	SSRX_N
14	SBU2	28	SSRX_P

Pin Descriptions

Pin Name	Pin #	I/O	Type	Description
RX1_P	1	I/O	Analog	High speed differential signal
RX1_N	2			
POL	3	I	Two Level	MUX control signal
TX1_P	4	I/O	Analog	High speed differential signal
TX1_N	5			
TX2_P	6	I/O	Analog	High speed differential signal
TX2_N	7			
AMSEL	8	I	Three Level	MUX control signal
RX2_P	9	I/O	Analog	High speed differential signal
RX2_N	10			
CSBU1	11	I/O	Analog	Low speed analog signal
CSBU2	12	I/O	Analog	Low speed analog signal
SBU1	13	I/O	Analog	Low speed analog signal
SBU2	14	I/O	Analog	Low speed analog signal
LNA_N	15	I/O	Analog	High speed differential signal
LNA_P	16			
EN	17	I	Three Level	MUX control signal and the whole chip enable control signal
LNB_N	18	I/O	Analog	High speed differential signal
LNB_P	19			
LNC_N	20	I/O	Analog	High speed differential signal
LNC_P	21			
VCC	22	PWR	Power	3.3V power
LND_N	23	I/O	Analog	High speed differential signal
LND_P	24			
SSTX_N	25	I/O	Analog	High speed differential signal
SSTX_P	26			
SSRX_N	27	I/O	Analog	High speed differential signal
SSRX_P	28			
VSSA		GND	Ground	All ground down bond

Application Diagram

For USB Host & DP Source

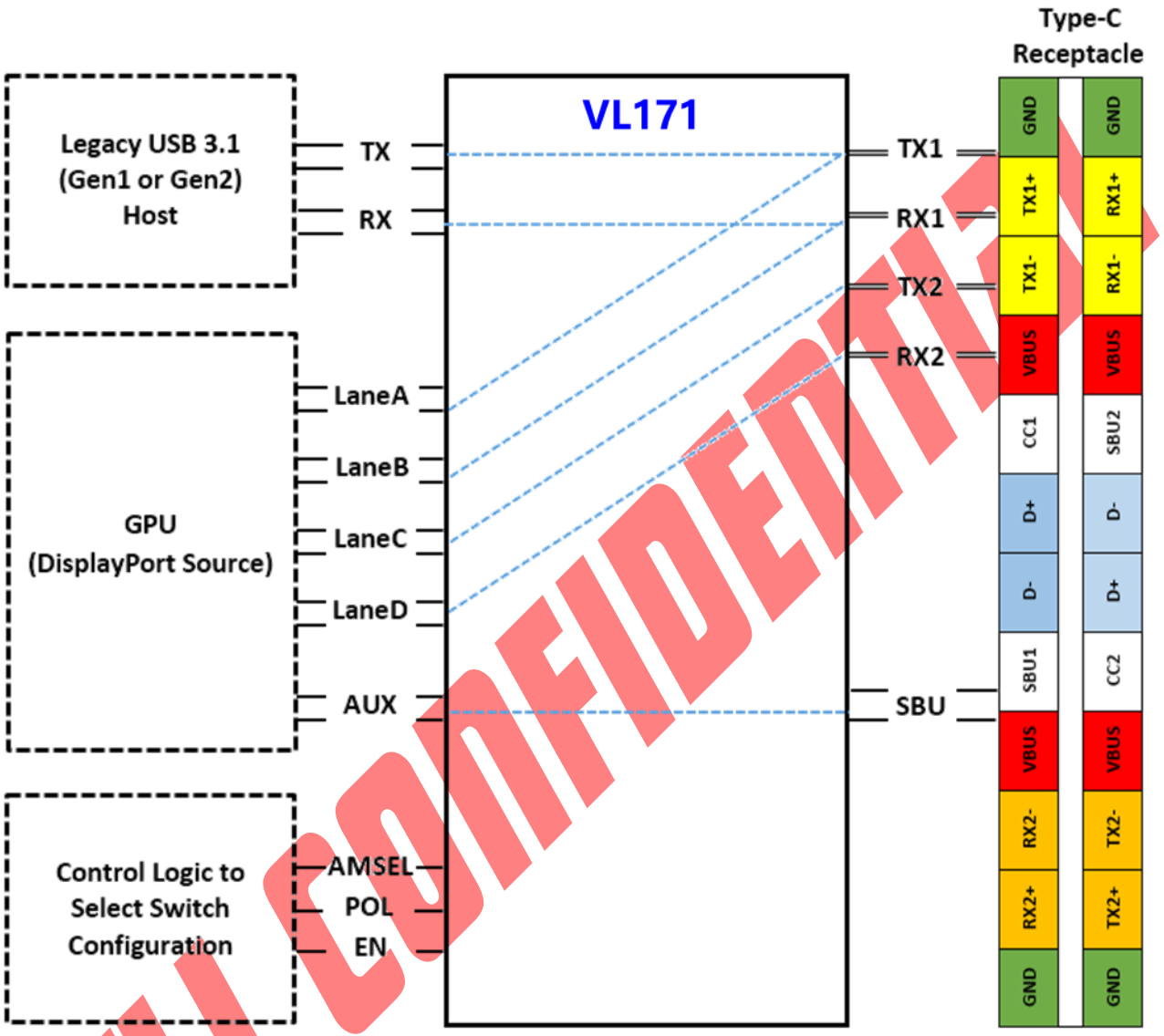


Figure 3 - Application for USB Host & DP Source

For USB Device/HUB & DP Sink

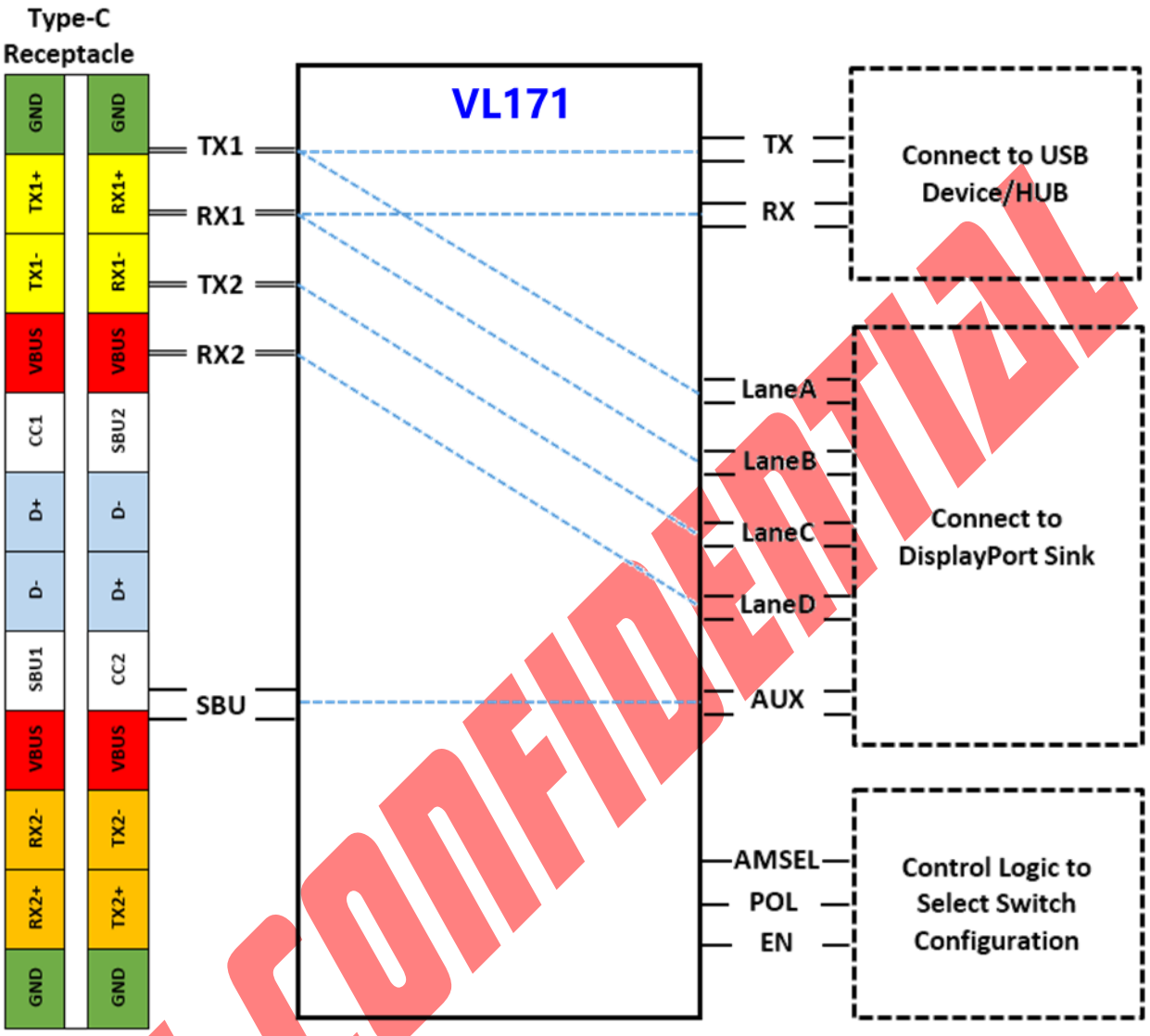


Figure 4 - Application for USB Device/HUB & DP Sink

Function Description

High speed differential signal switch

RL = 50Ω, AC performance (worse case, tt 60°C)

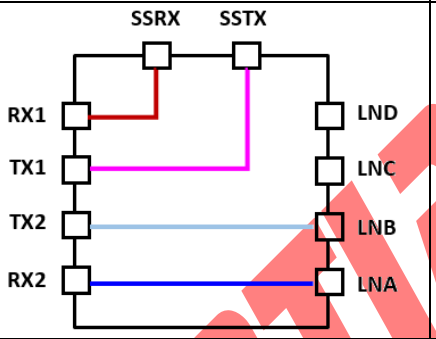
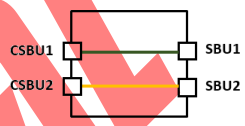
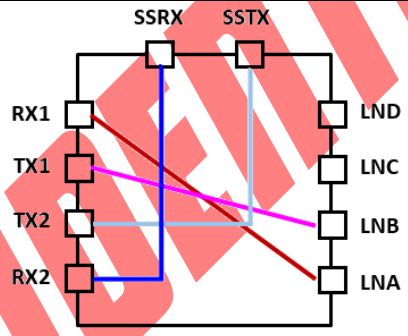
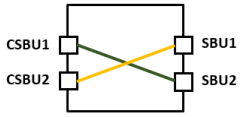
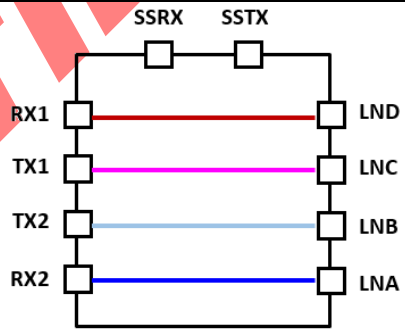
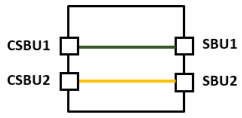
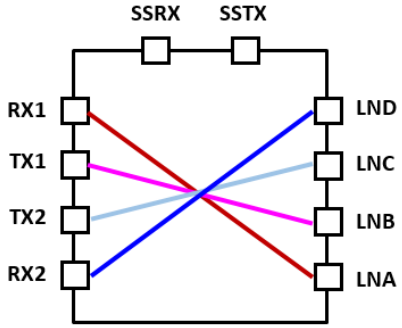
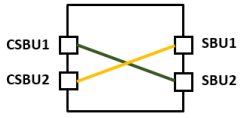
Parameter		Min.	Typ.	Max.	Unit
Differential Insertion loss	@100MHz for SS path		-0.82		dB
	@2.5GHz for SS path		-1.36		
	@5GHz for SS path		-1.82		
Differential Return loss	@100MHz for SS path		-21.1		dB
	@2.5GHz for SS path		-12.6		
	@5GHz for SS path		-12.5		
Differential Off Isolation	@100MHz		-59		dB
	@2.5GHz		-31		
	@5GHz		-26.9		
Differential Crosstalk between SSTX and SSRX	@100MHz		-85.6		dB
	@2.5GHz		-50.4		
	@5GHz		-40		

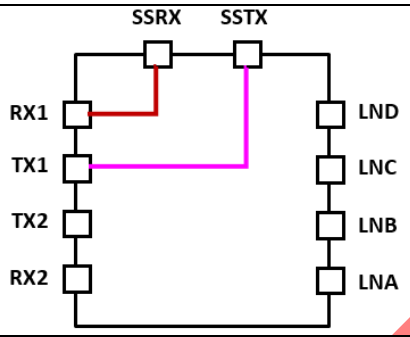
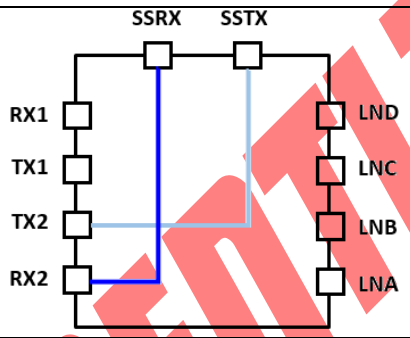
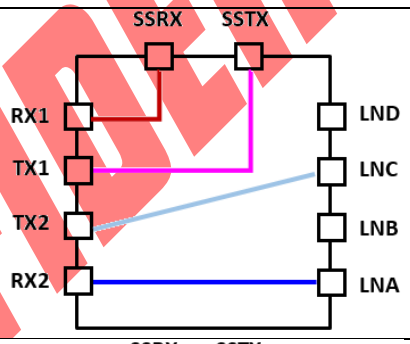
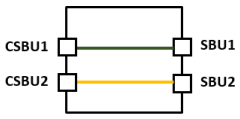
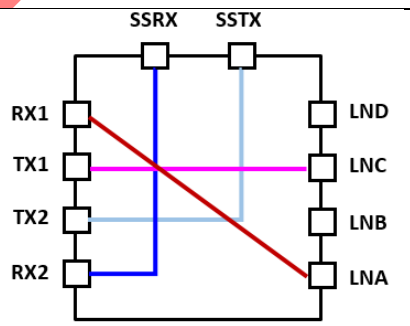
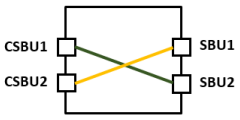
Low speed differential signal switch

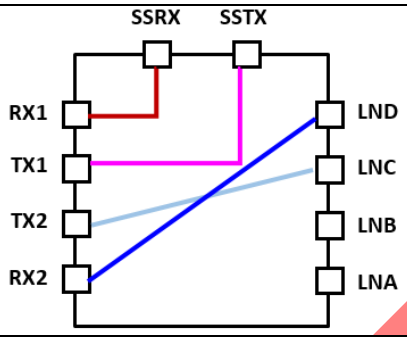
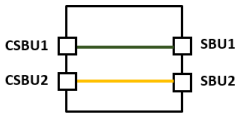
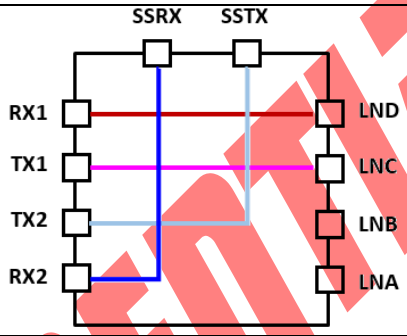
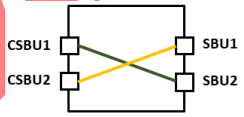
Parameter			Measurement with 100Ω	Unit
		VCOM(V)		
Differential Insertion loss	@100Mhz for LS path	0	-0.68	dB
		1	-0.73	
		2	-0.84	
Differential Return loss	@100Mhz		-20	dB
Low-speed switch –3 dB BW			2000	MHz

Look-up table for Switch connection configuration

The three level detectors sense the input voltage of EN, POL and AMSEL, and configure the signal pass paths.
The active current consumption 2.3mA and 12.3uA after EN = 0.

POL	AMSEL	EN	Configurations	High Speed Signal Flow	SBU Signal Flow
L	L	H	2CH USBSS+ 2CH AM (normal)		
H	L	H	2CH USBSS+ 2CH AM (flipped)		
L	H	H	4CH AM(normal)		
H	H	H	4CH AM(flipped)		

POL	AMSEL	EN	Configurations	High Speed Signal Flow	SBU Signal Flow
L	M	H	2CH USBSS(normal)		All Low Speed SBU Ports HiGHz
H	M	H	2CH USBSS(flipped)		All Low Speed SBU Ports HiGHz
L	M	M	2CH USBSS+ 2CH AM (normal)		
H	M	M	2CH USBSS+ 2CH AM (flipped)		

POL	AMSEL	EN	Configurations	High Speed Signal Flow	SBU Signal Flow
L	L	M	2CH USBSS+ 2CH AM from alternate GPU (normal)		
H	L	M	2CH USBSS+ 2CH AM from alternate GPU (flipped)		
L	H	M	Reserved	Reserved	Reserved
H	H	M	Reserved	Reserved	Reserved
X	X	L	OFF	OFF	OFF

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter		Min	Max	Unit	Note
T_{STG}	Storage Temperature		-40	150	°C	-
V_{ESD}	Electrostatic Discharge		2KV		V	Human Body Model
θ_{jc}	Thermal resistance between junction and case	4L PCB	28.1		°C/W	
		2L PCB	36.7			
Tj	Junction Temperature			125	°C	
P_D	Max Power Dissipation		-	8	mW	

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Items	Descriptions	Test conditions	min	type	max	unit
VCC	Power supply		3	3.3	3.6	V
ICC	Active current			2.3		mA
IQQ	quiescent current			12.3		uA
Vcom	Input common mode voltage		0		2.0	V
VIH	Input high voltage		2.7			V
VIM	Mid-level voltage		VCC/2-0.3	VCC/2	VCC/2+0.3	V
VIL	Input low voltage				0.4	V
Ron_hs	Switch on resistance			10	12	ohm
Ron_ls	Switch on resistance			10	12	ohm
Ron flatness	Ron for different Vcom			1		ohm
Ron mismatch				0.5		ohm
T_A	Ambient Temperature		-25		85	°C

Static characteristics

VDD = 3.3V ± 10 %; Temp = -40°C to +85°C; unless otherwise specified.

Item	Description	Test Condition	Min	Typ.	Max	Unit
VIH	Input high voltage		2.7			V
VIM	Mid-Level voltage		VCC/2 - 0.3	VCC/2	VCC/2 + 0.3	V
VIL	Input low voltage				0.4	V
Ron	Switch on resistance			6	8	Ω
Ron Flatness	Ron for different Vcom			1		Ω
Ron Mismatch				0.5		Ω

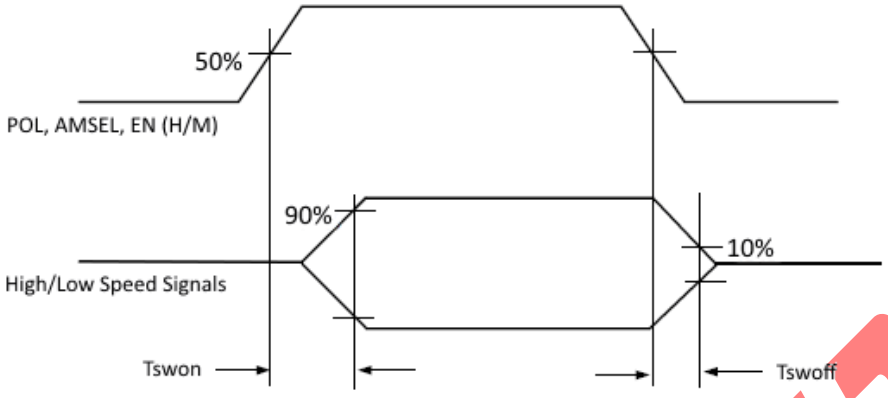
* The flatness is defined as difference of the maximal ON resistance and minimal ON-resistance for the whole voltage throughput domain

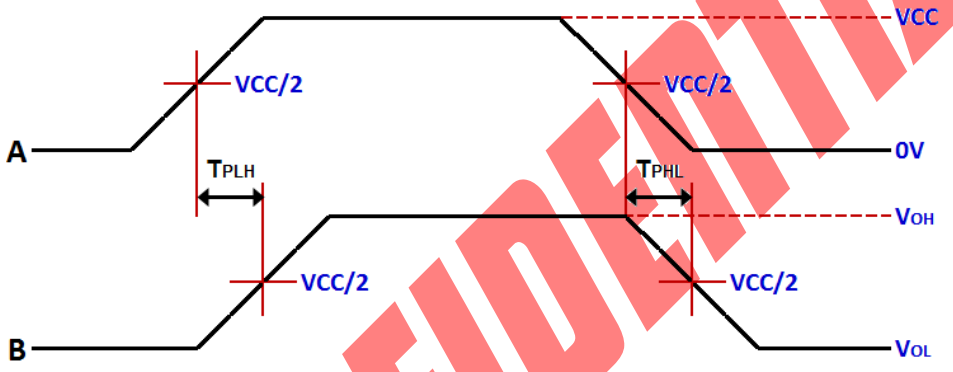
* Ron mismatch defined as the resistance difference of intra channels R(A_IN+ ➔ A_OUT+) and R(A_IN- ➔ A_OUT-)

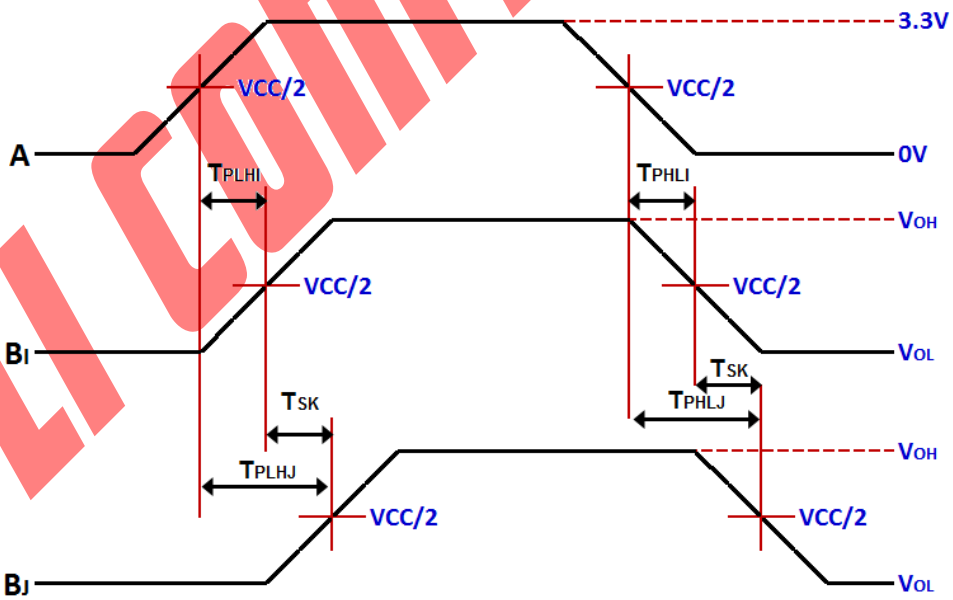
Dynamic characteristics:

TA = -25 ~ 85°C, VCC = 3.3V ± 10 %

Parameter	Description	Min	Typ.	Max	Unit
Tstartup	VCC valid (>85% 3.3V) to channel enable			10	us
Twakeup	Channel enable by changing VEN from VIL to VIH or VIM			120	us
Tswon	Switch turn on time (Twakeup excluded)			5	us
Tswoff	Switch turn off time (Twakeup excluded)			2	us
TPHL, TPLH	Propagation Delay	-	0.1	-	us
TSK	Output Skew between center port to any other port	-	1	30	ps







TSK = |TPLHJ - TPLHI| or = |TPHLJ - TPHLI|

Reflow Profile

Follow: IPC/JEDEC J-STD-020 D.1

Condition
Average ramp-up rate (217°C to peak): 1~2°C /sec max.
Preheat: 150~200C, 60~120 seconds
Temperature maintained above 217°C: 60~150 seconds
Time (tp)* within 5 °C of the specified classification temperature (Tc = (260°C)), (the time above 255°C) ≧ 30 sec.
Peak temperature: 260+5/-0°C
Ramp-down rate: 3°C /sec. max.
Time 25°C to peak temperature: 8 minutes max.
Cycle interval: 5 minus

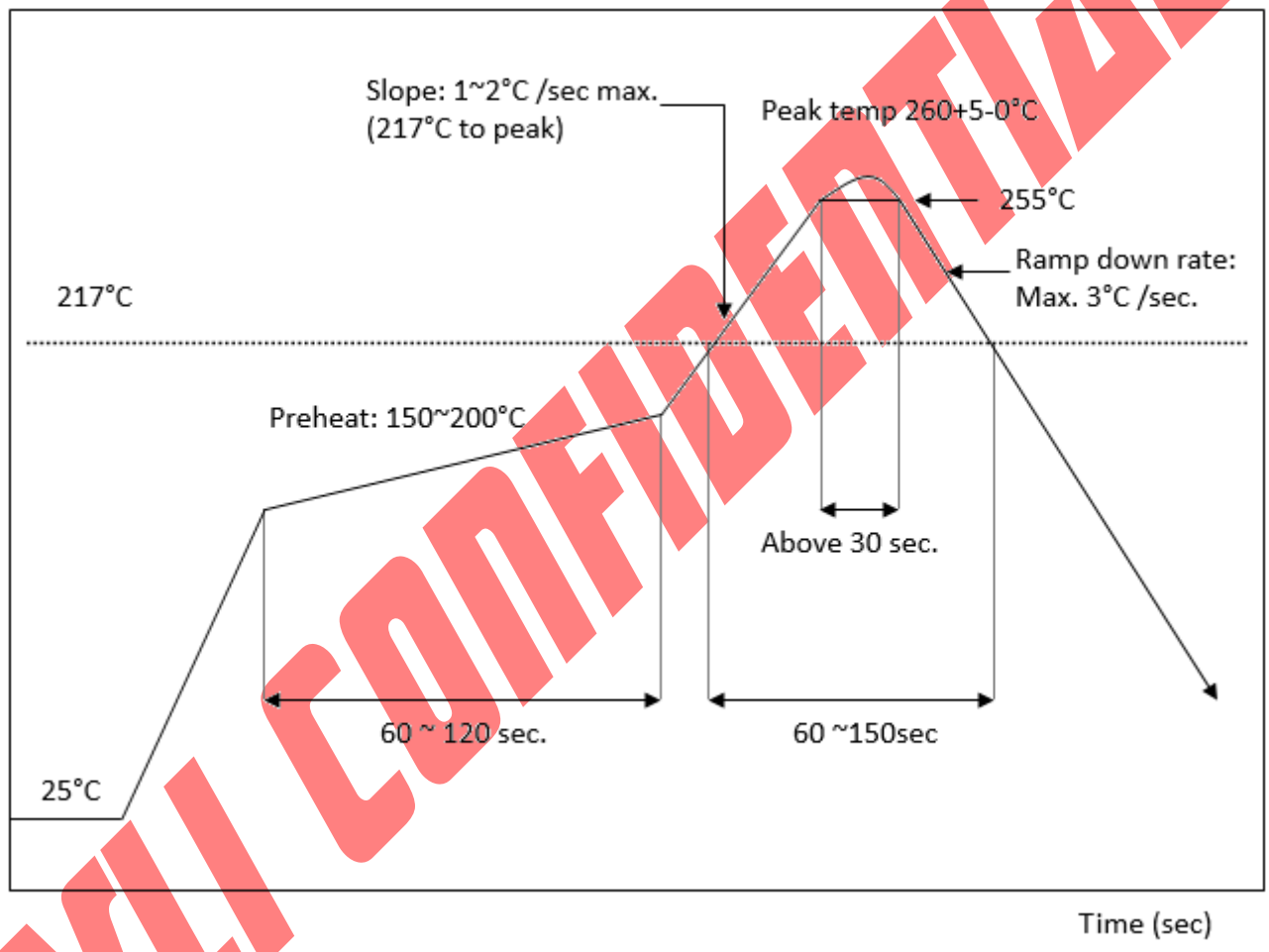
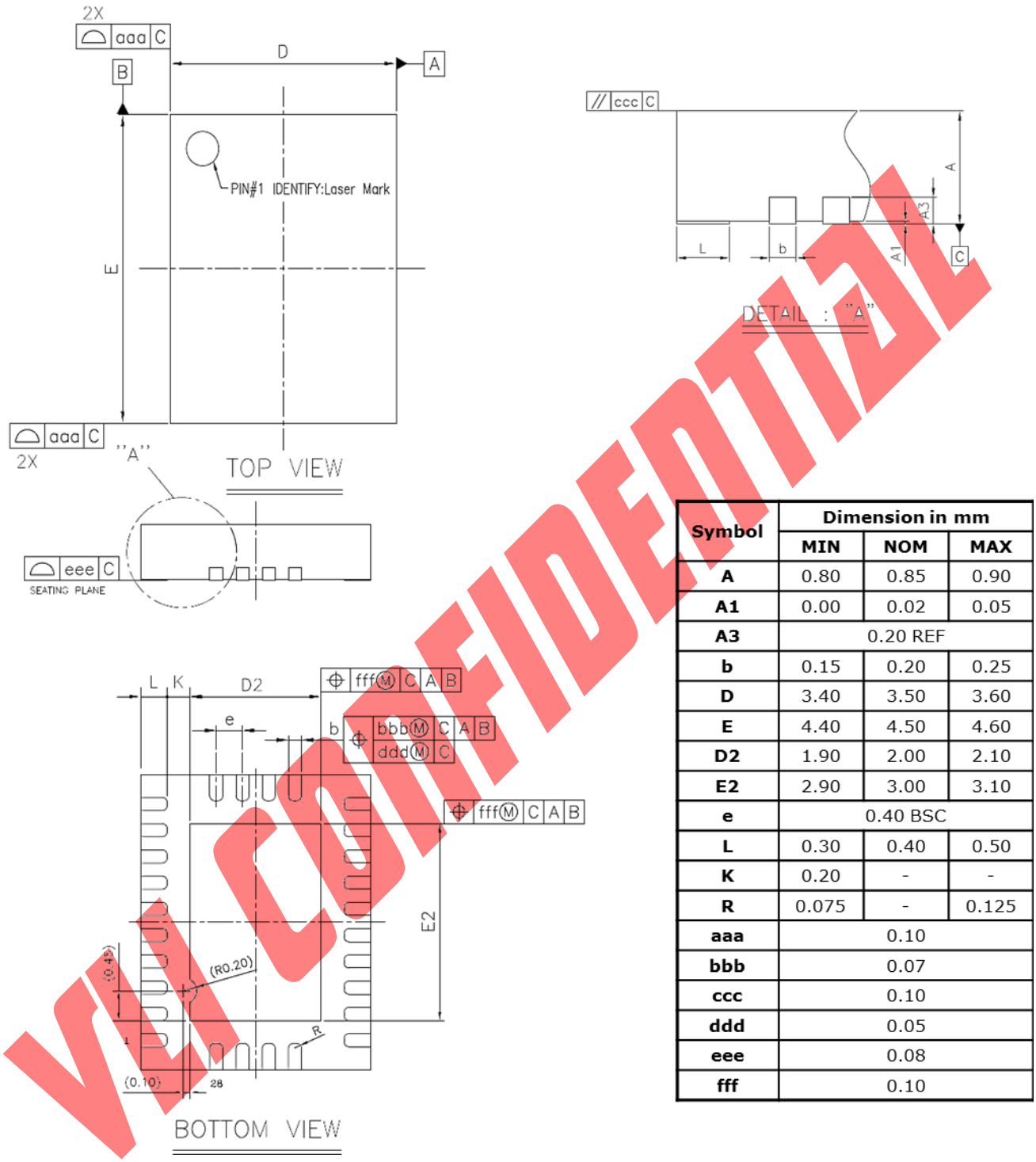


Figure 5 - Reflow

Package Mechanical Specifications



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.40	3.50	3.60
E	4.40	4.50	4.60
D2	1.90	2.00	2.10
E2	2.90	3.00	3.10
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	-	-
R	0.075	-	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 6 - Mechanical Specification

Package Top Side Marking

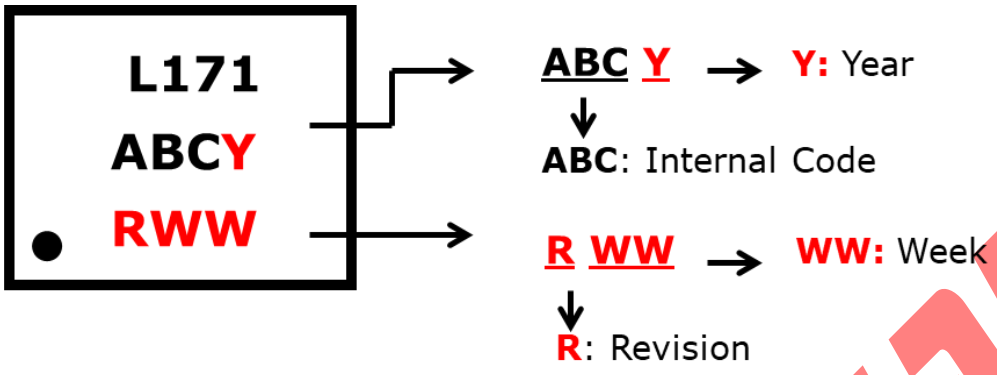
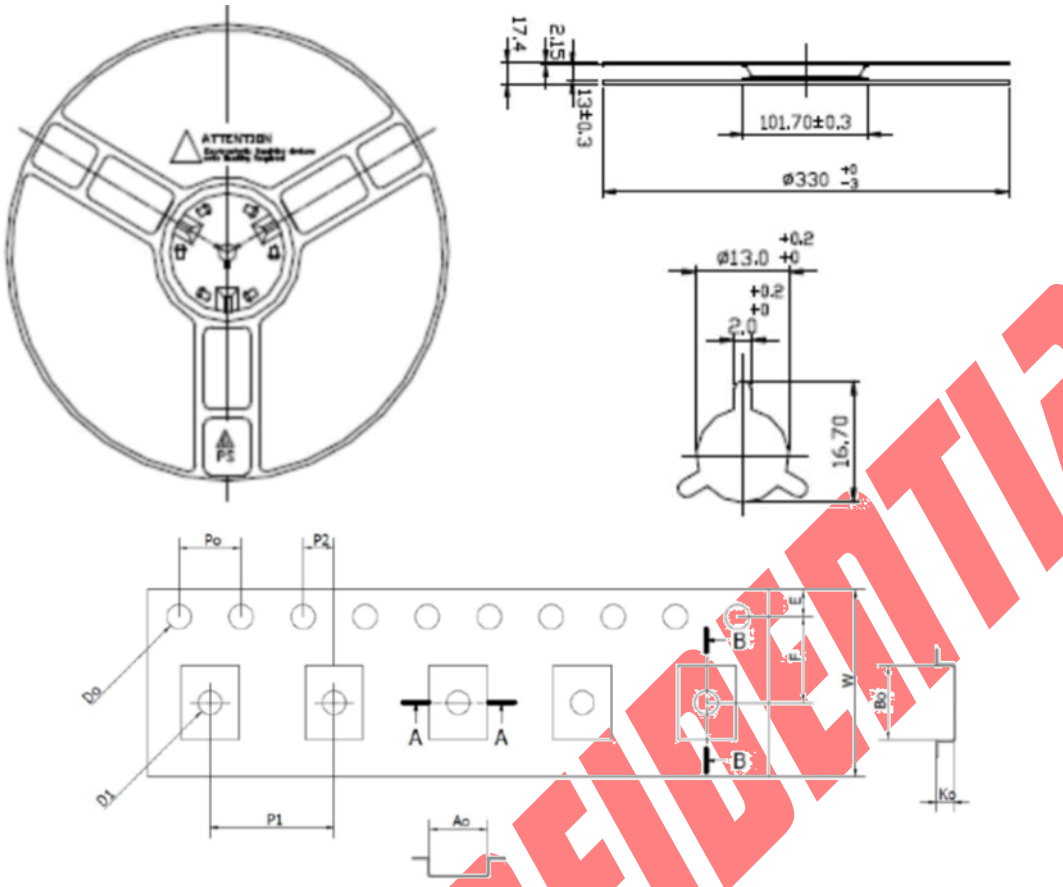


Figure 7 - Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

Tape and Reel Information



Unit: mm		
Symbol	**Spec**	**Tolerance**
A_0	3.75	± 0.10
B_0	4.75	± 0.10
K_0	1.1	± 0.10

Unit: mm		
Symbol	**Spec**	**Tolerance**
P_0	4	± 0.10
P_1	8	± 0.10
P_2	2	± 0.05
D_0	1.55	± 0.05
D_1	1.5	(Min.)
E	1.75	± 0.10
F	5.5	± 0.05
$10P_0$	40	± 0.2
W	12	± 0.2
T	0.25	± 0.05

Figure 8 - Tape and Reel Information

VIA Labs, Inc.
www.via-labs.com
7F, 529-1, Zhongzheng Rd.,
Xindian District, New Taipei City 23148 Taiwan, R.O.C.
TEL: 886-2-2218-1838