YUN-RONG (ALICE) DU

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Education

Columbia University New York, NY
M.S. in Electrical Engineering Expected Dec 2025

- 2024 Nikola Tesla Electrical Engineering Scholar Award.
- Courses: Advanced Logic Design, Digital VLSI Circuits, Analog Electronic Circuit, Power Management IC.

National Taiwan University (NTU) Taipei, TW
B.S.E. in Electrical Engineering June 2024

- Average GPA: 4.12/4.3, 2023 Spring Dean's Award for Academic Excellence.
- **A+** in Digital Circuit Laboratory, Integrated Circuit Design, Computer Architecture, Power Electronics Laboratory.

Skills

- **IC Design** Verilog HDL / FPGA / HSPICE / Cadence Virtuoso / Synopsys Design Vision / Cadence Innovus
- **Programming** C++ / Python / Assembly / Git / Linux

Work Experiences

Micron Taipei, TW
Field Application Engineer Summer Intern July 2024 - Aug 2024

- Performed memory-system compatibility test and issue debug with Intel MRC training and Rank Margining Tool.
- Developed a Python automation tool to compare and summarize multiple testing logs, speeding up test and debug flow by 90% for entire PC DRAM team.

Dell Technologies Taipei, TW
Electrical Engineer Summer Intern June 2023 - Aug 2023

- Built an automation tool with a visualization dashboard, reducing power product management time by 80%.

Projects

Digital System Design: Computer Architecture Feb 2024 - Jun 2024

- Implemented pipelined RISC-V processor with cache, branch prediction, compressed instruction extension, and multiplication instruction with Verilog; tested with Assembly and debugged with nWave.
- Collaborated with a team of three to plan and execute a comprehensive design and testing process, comparing multiple implementations for modules to optimize time and area.
- Secured 1st place in analysis and presentation and enhanced 5% AT^2 performance over baseline.

Integrated Circuit Design: Image-Processing Engine Feb 2023 - Jun 2023

- Completed image processing functions such as image load, shift, blur, and max/min/median filter in kernel.
- Went through entire frontend and backend design flow, including Verilog coding, Synthesis with Design Vision, and Automatic Place & Route (APR) with Innovus, achieving 70% improvement on AT^2 over baseline.

Digital Circuit Laboratory: Image Processing for Counting Sep 2022 - Jan 2023

- Initiated an FPGA project for fast object detection and counting, getting streaming video from camera through UART, storing it in SDRAM, and displaying results on screen using the VGA protocol.
- Achieved image recognition on streaming pixels using the Blob detection algorithm and Connected Component Analysis (CCA), obtaining the number of objects within one second.

NTUEE (National Taiwan University Electrical Engineering) Light Dance [link] Dec 2021 - Mar 2023

- Studied protocols and wrote a C++ library for LED control, resolving aberration issues during brightness decay and enhancing signal transmission speed between RPi, microcontroller STM32, and LED strips.
- Designed and drew the PCB layout for control circuits and conducted hardware validation for ten systems.

Activities

NTU for FRC (National Taiwan University for FIRST Robotics Competition) Taipei, TW
Director and Volunteer Jan 2021 - Dec 2022

- Initiated the club to train undergraduate students as STEM educators and support FRC teams in Taiwan.
- Led a team of 10 people to give lectures and hold workshops for five high schools to promote STEM education.
- Volunteered as the Control System Advisor in 2022 FRC New Taipei City x Hon Hai Regional.