Square Root Raised Cosine FIR Filter

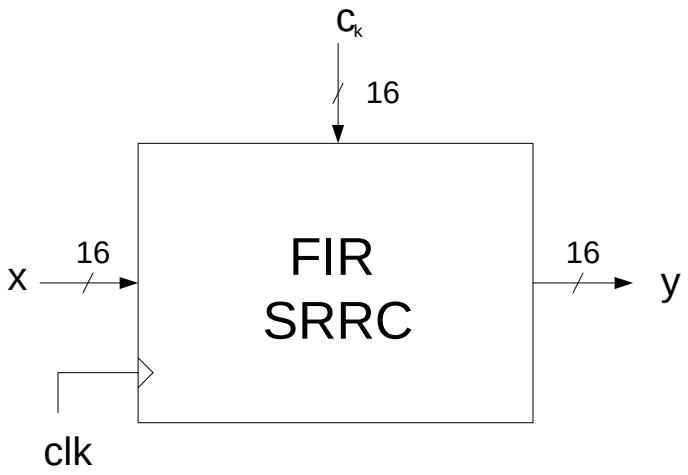
Design a digital circuit that realises a FIR (Finite Impulse Response) filter with a SRRC (Square Root Raised Cosine) impulse response and with the following characteristics:

- Order of the filter N = 22
- Samples per symbol = 4
- A roll-off factor of 0.5

$$y[n] = \sum_{i=0}^{N} c_i \cdot x[n-i]$$

For inputs, outputs and coefficients, use a 16-bit representation.
The following values can be used for the coefficients c_k : $c_0 = c_{22} = -0.0165$; $c_1 = c_{21} = -0.0150$; $c_2 = c_{20} = 0.0155$; $c_3 = c_{19} = 0.0424$; $c_4 = c_{18} = 0.0155$; $c_5 = c_{17} = -0.0750$; $c_6 = c_{16} = -0.1568$; $c_7 = c_{15} = -0.1061$; $c_8 = c_{14} = 0.1568$; $c_9 = c_{13} = 0.5786$; $c_{10} = c_{12} = 0.9745$; $c_{11} = 1.1366$.

The interface of the circuit to be designed is as follows:



You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions