Assignment 8

Extra 1: Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

Extra 1.1 For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

Extra 1.2 For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

Extra 1.1

Word Address	Binary Address	Tag	Index	Hit/Miss
3	0000 0011	0	3	M
180	1011 0100	11	4	M
43	0010 1011	2	11	M
2	0000 0010	0	2	M
191	1011 1111	11	15	M
88	0101 1000	5	8	M
190	1011 1110	11	14	M
14	0000 1110	0	14	M
181	1011 0101	11	5	M
44	0010 1100	2	12	M
186	1011 1010	11	10	M
253	1111 1101	15	13	M

Extra 1.2

Word Address	Binary Address	Tag	Index	Hit/Miss
3	0000 0011	0	1	M
180	1011 0100	11	2	M
43	0010 1011	2	5	M
2	0000 0010	0	1	H
191	1011 1111	11	7	M
88	0101 1000	5	4	M
190	1011 1110	11	7	H
14	0000 1110	0	7	M
181	1011 0101	11	2	H
44	0010 1100	2	6	M
186	1011 1010	11	5	M
253	1111 1101	15	6	M

Class instructor's explanation:

Extra 1.1

Direct mapped, one –word block, 16 blocks

This means that there are 16 cache locations (each can hold one word) and the cache mechanism only moves one word at a time.

When the first word comes (word 3, with binary address 0000 0011), the cache mechanism checks its least significant 4 bit (which is 0011) to determine its corresponding cache location/address. The rest bits (0000) are used as Tag. In this problem, all words ended with a miss status. The most obvious reason for this problem is that there are no repeated words. Please be careful. When you do have repeated words, there is no guarantee that you will have a hit (you still need to go through the process and examine the cache's Valid bit and Tag field to determine whether there are valid hits).

Extra 1.2

The only difference is the arrangement of the cache. Now, the cache, which still holds 16 words, has 8 blocks with 2-word in each block. Since each block holds 2 words, the cache mechanism moves 2 words at a time. When the first word comes (word 3), the cache mechanism not only moves it, but also moves word 2 at the same time.The motivation for this design is to take advantage of the principle of Spatial Locality. The assumption is that if you use word 3 this time, there is a good chance that you may need word 2 (which is a neighbor of word 3) in the near future. Please note that this is still a direct map cache (not an associative cache).

Since we only have 8 blocks (locations) in the cache, we only need 3 bits as the index. When the word 3 (with binary address 0000 0011) comes, the cache mechanism takes the address bits of bit 1, 2, and 3 (that is 001) as the index. It is important to note that bit 0 will not be used as part of the index. Please note that in this problem, the cache mechanism is designed to take two words at the same time. In this case, it will also take the word 2 (with binary address 0000 0010) along. This is the reason why later on, when word 2 request comes, it is a hit. As for the tag field, sure enough, the rest of the higher bits will be used as the Tag.