CPSC 440 Computer System Architecture
Spring 2024
Department of Computer Science
California State University, Fullerton
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Special Request (please help me out – thanks in advance):
My email box receives too many emails. It becomes very difficult to manage (and I may miss your email). When you mail me, please visit Canvas first and use Canvas email to email me your message. Please don't use your regular email (for example, Yahoo mail, Gmail, CSUF Gmail, to email me). This allows me to clearly see emails from my classes (typically, I have more than 100 students per semester). I understand that this will take you one or two minutes to open Canvas first. I appreciate your help and consideration (your one minute may save me 100 minutes).

Prerequisites: CPSC 240

Catalog Description: Computer performance, price/performance, instruction set design, and examples. Processor design, pipelining, memory, hierarchy design, and input/output subsystems.

Text:
"Computer Organization & Design – the hardware/software interface," by D. A. Patterson and J. L. Hennessy. Fifth Edition, Morgan Kaufmann Publishers, Inc.
Other materials will be posted online.

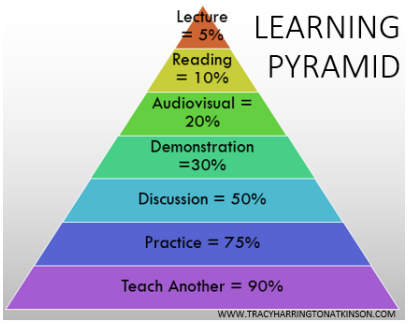
Tentative Schedule
(tentative, may change later)
In addition to MIPS and ARM, please note that some new lectures related to RISC-V (and some hands-on RISC-V demonstrations) may be added after Week 8.

Week	Reading materials	Group Discussion
1 (1/22/2024)	Chapter 1- Computer Abstractions and Technology	Monday: Whole class event (Orientation) Wednesday: Whole class event (Orientation – continue)

2 (1/29/2024)	Chapter 2 - Instructions: Language of the Computer	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
3 (2/5/2024)	Chapter 2- Instructions: Language of the Computer	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
4 (2/12/2024)	Chapter 3- Arithmetic for Computers	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
5 (2/19/2024)	Chapter 3- Arithmetic for Computers	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
6 (2/26/2024)	Chapter 4- The Processor	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
7 (3/4/2024)	Chapter 4- The Processor (continue)	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
8 (3/11/2024)	Chapter 4- The Processor (continue)	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
9 (3/18/2024)	Midterm on Monday 3/20/2024 Midterm Results on Wednesday, 3/20/2024 (Mandatory)	Whole Class Event for the entire week (everyone needs to attend)
10 (3/25/2024)	Chapter 4- The Processor (continue)	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
11 (4/1/2024)		Spring Recess
12 (4/8/2024)	Chapter 5 - Large and Fast: Exploiting Memory Hierarchy	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
13	Chapter 5 - Large and	Monday (Groups 1 and 2)

(4/15/2024)	Fast: Exploiting Memory Hierarchy	Wednesday (Groups 3 and 4)
14 (4/22/2024)	Interrupt and Exception	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
15 (4/29/2024)	Multicore vs. Multiprocessor	Monday (Groups 1 and 2) Wednesday (Groups 3 and 4)
16 (5/6/2024)	Final Exam Preview	Monday, 5/6/2024 – Whole class event (everyone needs to attend, Mandatory) Wednesday, 5/8/2024 - Individual consultation (attendance is NOT mandatory)
17 (5/13/2024)	Final Exam Week	In-class, in-person final exam (Mandatory)

All lectures (mp4 and slides) are available on Canvas. The class time will be reserved for small group discussions. Attendance is mandatory.



Please be aware that six meetings may (or may not) become asynchronous/synchronous online (per the university policy). Will announce the dates soon.

Grading Policy:
Homework assignments and forum discussions (effort-based): 20%
Group Project: 10%

Attendance: 10% (missing three classes will receive 0%)
Midterm: 30%
Final: 30%

Grades will be assigned at the highest category achieved as follows:

A+:	>=97%
A:	>=93%
A-:	>=90%
B+:	>=87%
B:	>=83%
B-:	>=80%
C+:	>=77%
C:	>=73%
C-:	>=70%
D:	>=60%
F:	< 60%

Grading Rubric:
Midterm and final exam come with their own grading rubric.

Homework Assignment and forum discussion - Effort-based, one point each. Reasonable effort – one point, Lack of effort – zero point

No late assignments accepted (no exceptions)

There are no make-ups for missed exams. No extra credit will be given.

Attending class is mandatory.

Lectures: All lectures are posted on Canvas.
The class time will mostly be dedicated to Group Discussions.

Discussion Assignments: (Will Post Later)

Homework Assignments:

Assignment_ 1

2.1) Convert the following C code to MIPS code. Assume that the variables f, g, h, and i are given and could be considered 32-bit integers.
F=g + (h-5)

2.2) For the following MIPS statements, what is the corresponding C statement?
add f, g, h
add f,i, f

2.5) Show how the value 0xabcdef12 would be arranged in memory of a little-endian and a big-endian machine. Assume the data is stored starting at address 0.

2.7
Translate the following C code to MIPS code. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4 respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7 respectively. Assume that the elements of the arrays A and B are 4-byte words:

B[8] = A[i] + A[j];

Assignment_2

2.10
Assume that registers $s0 and $s1 hold the values 0x80000000 and 0xD0000000, respectively.

2.10.1
What is the value of $t0 for the following assembly code?
add $t0, $s0, $s1

2.10.2
Is the result in `$t0` the desired result, or has there been overflow?

2.10.3
For the contents of registers `$s0` and `$s1` as specified above, what is the value of `$t0` for the following assembly code?

```
sub $t0, $s0, $s1
```

2.10.4
Is the result in `$t0` the desired result, or has there been overflow?

2.10.5
For the contents of registers `$s0` and `$s1`as specified above, what is the value of `$t0` for the following assembly code?

```
add $t0, $s0, $s1
add $t0, $t0, $s0
```

2.10.6
Is the result in `$t0` the desired result, or has there been overflow?

2.12
Provide the type and assembly language instruction for the following binary value:
`0000 0010 0001 0000 1000 0000 0010 0000two`

2.13
Provide the type and hexadecimal representation of following instruction:
`sw $t1, 32($t2)`

2.22.2
Suppose the program counter (PC) is set to `0x2000 0000`.
What range of addresses can be reached using the MIPS branch if equal (beq) instructions? (In other words, what is the set of possible values for the PC after the branch instruction executes?)

Extra 1:
Write the MIPS assembly code that creates the 32-bit constant `0010 0000 0000 0001 0100 1001 0010 0100two` and stores that value to register `$t1`.

Extra 2:
If the current value of the PC is `0x00000000`, can you use a single jump instruction to get to the PC address as shown in Extra 1?

Assignment_3

3.1 What is 5ED4 -07A4 when these values represent unsigned 16-bit hexadecimal numbers? The result should be written in hexadecimal. Show your work.

3.2 What is 5ED4 -07A4 when these values represent signed 16-bit hexadecimal numbers stored in sign-magnitude format? The result should be written in hexadecimal. Show your work.

3.3 Convert 5ED4 into a binary number. What makes base 16 (hexadecimal) an attractive numbering system for representing values in computers?

3.7 Assume 185 and 122 are signed 8-bit decimal integers stored in sign-magnitude format. Calculate 185 -122. Is there overflow, underflow, or neither?

3.9 Assume 151 and 214 are signed 8-bit decimal integers stored in two's complement format. Calculate 151+214 using saturating arithmetic. The result should be written in decimal. Show your work.

3.10 Assume 151 and 214 are signed 8-bit decimal integers stored in two's complement format. Calculate 151-214 using saturating arithmetic. The result should be written in decimal. Show your work.

3.20 What decimal number does the bit pattern **0×0C000000** represent if it is a two's complement integer? An unsigned integer?

3.21 If the bit pattern 0×0C000000 is placed into the Instruction Register, what MIPS instruction will be executed?

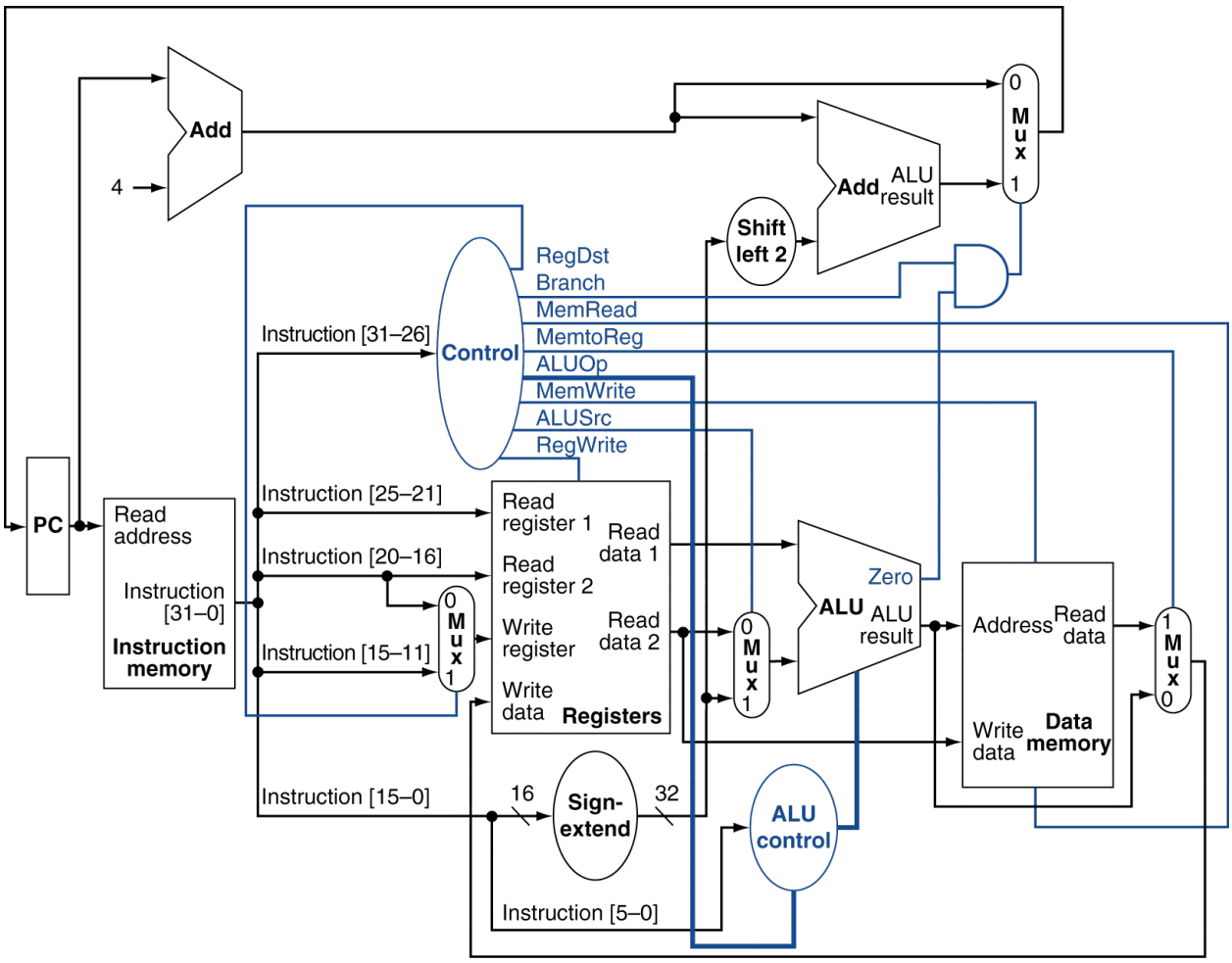
3.22 What decimal number does the bit pattern 0×0C000000 represent if it is a floating point number? Use the IEEE 754 standard.

Assignment_4

3.23
Write down the binary representation of the decimal number 63.25 assuming the IEEE 754 single precision format.
3.25 Write down the binary representation of the decimal number 63.25 assuming it was stored using the single precision IBM format (base 16, instead of base 2, with 7 bits of exponent).

3.41 Using the IEEE 754 floating point format, write down the bit pattern that would represent -1/4. Can you represent -1/4 exactly?

Assignment 5



Consider the following instruction:
Instruction: AND Rd, Rs, Rt
Interpretation: Reg[Rd] = Reg[Rs] AND Reg[Rt]

Extra 1 What are the values of control signals generated by the control in Figure shown above for this instruction?

Extra 1.1 Which resources (blocks) perform a useful function for this instruction?

Extra 1.2 Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

Extra 2: When processor designers consider a possible improvement to the processor data path, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with a data path from Figure 4.2, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively. Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the

latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

Extra 2.1 What is the clock cycle time with and without this improvement?

Extra 2.2 What is the speedup achieved by adding this improvement?

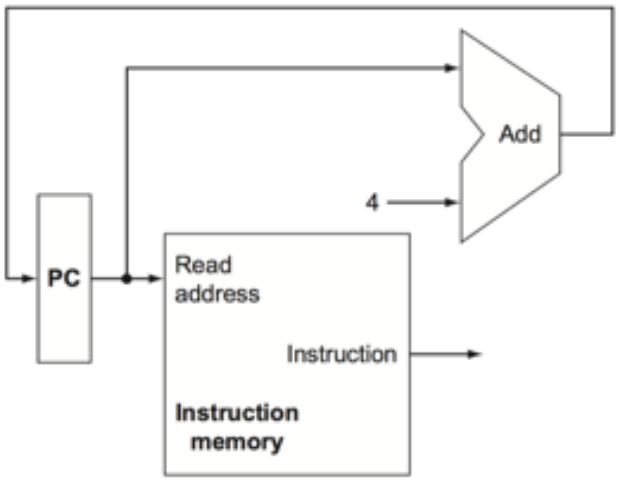
Extra 2.3 Compare the cost/performance ratio with and without this improvement.

Assignment_6

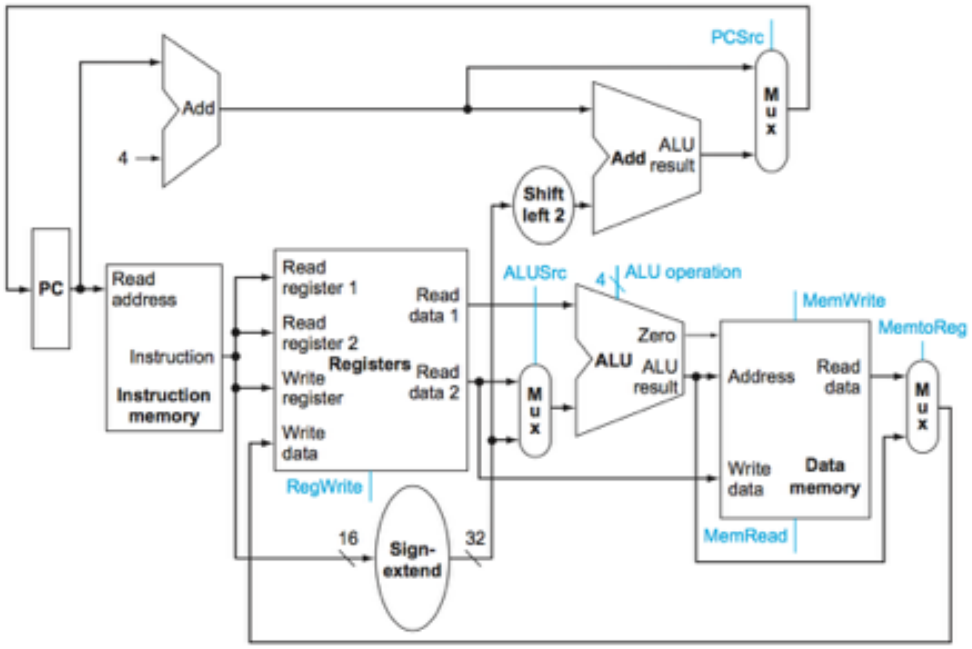
Extra 1 In this exercise assume that logic blocks needed to implement a processor's datapath have the following latencies:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

If the only thing we need to do in a processor is fetch consecutive instructions (Figure 4.6), what would the cycle time be?



Extra 2 Consider a datapath similar to the one in Figure 4.11, but for a processor that only has one type of instruction: unconditional PC relative branch. What would the cycle time be for this datapath?



Extra 3 [10] <§4.3> Repeat Extra 2, but this time we need to support only conditional PC-relative branches.

Assignment_7

Extra 1: The three problems in this exercise refer to the datapath element Shift-Left-2:

Extra 1.1 Which kinds of instructions require this resource?

Extra 1.2 For which kinds of instructions (if any) is this resource on the critical path?

Extra 1.3 Assuming that we only support beq and add instructions, discuss how changes in the given latency of this resource (Shift-Left-2) affect the cycle time of the processor. Assume that the latencies of other resources do not change.

Assignment 8

Extra 1: Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.
3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

Extra 1.1 For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.
Extra 1.2 For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

Academic Dishonesty Policy (for your reference)

Academic dishonesty includes but is not limited to cheating on examinations or assignments, unauthorized collaboration, plagiarism, falsification/fabrication of university documents, any act designed to give unfair academic advantage to the student (such as, but not limited to, submission of essentially the same written assignment for two courses without the prior permission of the instructor), assisting or allowing any of these acts, or the attempt to commit such acts.

Cheating is defined as the act of obtaining or attempting to obtain credit for work by the use of any dishonest, deceptive, fraudulent, or unauthorized means. Examples of cheating include, but are not limited to, the following: using notes or aides or the help of other students on tests and examinations in ways other than those expressly permitted by the instructor, plagiarism as defined below, tampering with the grading procedures, and collaborating with others on any assignment where such collaboration is expressly forbidden by an instructor. Violation of this prohibition of collaboration shall be deemed an offense for the person or persons collaborating on the work, in addition to the person submitting the work. Documentary falsification includes forgery, altering of campus documents or records, tampering with grading procedures (including submitting altered work for re-grading), fabricating lab assignments, or altering or falsifying medical excuses or letters of recommendation.

Plagiarism is defined as the act of taking the work (words, ideas, concepts, data, graphs, artistic creation) of another whether that work is paraphrased or copied in verbatim or near verbatim form and offering it as one's own without giving credit to that source. When sources are used in a paper, acknowledgment of the original author or source must be made through appropriate citation/attribution and, if directly quoted, quotation marks or indentations must be used. Improper acknowledgment of sources in essays, papers, or presentations in prohibited.

The initial responsibility for detecting and dealing with academic dishonesty lies with the instructor concerned. An instructor, who believes that an act of academic dishonesty has occurred, is obligated to discuss the matter with the student (s) involved. The instructor should possess reasonable evidence with respect thereto, such as documents or personal observation. In this meeting, and throughout the process, every effort should be made to preserve the integrity of the educational relationship between instructor and student. The student should be given the opportunity to respond to the complaint. If the violation is discovered during the offering or grading of the final exam, the instructor may assign a mark of "RP" until the instructor has an opportunity for such a meeting. Also because the student may challenge the allegation, he or she must be allowed to attend all classes and complete all assignments until the appellate process is complete. When necessary, such discussion may be conducted by telephone or electronic mail.

However, if circumstances prevent consultation with student(s), the instructor may take whatever action (subject to student appeal) he/she deems appropriate. An instructor who is convinced by the evidence that a student is guilty of academic dishonesty, shall:

1. Assign an appropriate academic penalty, including, but not limited to: oral reprimand; "F" or "O" on the assignment; grade reduction on assignment or course; or "F" in the course. Factors to take into consideration in assigning a grade sanction include: normative sanctions for comparable acts, severity of the offense (academic gain or potential academic gain if the action had gone undetected), harm or potential harm to other students in the class, premeditation of the act.
2. Report to the student(s) involved, to the department chair, and to the Dean of Students Office, Judicial Affairs, the alleged incident of academic dishonesty, including relevant documentation, actions taken by the instructor including grade sanction, and recommendations for additional action that he/she deems appropriate. The written report should be distributed as soon as possible, preferably within 15 calendar days from discovery, but not later than 30 calendar days after the first day of classes of the regular semester (fall or Summer) following the grade assignment.

The Dean of Students Office, Judicial Affairs, shall maintain a disciplinary file for each case of academic dishonesty with the appropriate documentation. Students shall be informed that a disciplinary file has been established and that they have an opportunity to appeal the actions of the instructor under the Academic Appeals Policy. Dean of Students Office, Judicial Affairs may initiate disciplinary proceedings under Title 5, Section 41301 and Executive Order 970. Sanctions which may be assessed include but are not limited to: warning, probation, educational sanctions, removal from academic program, suspension, expulsion, denial of admission or enrollment in university classes including Extended Education.

When two or more incidents involving the same student occur, the Dean of Students Office, Judicial Affairs shall initiate disciplinary proceedings. A student may appeal any sanction assessed for a charge of academic dishonesty under UPS 300.030, "Academic Appeals." If the Academic Appeals Board accepts the student's appeal then the disciplinary file will be purged. If a student does not

appeal the instructor's action or if the Academic Appeal Boards rejects the student's appeal the disciplinary file will be maintained in a confidential file in the Dean of Students Office, Judicial Affairs for a minimum of seven years. Disciplinary probation and suspension are noted on the student's academic record during the term of the probation or suspension. A permanent notation will be made on a student's academic record if he or she is expelled from the university. A second academic integrity violation usually results in suspension from the university for a period of time.

In order to facilitate due process and to insure that a student knows that academic dishonesty is subject to action, this policy shall be published in the Catalog and Student Handbook. Copies of this policy shall also be available in every department office, the Dean of Students Office, and in the Office of the Vice President for Student Affairs.

Disabled Student Services: (from: http://www.fullerton.edu/DSS/handbook/DSSGenInfo.htm)

In compliance with CSU policy, students with disabilities may be found eligible for one or more of the following services from DSS:

- Diagnostic assessment, including both individual and group assessment not otherwise provided by the institution, to determine educational functioning or to verify specific disabilities;
- Disability-related counseling and advising, including specialized academic, vocational, personal and peer counseling that is developed specifically for students with disabilities and is not duplicated by regular counseling and advisement services available to all students;
- Interpreter services, including manual, steno and oral interpreting for hearing-impaired students;
- Reader services to coordinate and provide access to information required for equitable academic participation, if this access is not available in other suitable modes;
- Test-taking facilitation, including adapting tests for and proctoring tests taken by students with disabilities;
- Transcription services, such as providing Braille and large print materials not available through other sources;
- Notetaker services for writing, note-taking, and manual manipulation for classroom and related academic activities;
- Access to, and arrangements for, adaptive educational equipment and technology, materials and supplies;
- Liaisons with campus and community agencies, including referral and follow-up services with these agencies on behalf of students with disabilities;
- On-campus and off-campus registration assistance, including priority registration, assistance with applications for financial aid and related college services;
- Disabled Person (DP) parking, including on-campus parking registration, temporary parking permit arrangements, and application assistance for students who do not have state disabled person placards or license plates;
- Access to the Computer Access Lab with specially designed hardware and software to accommodate various disabilities;
- Activities to coordinate and administer specialized services, including consultation with faculty for students with special academic needs associated with their disabilities;
- Activities to assess the planning, implementation and effectiveness of these services and programs;
- Activities to increase general campus awareness of students with disabilities.

Each semester, DSS provides students with an Accommodation Letter for each class requested. In order for students to receive the appropriate accommodations in their classes, students must present a current Accommodation Letter to each of their professors at the beginning of the semester, or at such time as the disability is verified.

Upon presentation by the student of a current Accommodation Letter professors are obliged to comply with the prescribed academic adjustments stated therein.

Computer Access Lab

This facility provides computer support services for CSUF students, faculty and staff with disabilities who need access to computers to become more independent and productive in their work. CAL offers one-to-one training on IBM-compatible computers, technical support and consulting, and public-access workstations. Alternative computer access systems include voice recognition, speech synthesis, screen readers, screen magnification and large displays, computer-based Braille translation and embossing, computer-based reading machines, closed circuit television magnification systems, and a variety of devices to accommodate special seating and positioning needs.

The Computer Access Lab is located within Disabled Student Services, UH-101. A separate entrance is provided through the double doors in the northeast corner of the building. Further information is available at (657) 278-5397 (657) 278-5397

Emergency Procedures

For your own safety and the safety of others, each student is expected to read and understand the guidelines published at «http://prepare.fullerton.edu/campuspreparedness/». Should an emergency occur, follow the instructions given to you by faculty, staff, and public safety officials. An emergency information recording is available by calling the Campus Operation and Emergency Closure line at 657-278-4444.