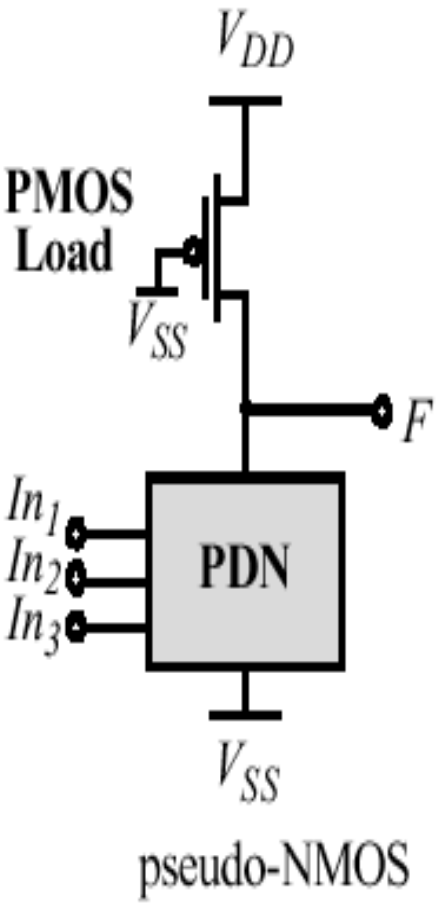
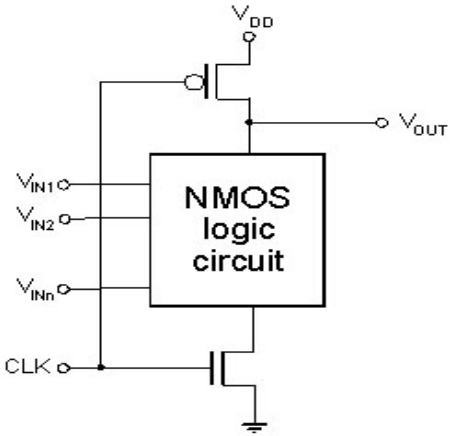
Pseudo nMOS Logic

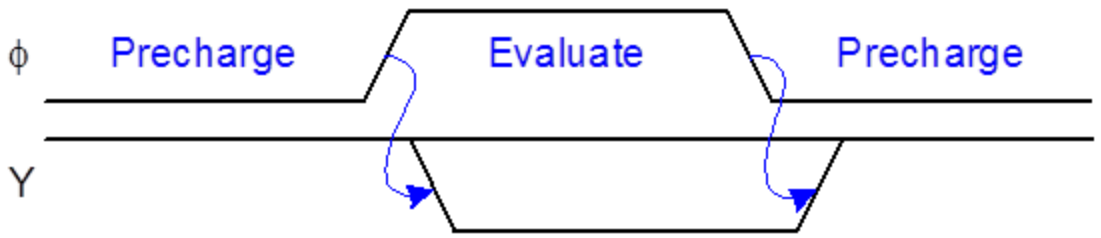


Using a PMOS transistor simply as a pull-up device for an n-block is called pseudo-NMOS logic. In this type of logic the transistor widths must be chosen properly, i.e., The pull-up transistor must be chosen wide enough to conduct a multiple of the n-block's leakage and narrow enough so that the n-block can still pull down the output safely.

The advantage of pseudo-NMOS logic are its high speed (especially, in large-fan-in NOR gates) and low transistor count. On the negative side is the static power consumption of the pull-up transistor as well as the reduced output voltage swing and gain, which makes the gate more susceptible to noise. Furthermore, when the gate of the pull-up transistor is connected to a appropriate control signal it can be turned off, i.e., pseudo-NMOS supports a power-down mode at no extra cost.

Dynamic CMOS





When the clock is low, the NMOS device is cutoff while the PMOS is turned ON. This has the effect of disconnecting the output node from ground while simultaneously connecting the node to VDD. Since the input to the next stage is charged up through the PMOS transistor when the clock is low, this phase of the clock is known as the **'precharge'** phase. When the clock is high however, the PMOS is cutoff and the bottom NMOS is turned ON, thereby disconnecting the output node from VDD and providing a possible pull-down path to ground through the bottom NMOS transistor. This part of the clock cycle is known as the '**evaluation**' phase, and so the bottom NMOS is called the 'evaluation NMOS.'

When the clock is in the evaluation phase, the output node will either be maintained at its previous logic level or discharged to GND. In other words, the output node may be selectively discharged through the NMOS logic structure depending upon whether or not a path to GND is formed due to inputs of the NMOS logic block. If a path to ground is not formed during the evaluation phase, the output node will maintain its previous voltage level since no path exists from the output to VDD or GND for the charge to flow away.

OR YOU Can understand from this:

The dynamic gate works or operates in two phases: Precharge phase and evaluation. During the precharge phase, the clock input is low, turning off the NMOS device and switching on the PMOS device, this pulls the output high, as there is no path from the output to the ground.

During evaluation the clock input is high, turning the PMOS transistor off and switching on the NMOS transistor. In this case the output of the device depends on the inputs.

According to the precharge rule there should be no active path from the output to the ground during the precharge cycle, otherwise there will be a dissension between the PMOS precharge transistor and the NMOS transistors pulling to ground, consuming excess power and leaving the output at indeterminate value.

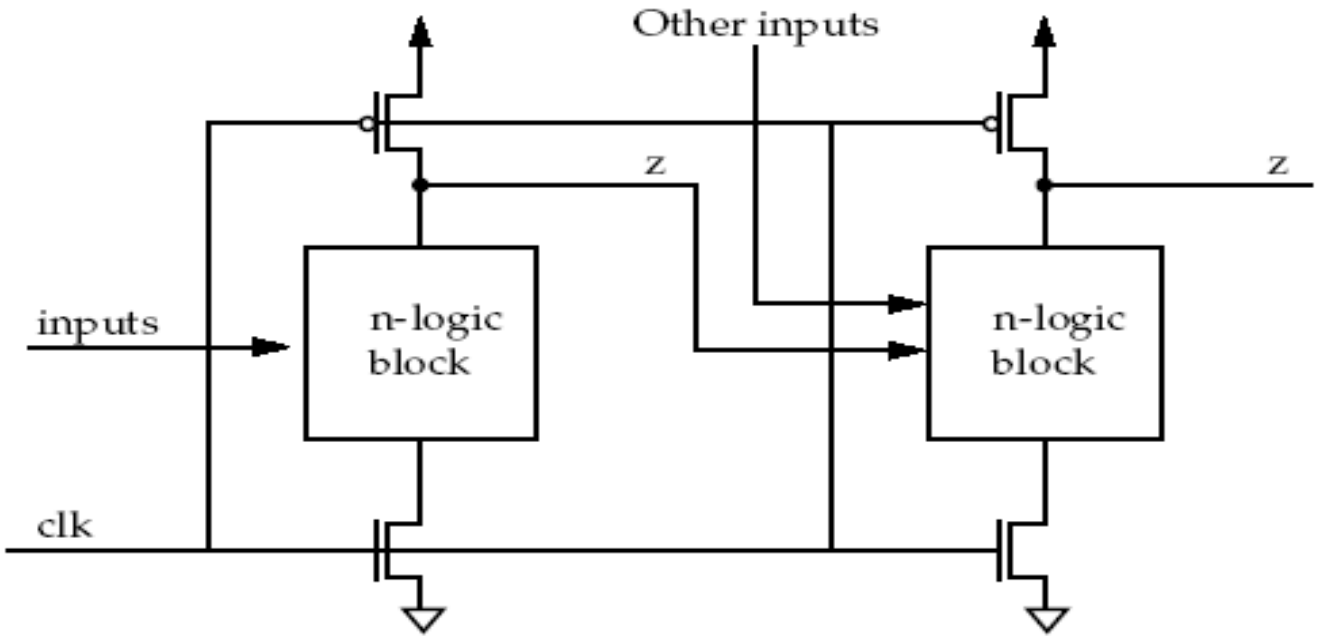
There are many advantages to using dynamic CMOS logic over static CMOS logic or Pseudo NMOS logic.

The elimination of the complimentary PMOS transistors significantly reduces the surface area needed to implement the various logic functions not only because the physical number of transistors is nearly cut in half, but because the physical size of the PMOS transistors tend to be much larger than the size of an NMOS transistor.

The switching speeds are also increased using the dynamic logic configuration since the speed bottleneck caused by the lengthier time the PMOS requires to pull-up the output node is eliminated. Since this node is already precharged high through the PMOS during the precharge phase, the output node needs only to be selectively discharged during the evaluation phase. Discharging the output node through the NMOS devices is significantly faster than the time needed to charge up the output node through the PMOS device.

CMOS Domino Logic

CMOS domino gates are formed by cascading dynamic gates. This kind of design is referred to as Domino Logic since the pull-down of one stage can conditionally cause the pull-down of succeeding stages and so on like falling dominoes. The number of Domino Logic stages that may be cascaded is limited only by the sum of the total pull-down times in all cascaded logic blocks which must be contained within the evaluation clock phase.



STICK DIAGRAM AND LAYOUT REPRESENTATION

Stick diagrams and layout representation are used to convey layer information through the use of a color code.

The Stick diagrams and layout representation for CMOS are a logical extension of the nMOS style. The exception is yellow is used to identify p-type transistors and wires as depletion mode devices are not used.

Component	Colour	Use
metal 1		power and signal wires
metal 2		power wires
polysilicon		signal wires and transistor gates
n-type diffusion		signal wires, source and drain of transistors
p-type diffusion		signal wires, source and drain of transistors
contact	●	signal connection
via	□	connection between metal layers
insulator	none	-

Metal

Two types of metal are used to represent the supply rails metal1 ( ) or metal2 ( )

Polysilicon

Polysilicon ( ) is used to represent the gate.

n-type diffusion

n-type diffusion ( ) is used to represent the source and drain n-transistors.

p-type diffusion

p-type diffusion ( ) is used to represent the source and drain p-transistors.

Contacts

Contacts (●) are used to represent electrical connections.

Via

Cuts called **vias** are used to make contact between two metal layers

CMOS Joining Rules

	n-type diffusion	p-type diffusion	poly	metal1	metal2
n-type diffusion	✓	✗	1	2	✗
p-type diffusion	✗	✓	1	2	✗
poly	1	1	✓	2	✗
metal1	2	2	2	✓	3
metal2	✗	✗	✗	3	✓

symbol	key
✓	allowed - connection formed

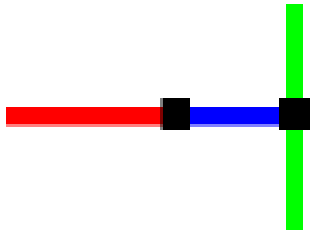
✗	prohibited
1	transistor formed
2	contact needed if connection required, otherwise no connection is made
3	via needed if connection required, otherwise no connection is made

- wherever red cross green an **n-transistors** is formed and **p-transistor** is formed wherever red cross yellow

- When wires of the same type are crossed connection is made even if you don't use contact or via.
- Diffusions of the opposite types cannot cross and contact

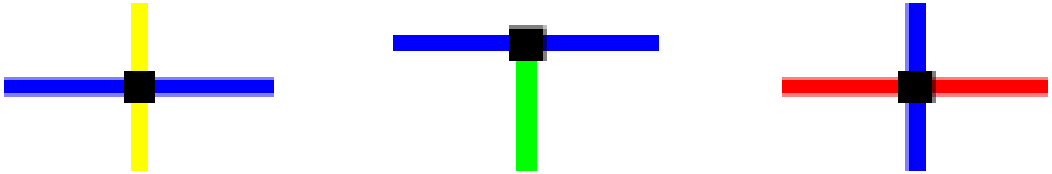
- poly (red) cannot contact n-diff (green) and p-diff (yellow).

- when you want to connect poly (red) to n-diff (green) or p-diff (yellow), you must first connect poly (red) to metal1 (blue) and then metal1 (blue) to n-diff (green) or p-diff (yellow).

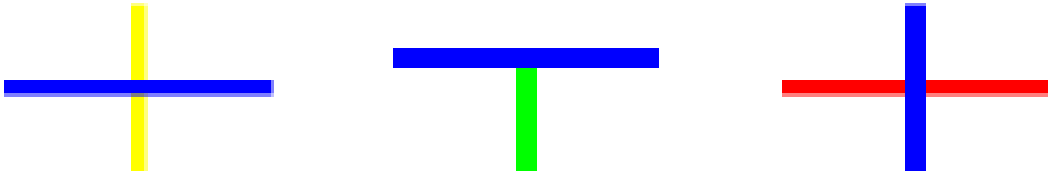


O.K.

- Metal1 (blue) can contact ndiff (green), pdiff (yellow) and poly (red), but remember contact is needed, otherwise no connection is made, even if the layers are crossed



O.K. Connection made.

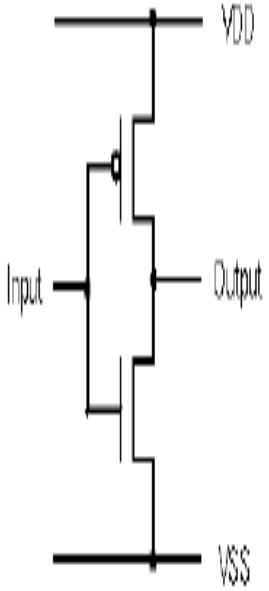


O.K. No connections.

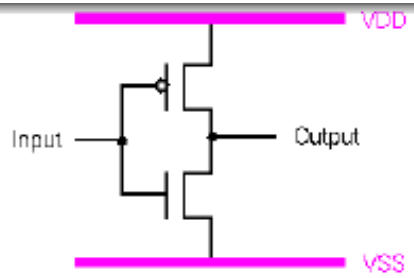
- Metal1 (blue) can contact metal2 (purple), but remember, via is needed, otherwise no connection is made even if the layers are crossed.

4.3 Inverter Stick Diagram

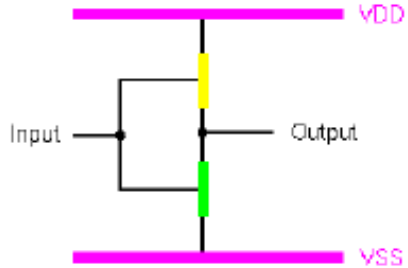
Starting from the circuit diagram of inverter, we can design the stick layout step by step.



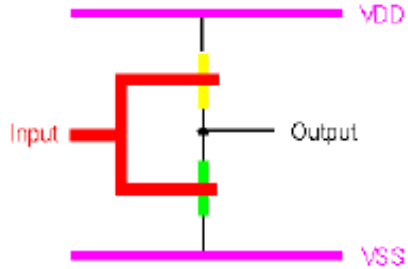
1. Two horizontal wires are used for connection with VSS and VDD. This is done in metal2, but you can decide to use metal1 instead.



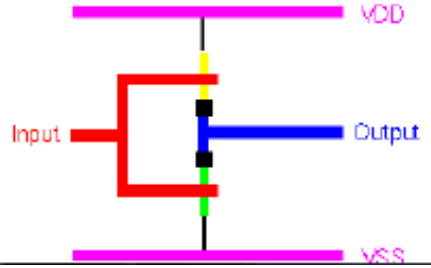
2. Two vertical wires (p-diff and n-diff) are used to represent the p-transistor (yellow) and n-transistor (green).



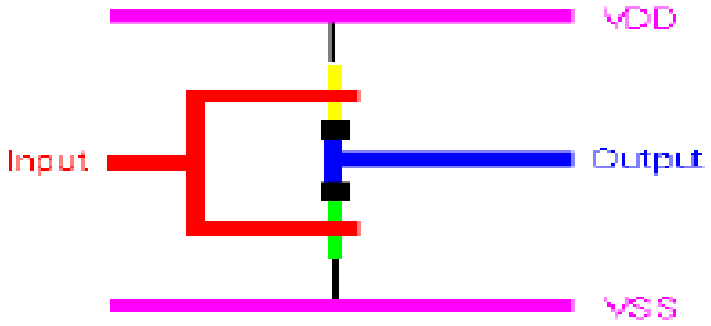
3. Then the gates of the transistors are joined with a polysilicon wire, and connected to the input.



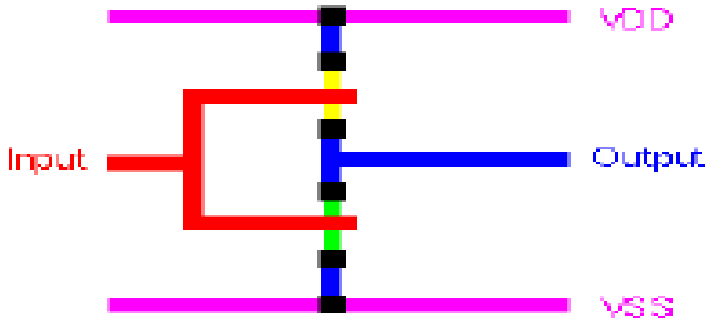
4. The drains of two transistors are then connected with metal1 and joined to the output. There cannot be direct connection from n-transistor to p-transistors.



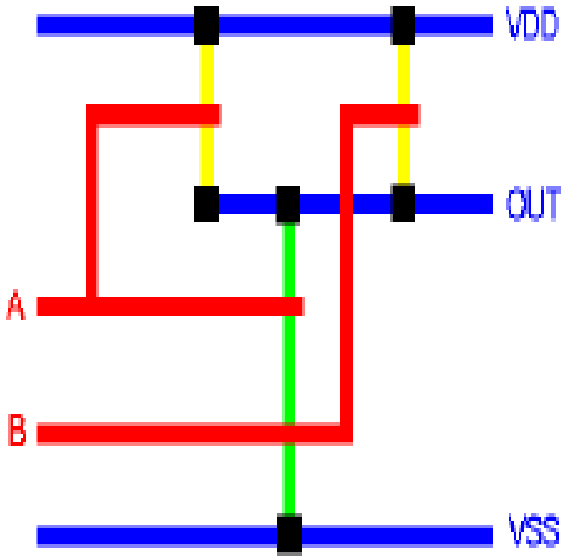
4. The drains of two transistors are then connected with metal1 and joined to the output. There cannot be direct connection from n-transistor to p-transistors.



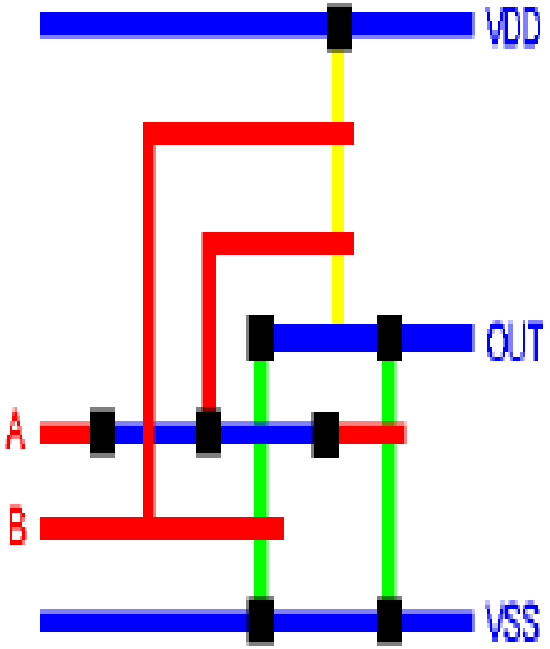
5. The sources of the transistors are next connected to VSS and VDD with metal1. Notice that vias are used, not contacts.



4.4 NAND Gate Stick Diagram



4.5 NOR Gate Stick Diagram



LAYOUT DESIGN RULES

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules.

These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.
If a metal line width is made too small, for example, it is possible for the line to break during the fabrication process or afterwards, resulting in an open circuit.
If two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process.

The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area, for any circuit to be manufactured with a particular process.

we can say, in general, that observing the layout design rules significantly increases the probability of fabricating a successful product with high yield.

The design rules are usually described in two ways :

• Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations, are stated in terms of absolute dimensions in micrometers.

• Lambda rules, which specify the layout constraints in terms of a single parameter (λ) and, thus, allow linear, proportional scaling of all geometrical constraints.

Lambda-based layout design rules were originally devised to simplify the industry- standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda-based design rules must therefore be handled with caution in sub-micron geometries. In the following, we present a sample set of the lambda-based layout design rules devised for the MOSIS CMOS process and illustrate the implications of these rules on a section a simple layout which includes two transistors

SCALING

The size of the circuits in IC's continues to increase. Proper scaling allows to shrink a design.
Technology scaling rate is approximately 13% / year, halving every 5 years.
Besides increasing the number of devices, scaling has had a profound impact on both speed and power.

Full Scaling (Constant Electrical Field Scaling)

In the ideal model, all the dimensions of the MOS devices, e.g., the voltage supply level and depletion widths are scaled by the same factor S.
Keeping the electric field patterns constant avoids breakdown and other secondary effects.
This leads to greater device density, higher speed and reduced power consumption.
Ron remains constant -- performance is improved because of the reduced capacitance.
Circuit speed increases linearly while the power scales down quadratically!
Both clearly indicate the benefits of scaling.

CMOS Subsystem Design Process

General Considerations:

Lower unit cost

Higher reliability

Lower power dissipation, lower weight and lower volume

Better performance

Enhanced repeatability

Possibility of reduced design/development periods

Some Problems

1. How to design complex systems in a reasonable time & with reasonable effort.
2. The nature of architectures best suited to take full advantage of VLSI and the technology
3. The testability of large/complex systems once implemented on silicon

Some Solution

Problem 1 & 3 are greatly reduced if two aspects of standard practices are accepted.

1. a) Top-down design approach with adequate CAD tools to do the job
   b) Partitioning the system sensibly
   c) Aiming for simple interconnections
   d) High regularity within subsystem
   e) Generate and then verify each section of the design
2. Devote significant portion of total chip area to test and diagnostic facility
3. Select architectures that allow design objectives and high regularity in realization

Illustration of design processes:

1. Structured design begins with the concept of hierarchy

2. It is possible to divide any complex function into less complex sub functions that is up to leaf cells

3. Process is known as top-down design

4. As a systems complexity increases, its organization changes as different factors become relevant to its creation

5. Coupling can be used as a measure of how much sub models interact

6. It is crucial that components interacting with high frequency be physically proximate, since one may pay severe penalties for long, high-bandwidth interconnects

7. Concurrency should be exploited – it is desirable that all gates on the chip do useful work most of the time

8. Because technology changes so fast, the adaptation to a new process must occur in a short time.

Hence representing a design several approaches are possible. They are:

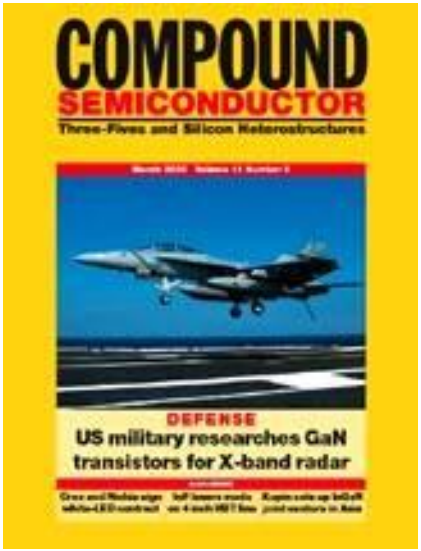
- Conventional circuit symbols
- Logic symbols
- Stick diagram
- Any mixture of logic symbols and stick diagram that is convenient at a stage
- Mask layouts
- Architectural block diagrams and floor plans

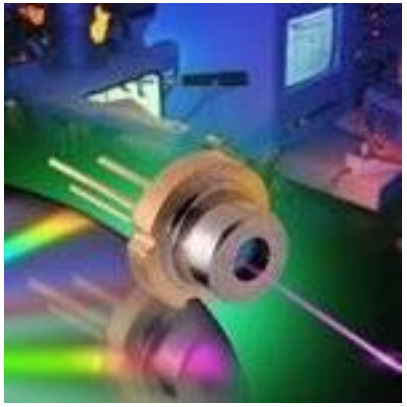
See the Pdf file

To summaries the design steps

- Set out the specifications
- Partition the architecture into subsystems
- Set a tentative floor plan
- Determine the interconnects
- Choose layers for the bus & control lines
- Conceive a regular architecture
- Develop stick diagram
- Produce mask layouts for standard cell
- Cascade & replicate standard cells as required to complete the design

Gallium Arsenide Semiconductors





What is Gallium Arsenide?

Gallium Arsenide (GaAs) is a compound semiconductor: a mixture of two elements, Gallium (Ga) and Arsenic (As). Gallium is a byproduct of the smelting of other metals, notably aluminum and zinc, and it is rarer than gold. Arsenic is not rare, but is poisonous.

The uses of GaAs are varied and include being used in some diodes, field-effect transistors (FETs), and integrated circuits (ICs). GaAs components are useful in at ultra-high radio frequencies and in fast electronic switching applications. The benefit of using GaAs in devices is that it generates less noise than most other types of semiconductor components and, as a result, is useful in weak-signal amplification applications.

Advantages and Disadvantages of GaAS

Advantages

- Very high electron mobility
- High thermal stability
- Low noise
- Wide temperature operating range

Disadvantages

- No natural oxide as in Silicon
- High production costs
- Small size (4”) ingots

Unlike silicon cells, Gallium Arsenide cells are relatively insensitive to heat. Alloys made from GaAs using P, SB have characteristics complementary to those of GaAs, allowing great flexibility.

GaAs is very resistant to radiation damage. This, along with its high efficiency, makes GaAs very desirable for space applications. However, GaAs does nave drawbacks; the greatest barrier is the high cost of a single-crystal GaAs substrate.

GaAs and Other Compound Semiconducors

Semiconductor (commonly used compounds)		Silicon	Gallium arsenide (AlGaAs/ InGaAs)	Indium phosphide (InAlAs/ InGaAs)[a]	Silicon carbide	Gallium nitride (AlGaN/ GaN)
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm2/Vs	1500	8500	5400	700	1000-2000
Saturated (peak) electron velocity	$X10^7$ cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0
Thermal conductivity	W/cm•K	1.5	0.5	0.7	4.5	>1.5
Relative dielectric constant	ε_r	11.8	12.8	12.5	10.0	9.0

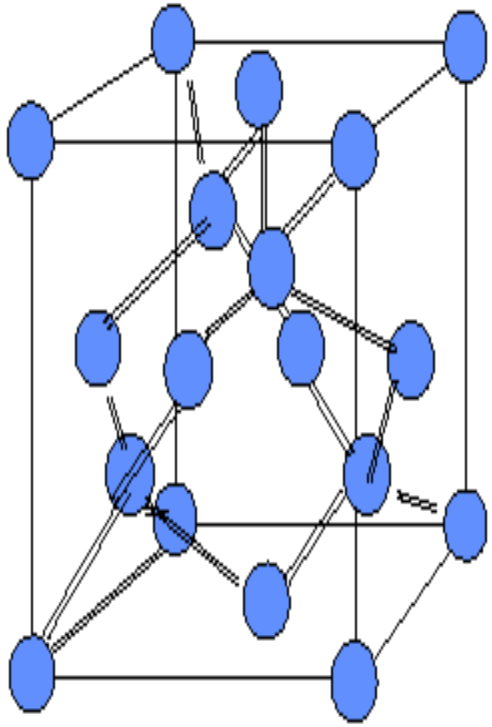
[a] The compounds are loosely known as indium-based.

The higher electron mobility for GaAs shows promise for high speed devices and circuits. The direct gap allows for emission of photons in LEDs and LASER devices.

	Silicon	GaAs
Minority Carrier Lifetime	0.003	1E-8
Electron Mobility	1500	8000
Hole Mobility (cm2/Vs)	600	400
Energy Gap (eV)	1.12 (indirect)	1.43 (direct)
Vapor Pressure	1E-8@930C	1@1050C

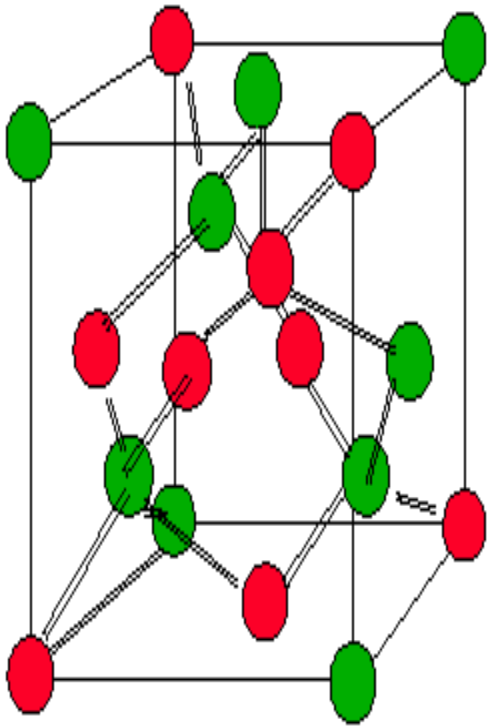
Crystal Structure

Diamond Lattice (Silicon)



Si

Zincblende Lattice (GaAs)



As

Ga

GaAs Devices

The **first generation** of GaAs devices included:

- depletion mode MESFET (Metal Semiconductor FET)
- enhancement mode MESFET
- enhancement mode JFET
- complementary enhancement mode FET (CE-JFET)

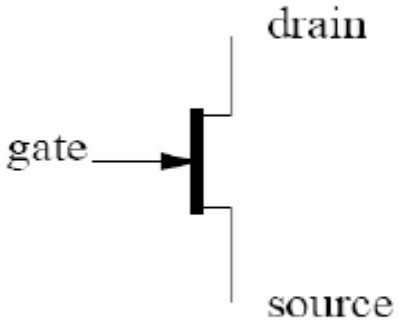
These devices have switching delays as low as 50ps for between 1 and 2.5mW power dissipation. MESFETs have been the mainstay of digital GaAs circuits.

The **second generation** devices include

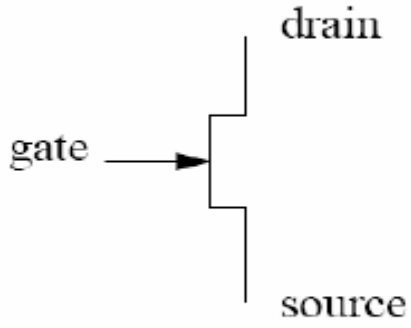
- high electron mobility transistor (HEMT)
- heterojunction bipolar transistor (HJBT)

Electron moblity in the second generation is up to 5 times higher than the first generation and are mostly used for analog circuits such as low noise RF amplifiers.

A recent innovation in device design has led to the introduction of complementary HEMT devices, i.e. p-devices with much better mobility than previous device generations which allows CMOS-like structures to be made.



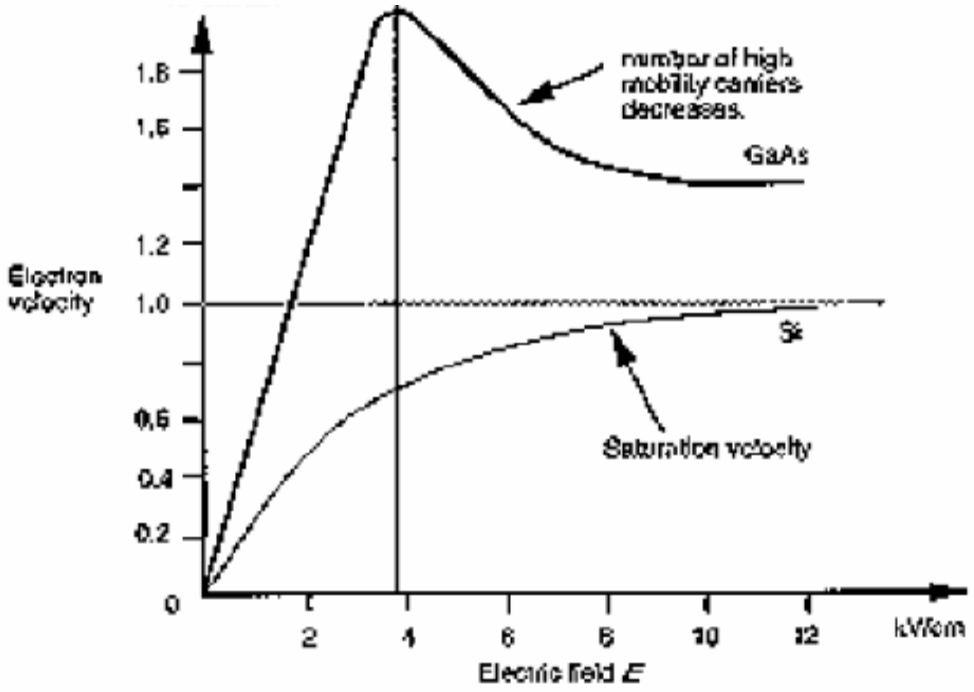
D-MESFET



E-MESFET

Characteristics - compared to Si.

- The saturated electron drift velocity of GaAs is ~2 times Silicon at lower electric field strengths due to a small valence band gap.

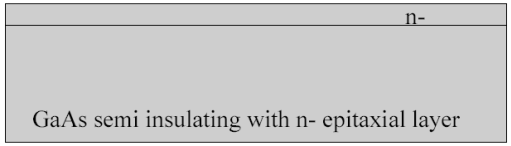


- This means GaAs devices require less voltage to enter saturation.
- The mobility of electrons in GaAs is 6-7 times that of Silicon resulting in very fast electron transit times.

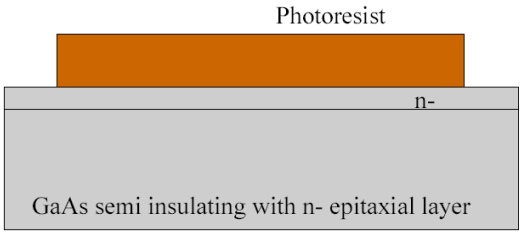
- Intrinsic bulk resistivities are higher (GaAs=10^8,Si=$2.2x10^5\Omega$.cm) which minimises parasitic capacitances and allows easy isolation of multiple devices in a single substrate.
- Higher radiation resistance because there is no gate oxide to trap charges.
- Wider operating temperature due to wider bandgap (-/+200C)
- Better photo-response than Si.
- Substrate is more brittle than Si and therefore thicker.
- mobility is dependent on direction in crystal planes, so layout devices with gates all in one direction to maximise mobility.
- mobility of holes in GaAs is slightly worse than that of Silicon, so p-type devices in GaAs are large and slow. Therefore complementary GaAs structures have been unpopular.

GaAs Processing

Semi insulating starting wafer
5 Levels Photo
2 Levels Ion Implant
2 Levels LPCVD SiO2

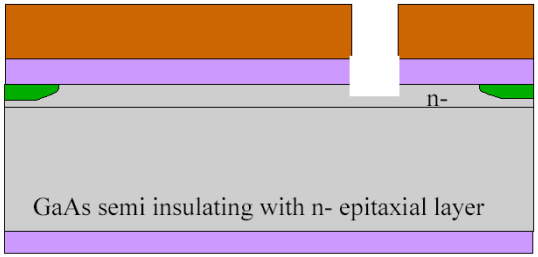


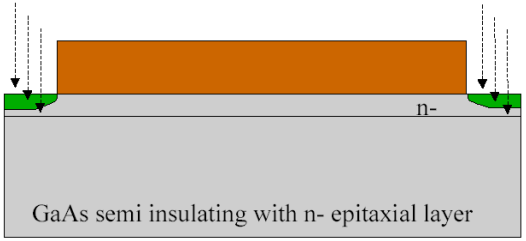
Starting wafer



First Photoresist for Channel Stop

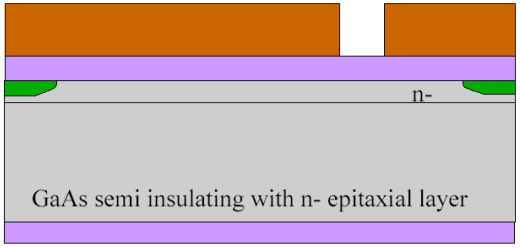
2nd Photo Channel Etch

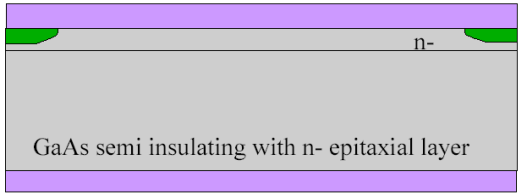




Alignment & Channel Stop Implant

2nd Photo Channel Etch

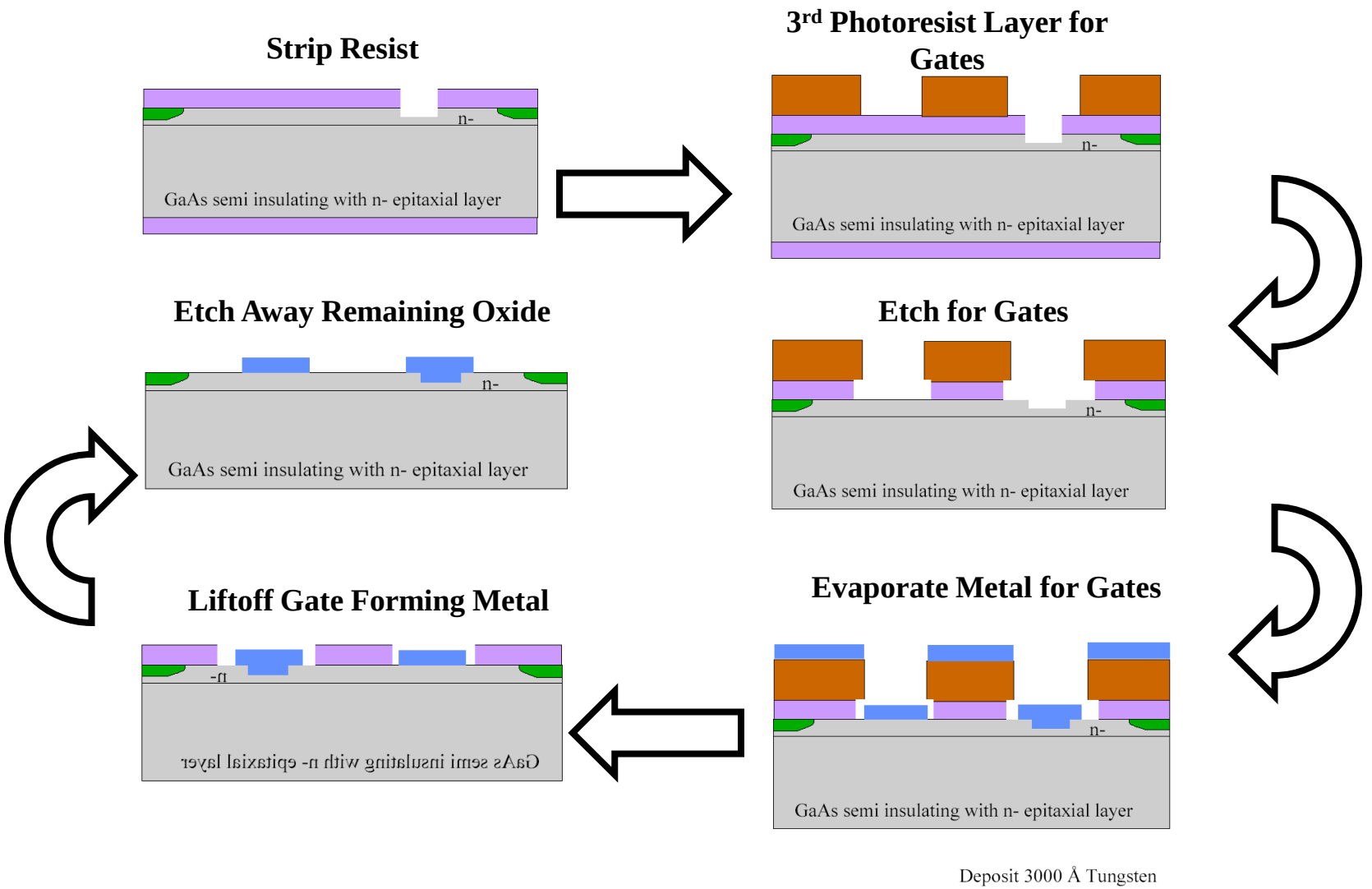




First Encapsulation

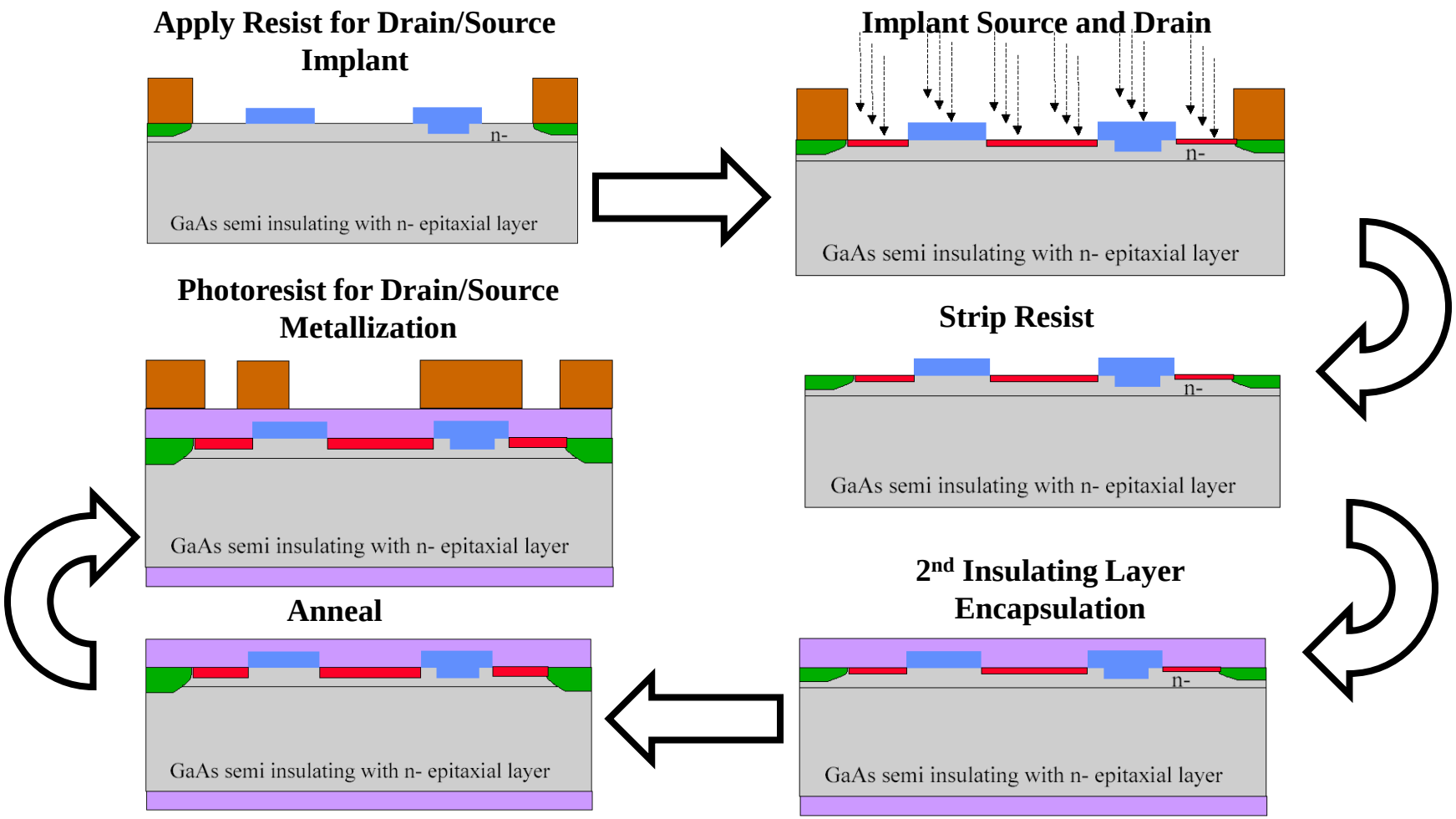
LTO SiO2 5000 Å

GaAs Processing

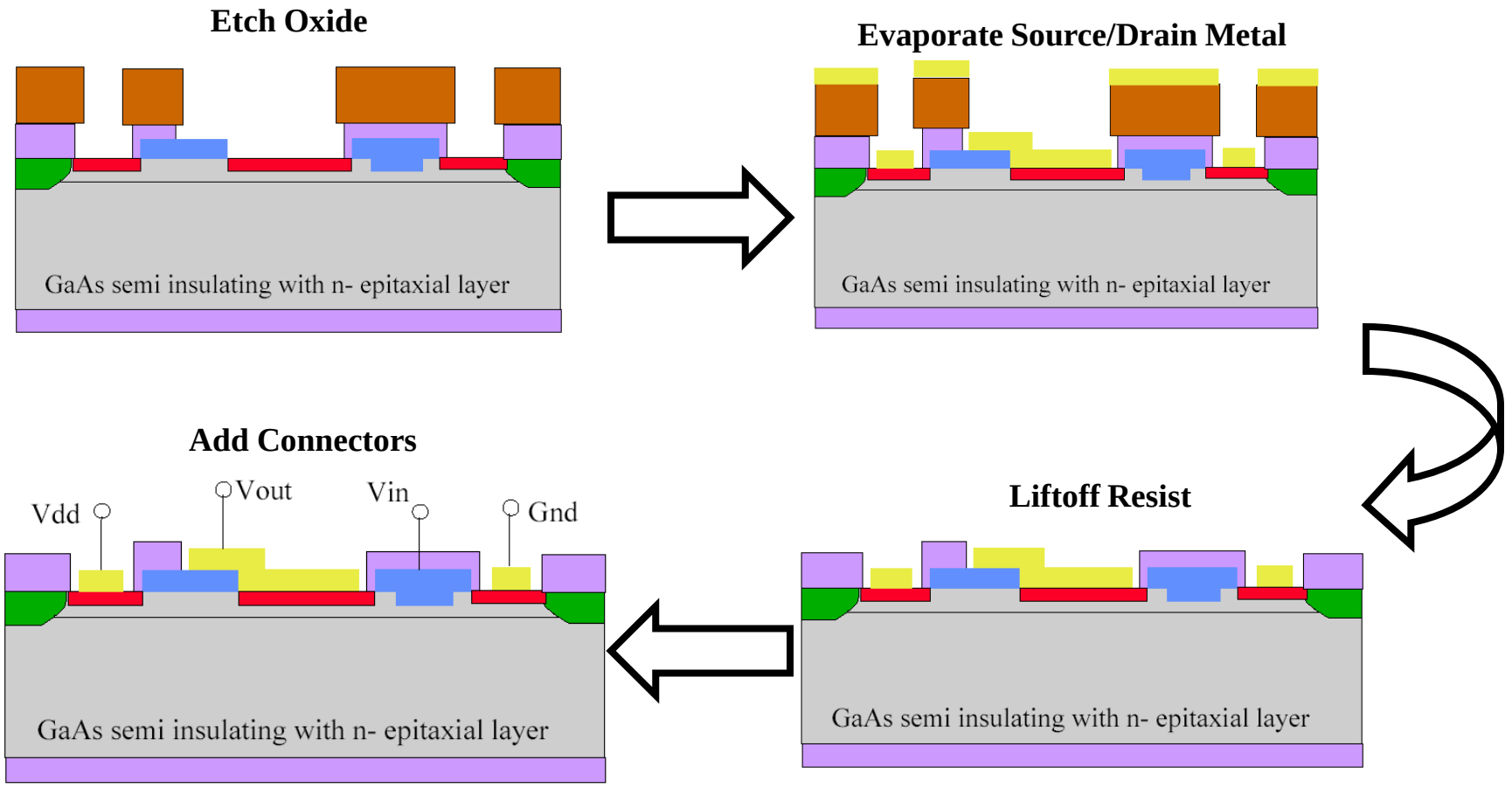


Deposit 3000 Å Tungsten

GaAs Processing



GaAs Processing



Gallium arsenide is **used** in the manufacture of devices such as microwave frequency integrated circuits, monolithic microwave integrated circuits, infrared light-emitting diodes, laser diodes, solar cells and optical windows.

Having a higher electron mobility, this allows flow of electricity in transistors to flow much faster and can lead to many **future applications** such as:

- faster computers
- better wireless communication devices