Course Title: Digital Logic and System Design

Course Code: CSE 210

Final project on ALU

Experiment Name: Design a 4-bit ALU with 4-bit parallel adder (using logics gate)

ALU - Arithmetic and Logical Unit :

$Xi = Ai + S2.S1'.S0'.Bi + S2.S1.S0'.Bi'$

$Yi = S0.Bi + S1.Bi'$

$Zi = S2'.Ci$

Arithmetic -

Input - A , B

S2	S1	S0	Cin	Xi	Yi	Fi = (Xi xor Yi xor cin)	
0	0	0	0	Ai	0	A + 0 = A	Transfer
			1	Ai	0	A + 0 +1 = A + 1	Increment
0	0	1	0	Ai	Bi	A+B (Add)	addition
			1	Ai	Bi	A+B+1 (Add)	Add with carry
0	1	0	0	Ai	Bi'	A+ B' =A-B -1	Add A with B`
			1	Ai	Bi'	A +B'+1 = A - B	Subtraction
0	1	1	0	Ai	1	A + 2^n -1	Decrement

			1	Ai	1	A + (2^n -1) + 1 = A + 2^n	Transfer

Logical:

S2	S1	S0	Xi	Yi	F = (Xi xor Yi)	
1	0	0	Ai + Bi	0	A + B (or)	
1	0	1	Ai	Bi	A xor B	
1	1	0	Ai + Bi’	Bi’	A . B	
1	1	1	Ai	1	A’	

Report:

1) Problem Statement

2) Instruments (used in this experiment)

3) Truth table

4) Logic expression

5) Logic Diagram

6) Discussion