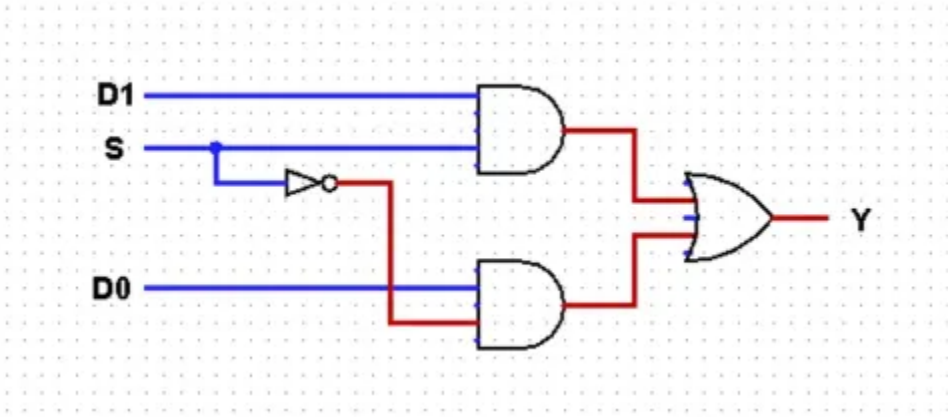
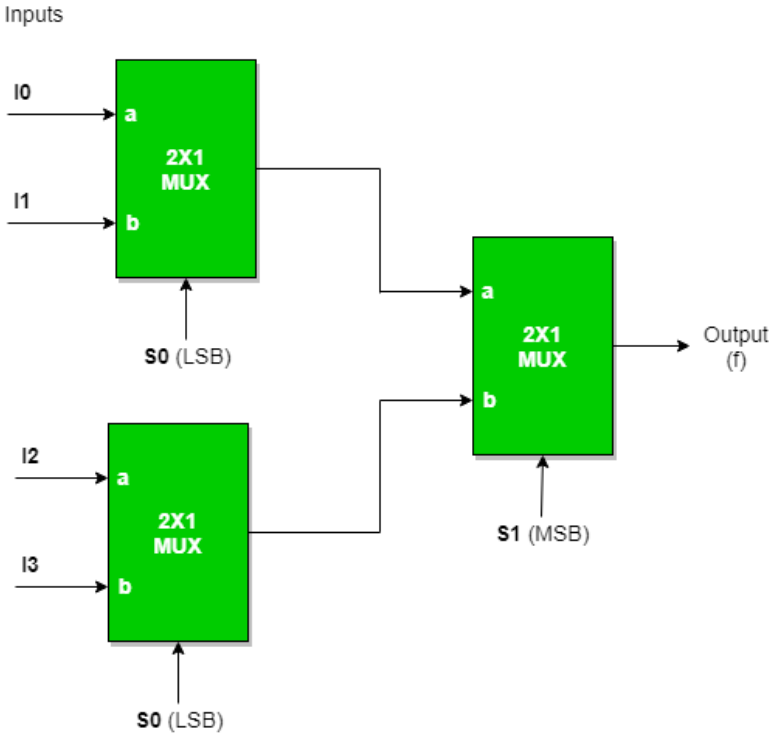
a) Design a 2x1 MUX.
b) Using 2 2x1 MUX, design a 4x1 MUX.
c) Design and implementation of 1 bit Logic unit.



2x1 MUX



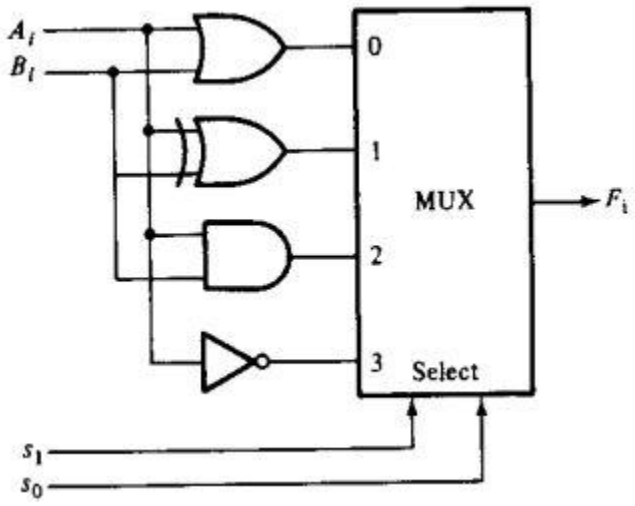
2 2x1 to form 4x1

Truth Table

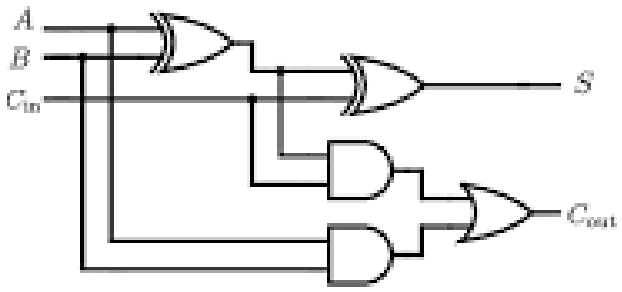
S0	S1	f
0	0	I0
0	1	I1
1	0	I2
1	1	I3

LU

s_1	s_0	Output	Operation
0	0	$F_i = A_i + B_i$	OR
0	1	$F_i = A_i \oplus B_i$	XOR
1	0	$F_i = A_i B_i$	AND
1	1	$F_i = A_i'$	NOT

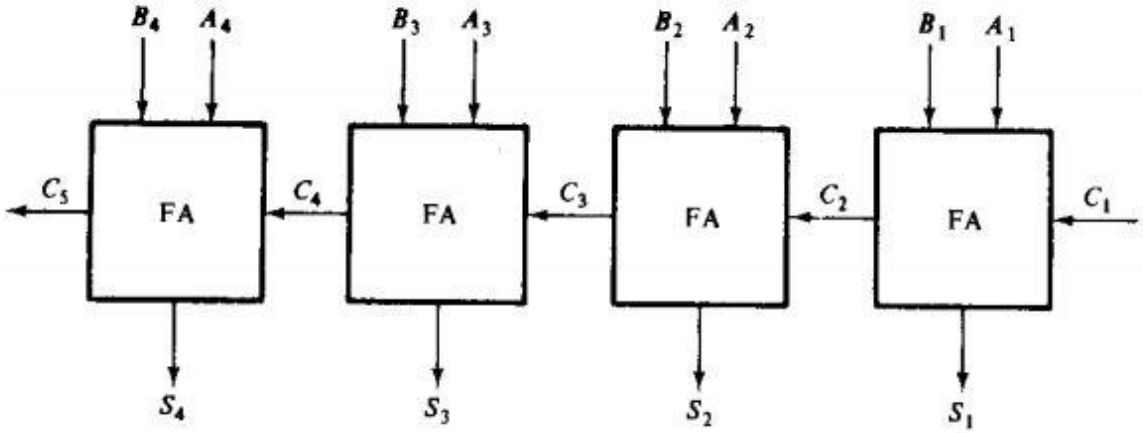


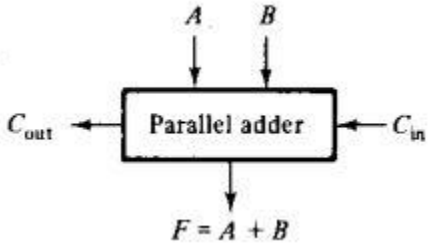
AU

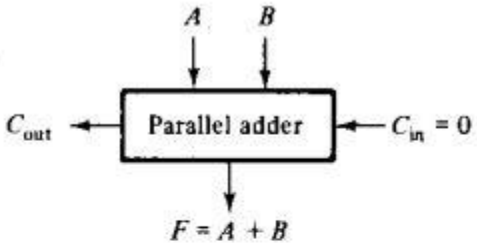


Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

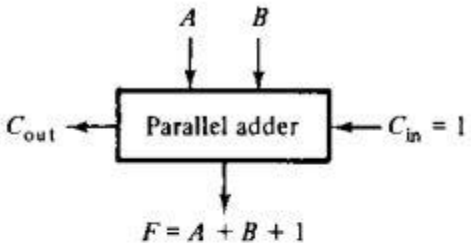
FA



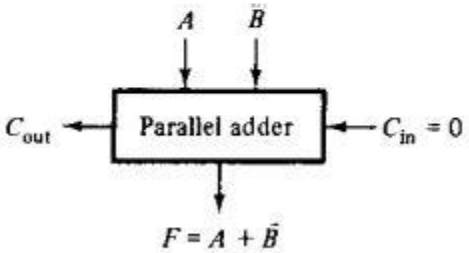




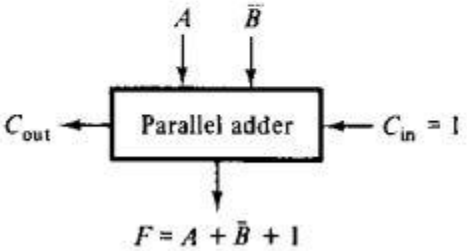
(a) Addition



(b) Addition with carry



(c) A plus 1's complement of B



(d) Subtraction

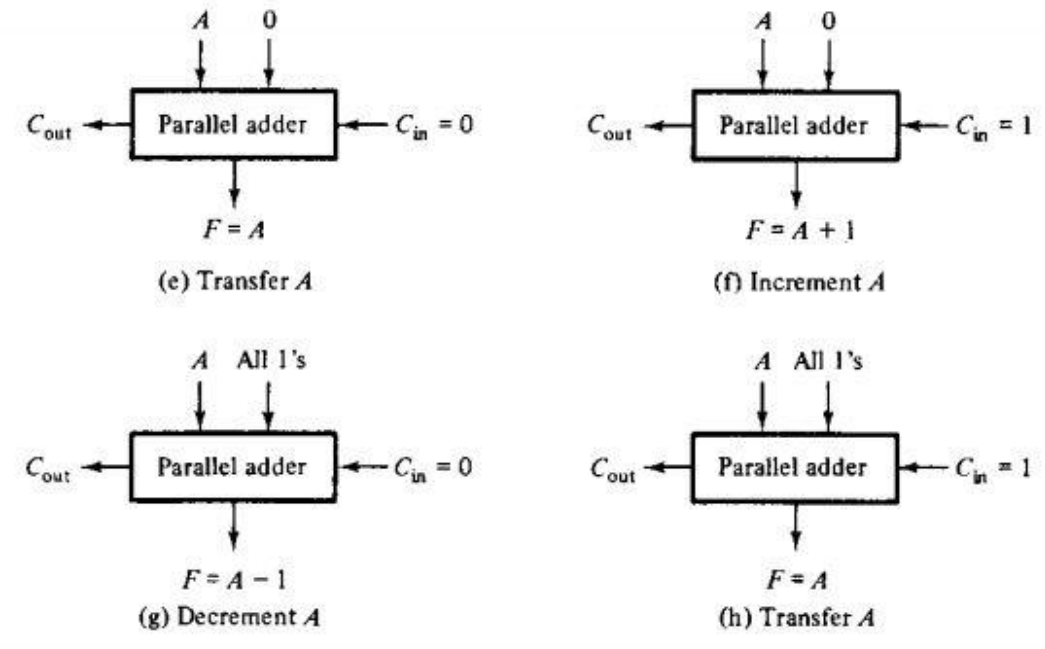
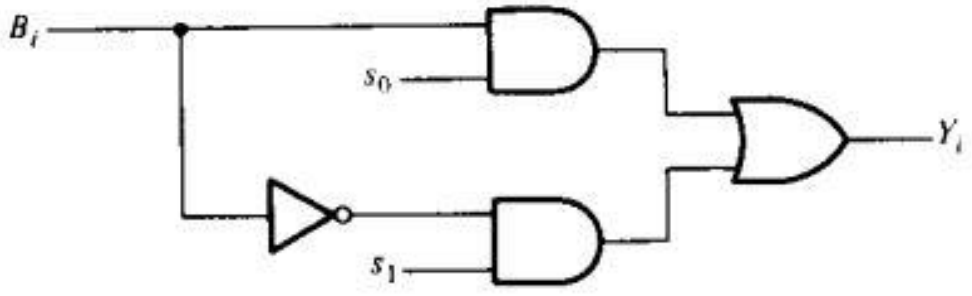


Figure 9-6 Operations obtained by controlling one set of inputs to a parallel adder

S_1	S_0	Y_i
0	0	0
0	1	B_i
1	0	B_i'
1	1	1



Function select			Y equals	Output equals	Function
s_1	s_0	C_{in}			
0	0	0	0	$F = A$	Transfer A
0	0	1	0	$F = A + 1$	Increment A
0	1	0	B	$F = A + B$	Add B to A
0	1	1	B	$F = A + B + 1$	Add B to A plus 1
1	0	0	$\overline{B}$	$F = A + \overline{B}$	Add 1's complement of B to A
1	0	1	$\overline{B}$	$F = A + \overline{B} + 1$	Add 2's complement of B to A
1	1	0	All 1's	$F = A - 1$	Decrement A
1	1	1	All 1's	$F = A$	Transfer A

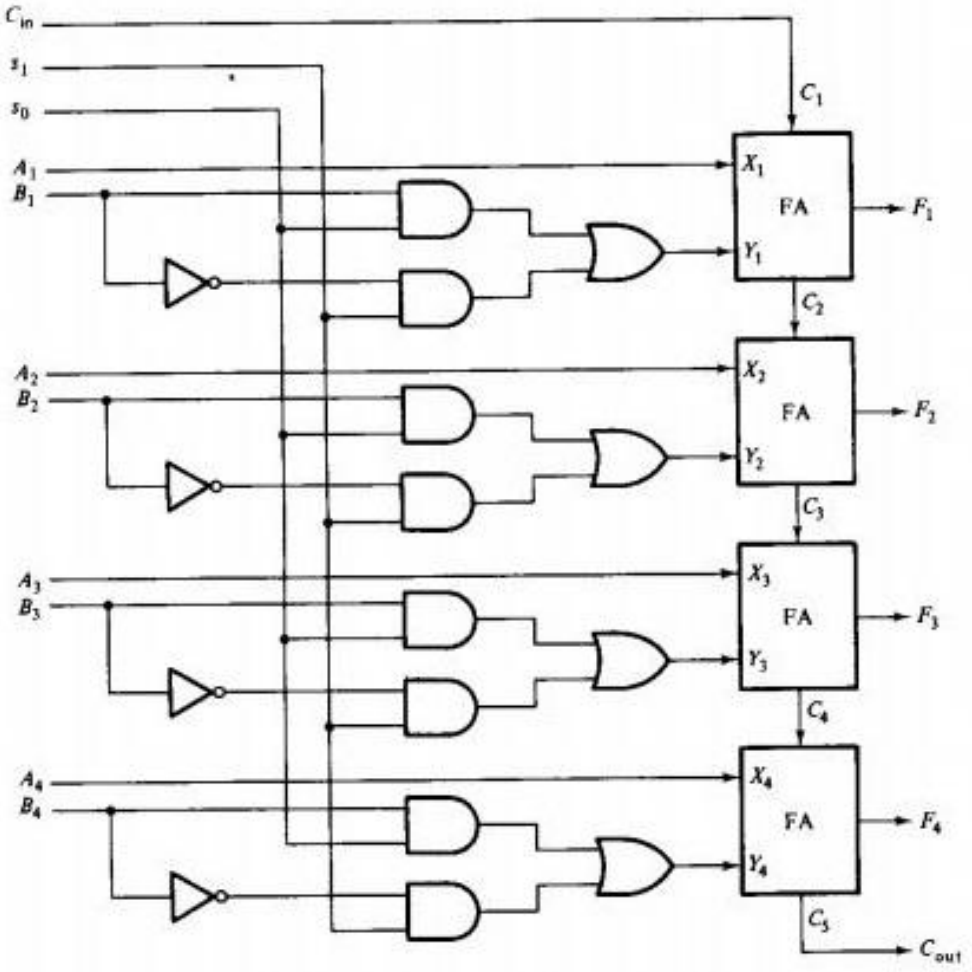


Figure 9-8 Logic diagram of arithmetic circuit