HW3 + Simulations

FPGA & ASIC

Ali Naghiloo 40010093

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Dr. Hosseini-Nejad

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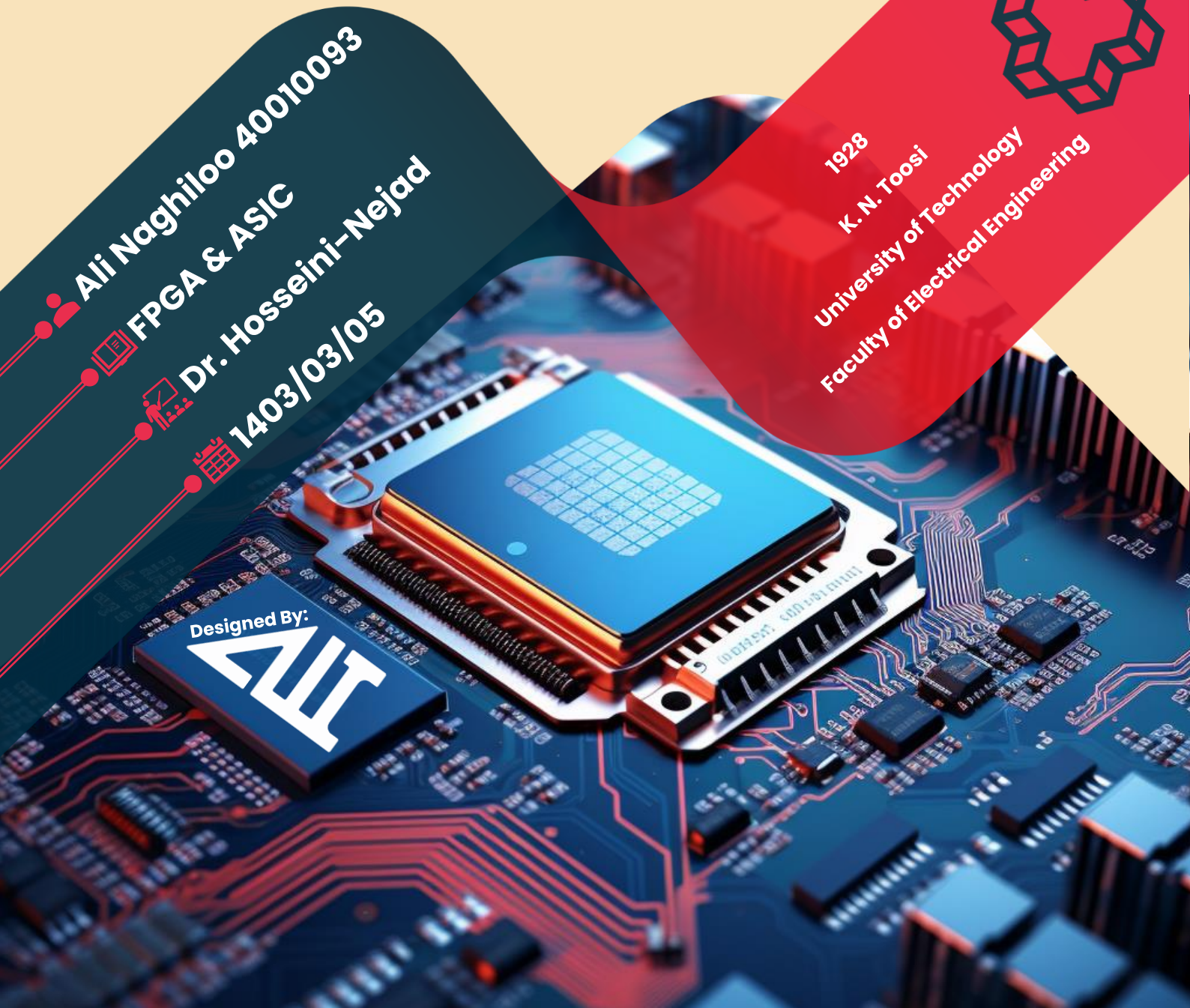
K. N. Toosi
University of Technology
Faculty of Electrical Engineering



DPRAM Code:

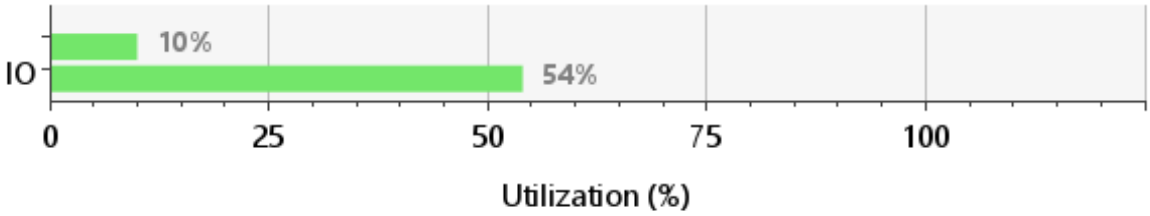
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity DPRAM is
    GENERIC(WIDTH : INTEGER := 8;
            LENGTH : INTEGER := 256;
            Read : std_logic := '0');

    Port ( DiA,DiB : in STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0);
           AddrA,AddrB : in integer range 0 TO LENGTH-1;
           DoA,DoB : out STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0);
           CLKA,CLKB : in STD_LOGIC;
           R_WA,R_WB: in STD_LOGIC;
           EnA,EnB : in STD_LOGIC);
end DPRAM;

architecture Behavioral of DPRAM is

subtype Byte is STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0);
type RAM_type is array (0 to Length-1) of Byte;
shared variable RAM : RAM_type;

begin

A: process(CLKA)
begin
if (CLKA'event and CLKA='1') then
    if (ENA='1') then
        if (R_WA = Read) then DoA <= RAM(AddrA); --Reading
        else RAM(AddrA) := DiA; --Writing
        end if;
    end if;
end if;
end process;

B: process(CLKB)
begin
if (CLKB'event and CLKB='1') then
    if (ENB='1') then
        if (R_WB = Read) then DoB <= RAM(AddrB); --Reading
        else RAM(AddrB) := DiB; --Writing
        end if;
    end if;
end if;
end process;
end Behavioral;
```

```
------------------------------ TB -------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity DPRAM_tb is
end DPRAM_tb;

architecture Behavioral of DPRAM_tb is
    constant WIDTH : integer := 8;
    constant LENGTH : integer := 256;
    signal DiA,DiB : STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0):=(others=>'0');
    signal AddrA : integer range 0 TO LENGTH-1 :=0;
    signal AddrB : integer range 0 TO LENGTH-1 :=1;
    signal DoA,DoB : STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0):=(others=>'0');
    signal CLKA,CLKB : STD_LOGIC :='0';
    signal R_WA,R_WB : STD_LOGIC :='1';
    signal EnA,EnB : STD_LOGIC:='1';

    constant periodA : time := 9.33 ns;
    constant periodB : time := 9.33 ns;
begin
    UUT: entity work.DPRAM generic map(WIDTH, LENGTH, '0')
         port map(DiA, DiB, AddrA, AddrB, DoA, DoB, CLKA, CLKB, R_WA, R_WB, EnA, EnB);

        CLKA <= not CLKA after PeriodA/2;
        CLKB <= not CLKB after PeriodB/2;

     addra <= 1 after 10 ns, 3 after 20 ns, 5 after 30 ns, 7 after 40 ns, 9 after 50 ns,
              4 after 60 ns, 9 after 70 ns, 10 after 80 ns, 3 after 90 ns, 6 after 100 ns ;

     addrb <= 2 after 10 ns, 4 after 20 ns, 6 after 30 ns, 8 after 40 ns, 10 after 50 ns,
              2 after 60 ns, 8 after 70 ns, 1 after 80 ns, 5 after 90 ns, 7 after 100 ns ;

     dia <= X"0F" after 10 ns, X"09" after 20 ns, X"A6" after 30 ns, X"F7" after 40 ns,
X"E9" after 50 ns;
     dib <= X"0D" after 10 ns, X"04" after 20 ns, X"A6" after 30 ns, X"D7" after 40 ns,
X"FD" after 50 ns ;

     r_wa <= '1' after 4 ns , '0' after 55 ns;
     r_wb <= '1' after 4 ns , '0' after 55 ns;

end Behavioral;
```

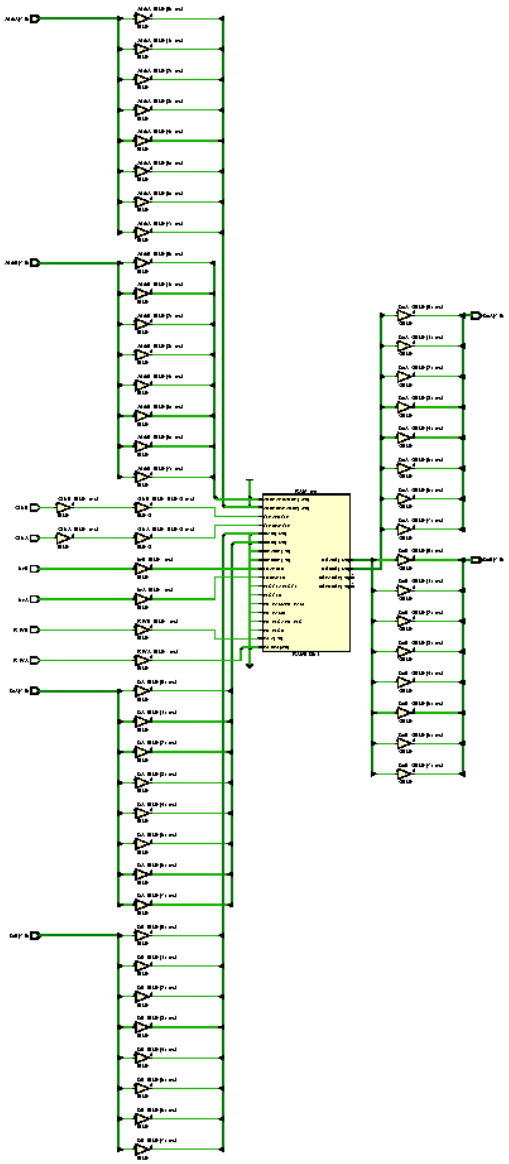
Utilization-synth & synthesis report is as follows:

Summary

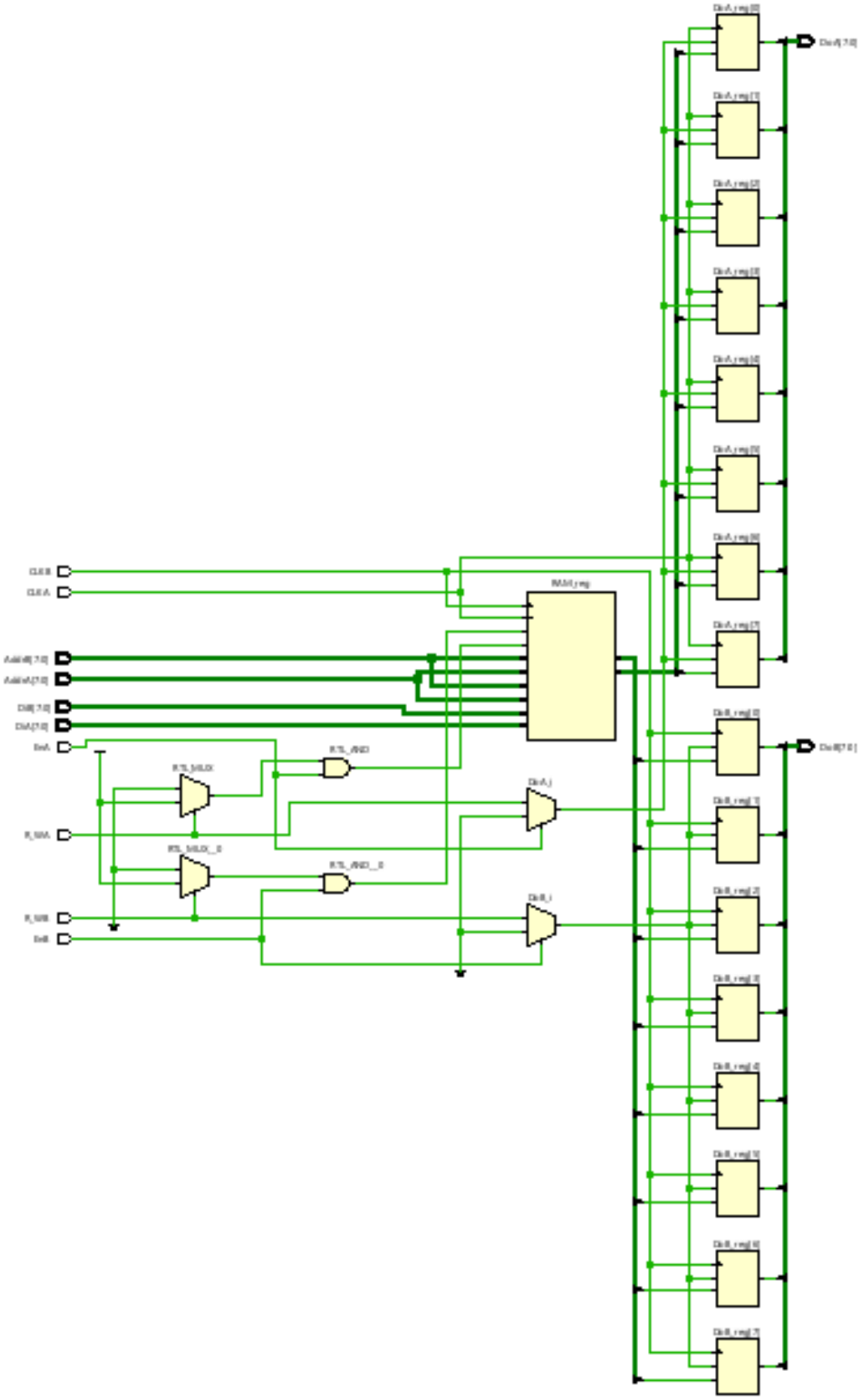
Resource	Utilization	Available	Utilization %
BRAM	0.50	5	10.00
IO	54	100	54.00



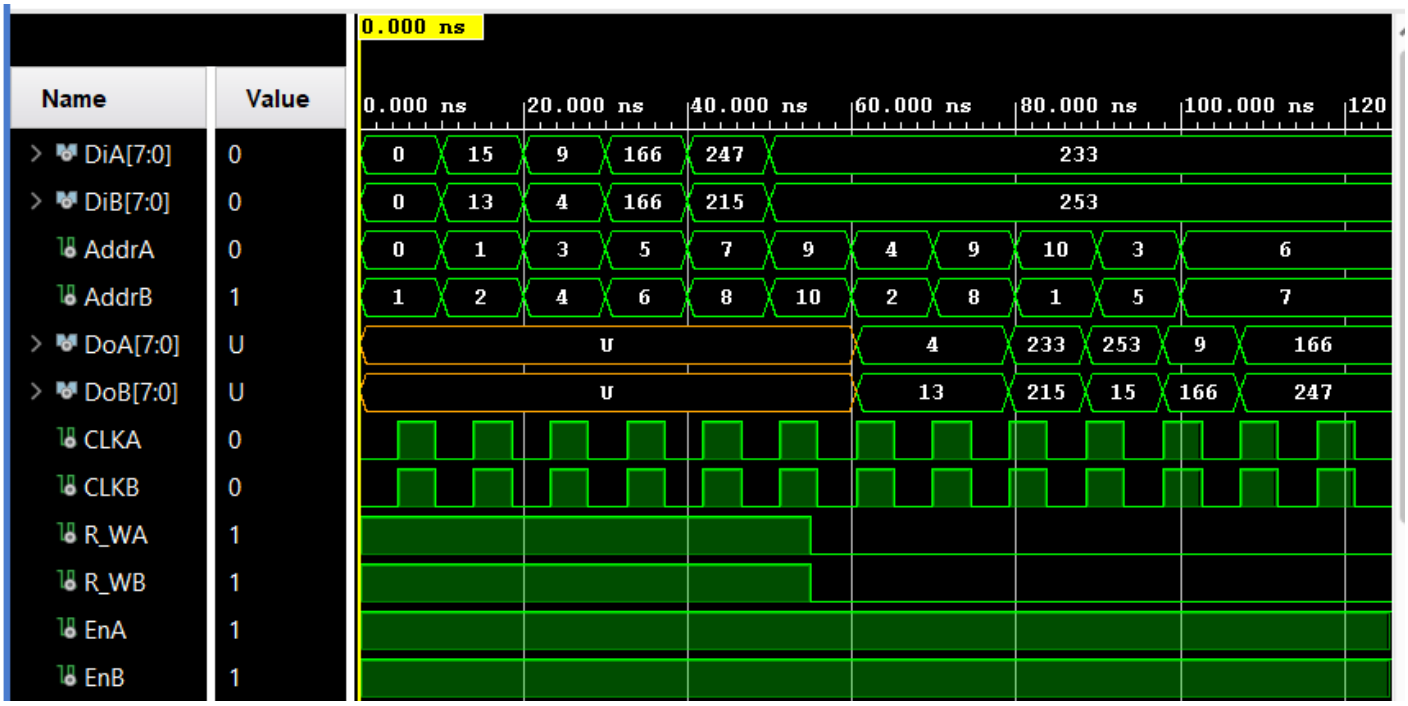
LUT Schematic:



RTL Schematic:



Waveform


0.000 ns
Name
Value
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120
DiA[7:0] 0
DiB[7:0] 0
AddrA 0
AddrB 1
DoA[7:0] U
DoB[7:0] U
CLKA 0
CLKB 0
R_WA 1
R_WB 1
EnA 1
EnB 1
0 15 9 166 247 233
0 13 4 166 215 253
0 1 3 5 7 9 4 9 10 3 6
1 2 4 6 8 10 2 8 1 5 7
U 4 233 253 9 166
U 13 215 15 166 247

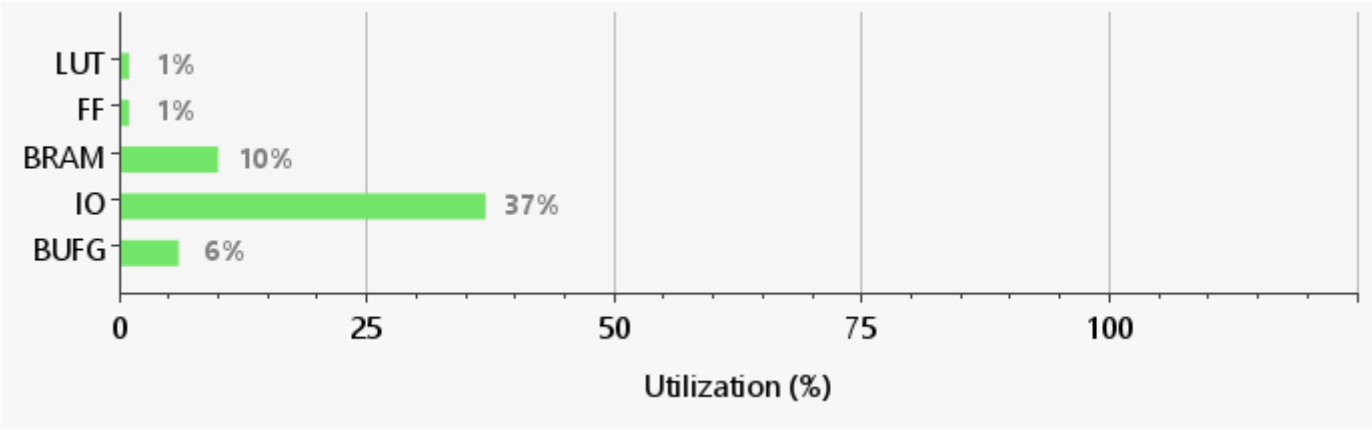
LIFO CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity LIFO is
    generic (width : integer :=8;
             length : integer :=256;
             Write : std_logic :='1');

    port (  Di : in std_logic_vector(width-1 downto 0);
            Addr : in integer range 0 to length-1 ;
            Reset : in std_logic;
            Do : out std_logic_vector(width-1 downto 0);
            Rd_Wr : in std_logic;
            CLK : in std_logic;
            SP : buffer integer range 0 to Length-1;
            Full : buffer  std_logic:='0';
            Empty : buffer std_logic:='1');
end entity LIFO;

architecture behavorial of LIFO is
--signal SP : integer range 0 to Length-1 :=0;

subtype Byte is std_logic_vector(width-1 downto 0);
type LIFO_type is array (0 to length-1) of Byte;
signal memory : LIFO_type;

begin
    process(CLK,reset)
    begin
    if (Reset='1') then SP <= Addr;
    elsif (CLK'event and CLK='1') then
        if (Rd_Wr=Write and Full/='1') then memory(SP)<=Di; SP<=SP+1;
        elsif (Rd_Wr/=Write and Empty/='1') then Do<=memory(SP-1); SP<=SP-1;
        end if;
    end if;
    end process;
Full <= '1' when SP=Length else '0';
Empty <= '1' when SP=Addr else '0';
end architecture behavorial;
```

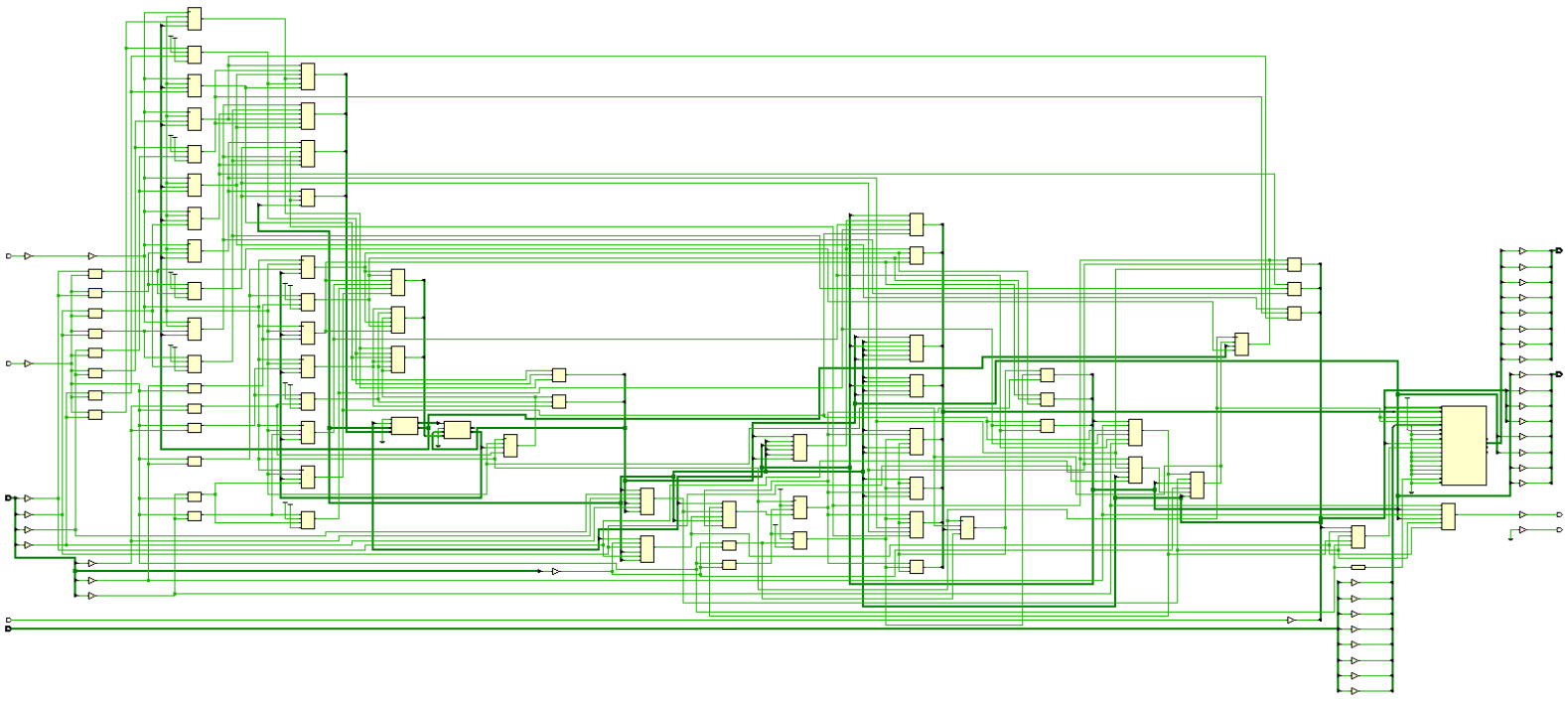
```
------------------------------ TB ------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity LIFO_tb is
end LIFO_tb;

architecture Behavioral of LIFO_tb is
    constant WIDTH : integer := 8;
    constant LENGTH : integer := 256;
    signal Di : STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0):=(others=>'0');
    signal Addr : integer range 0 to LENGTH-1 := 0;
    signal Reset : std_logic :='0';
    signal Do : STD_LOGIC_VECTOR(WIDTH-1 DOWNTO 0);
    signal Rd_Wr : std_logic:='1';
    signal CLK : std_logic:='0';
    signal SP : integer range 0 to Length-1 :=0;
    signal Full : std_logic :='0';
    signal Empty : std_logic :='1';

    constant period : time := 5 ns;
begin
    UUT: Entity work.LIFO generic map(WIDTH, LENGTH, '1')
         port map(Di, Addr, Reset, Do, Rd_Wr, CLK, SP, Full, Empty);

CLK <= not CLK after Period/2;
Reset <= '1' after 1 ns,'0' after 10 ns ;

stimulus1: Process
begin
Addr <= 245;
Rd_Wr <= '1';
Wait for 49 ns;

Addr <= 7;
Rd_Wr <= '0';
wait;
end process;
stimulus2: Process
begin
for i in 0 to 10 loop
Di <= Di + 19;
wait for 4.33 ns;
end loop;
wait;
end process;
end Behavioral;
```

Utilization-synth & synthesis report is as follows:

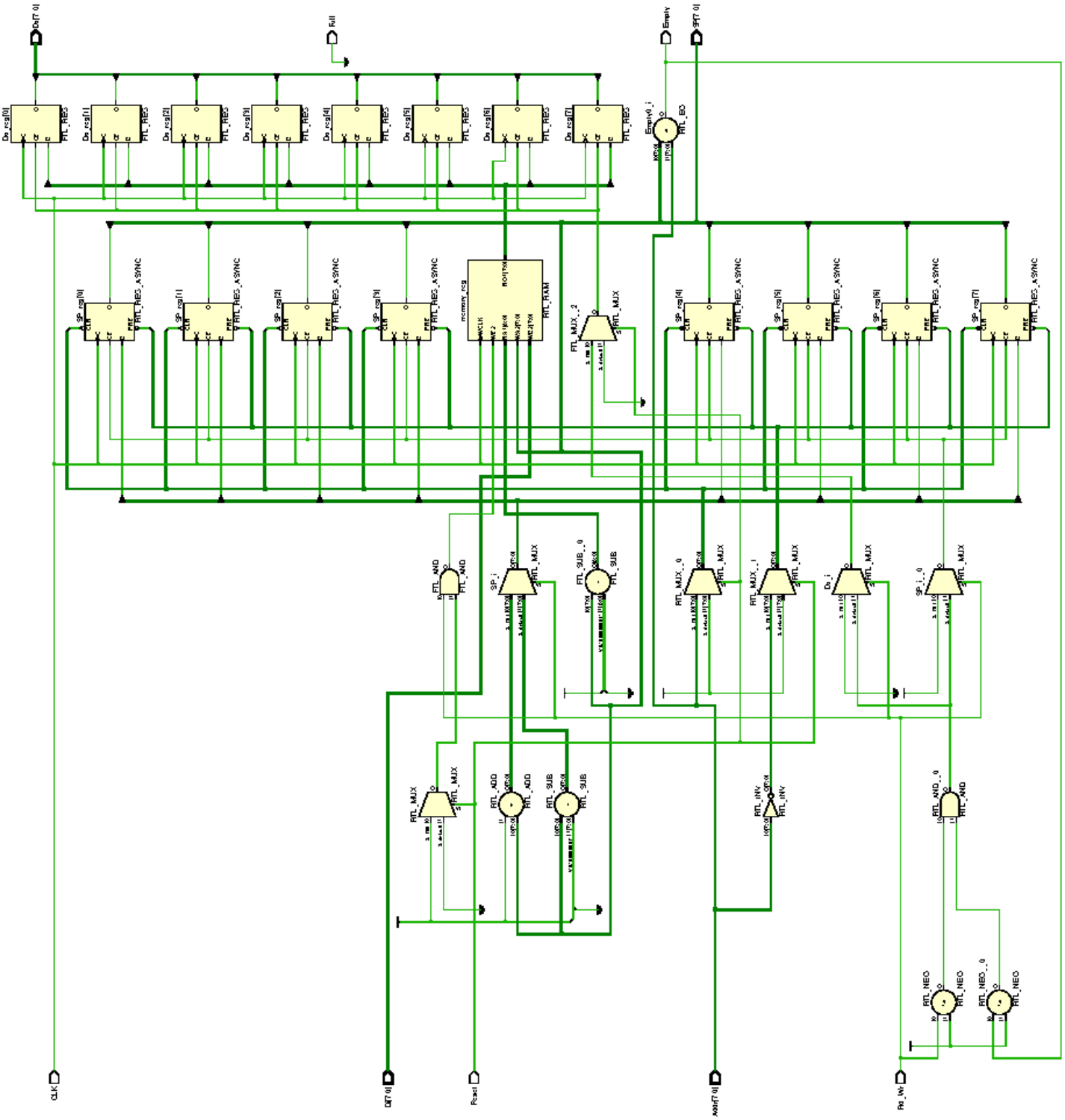
Resource	Utilization	Available	Utilization %
LUT	46	3750	1.23
FF	16	7500	0.21
BRAM	0.50	5	10.00
IO	37	100	37.00
BUFG	1	16	6.25



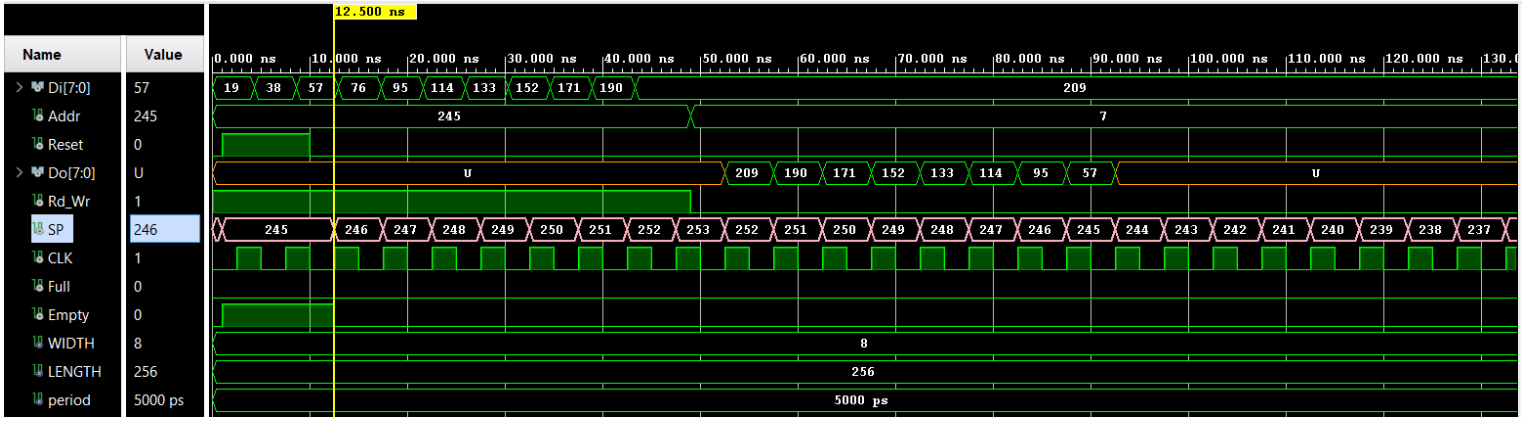
LUT Schematic:



RTL Schematic:



Waveform


Name
Value
Di[7:0]
57
Addr
245
Reset
0
Do[7:0]
U
Rd_Wr
1
SP
246
CLK
1
Full
0
Empty
0
WIDTH
8
LENGTH
256
period
5000 ps
12.500 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000 ns
110.000 ns
120.000 ns
19 38 57 76 95 114 133 152 171 190 209
245 7
U 209 190 171 152 133 114 95 57 U
245 246 247 248 249 250 251 252 253 252 251 250 249 248 247 246 245 244 243 242 241 240 239 238 237
8
256
5000 ps