COMSATS University Islamabad, Lahore Campus
Department of Electrical and Computer Engineering
M. A. Jinnah Campus, Lahore.

EEE241 – Digital Logic Design

SP23-BCS-A Fall 2023

Total Marks 20 **Wednesday 22 November 2023**

Assignment 2

Resource Person: Dr. Muhammad Farooq-i-Azam

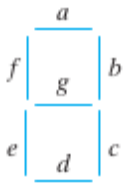
Submission Deadline: **Wednesday 29 November 2023**

Problem 1 **(10)**

Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

Problem 2 **(10)**

A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig. P4.9(a). The numeric display chosen to represent the decimal digit is shown in Fig. P4.9(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.



(a) Segment designation

(b) Numerical designation for display

FIGURE P4.9

Notice

Work submitted should be your own. A strict disciplinary action will be taken against any students who submit plagiarized homework or assignment. This includes ZERO marks in the submitted work, fine, failure in the course and expulsion from the degree program.