

Digital Fundamentals

CHAPTER 6 Functions of Combinational Logic

Basic Adders

Half-Adder

Simple Binary Addition

0 + 0 = 0 Zero plus zero equals zero

0 + 1 = 1 Zero plus one equals one

1 + 0 = 1 One plus zero equals one

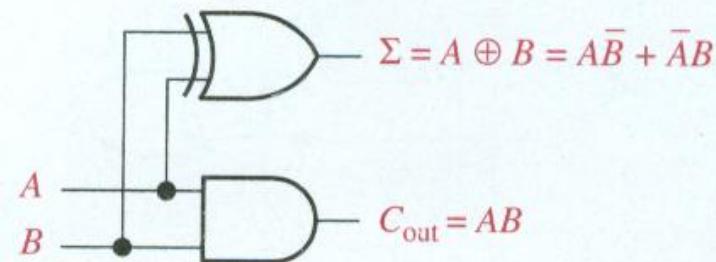
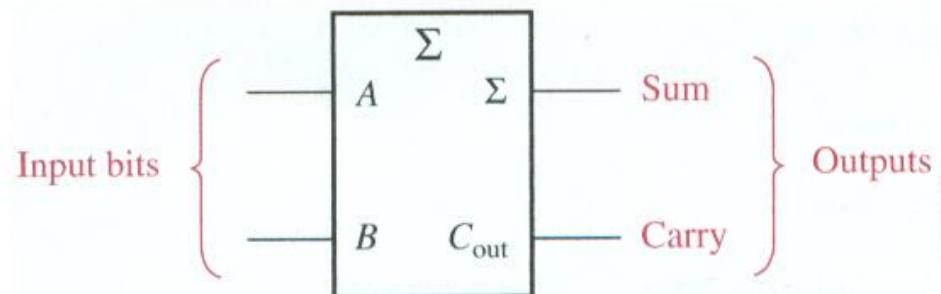
1 + 1 = 10 One plus one equals zero with a carry of one

Half-Adder

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum
 C_{out} = output carry
A and B = input variables (operands)

Half-Adder Truth Table



Full-Adder

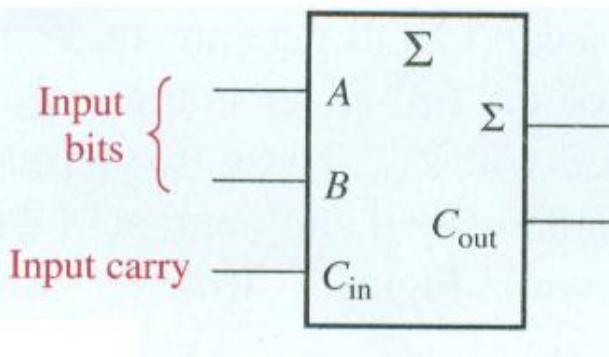
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as CI

C_{out} = output carry, sometimes designated as CO

Σ = sum

A and B = input variables (operands)

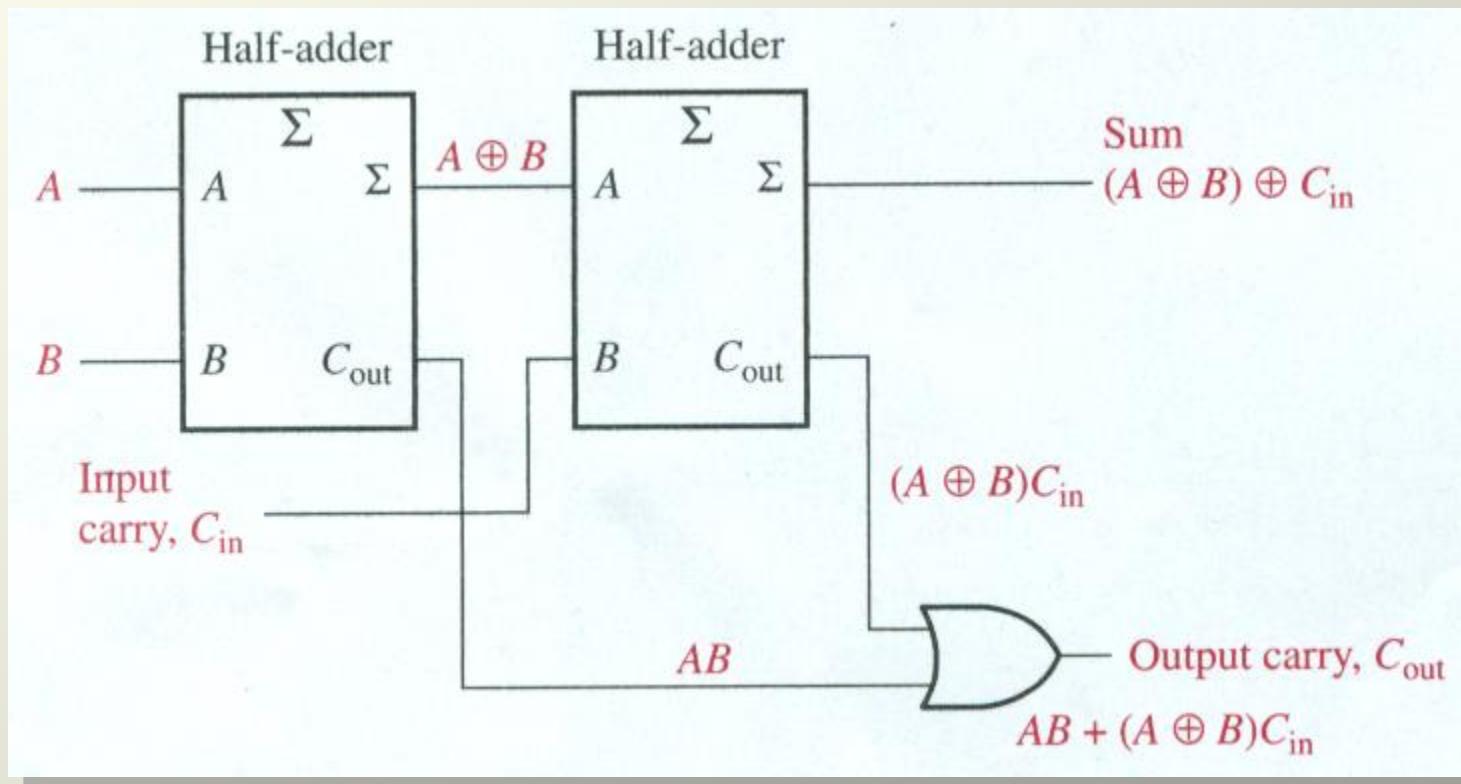


$$\Sigma = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B)C_{in}$$

Full-Adder

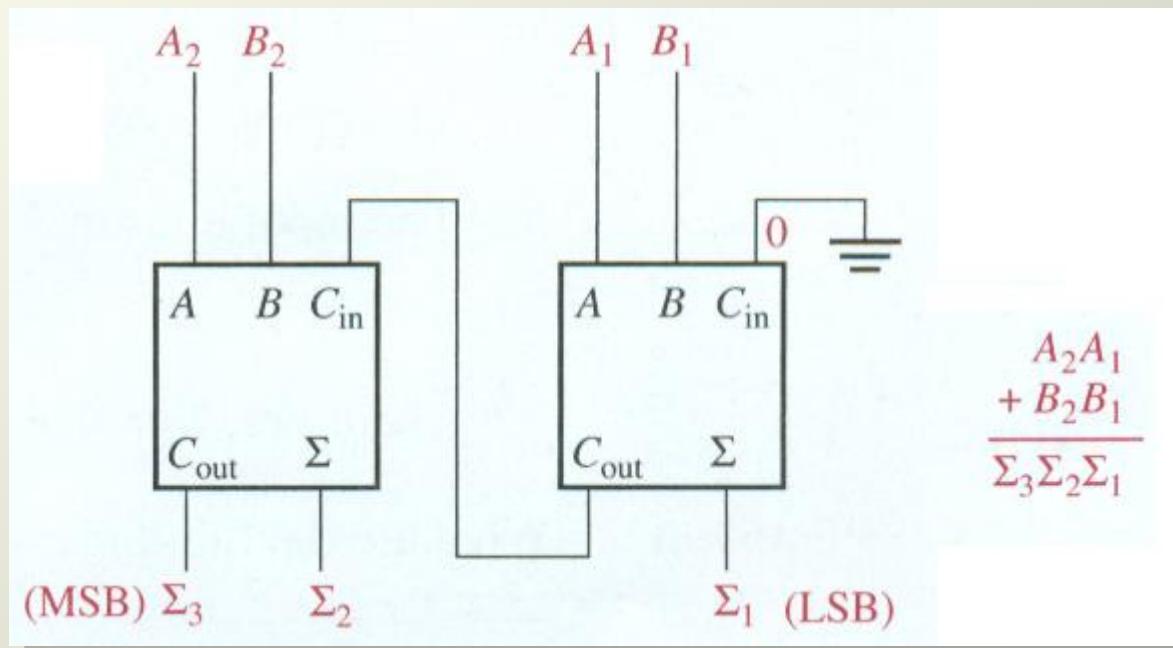
- Full adder from two half-adder circuits



Parallel Binary Adders

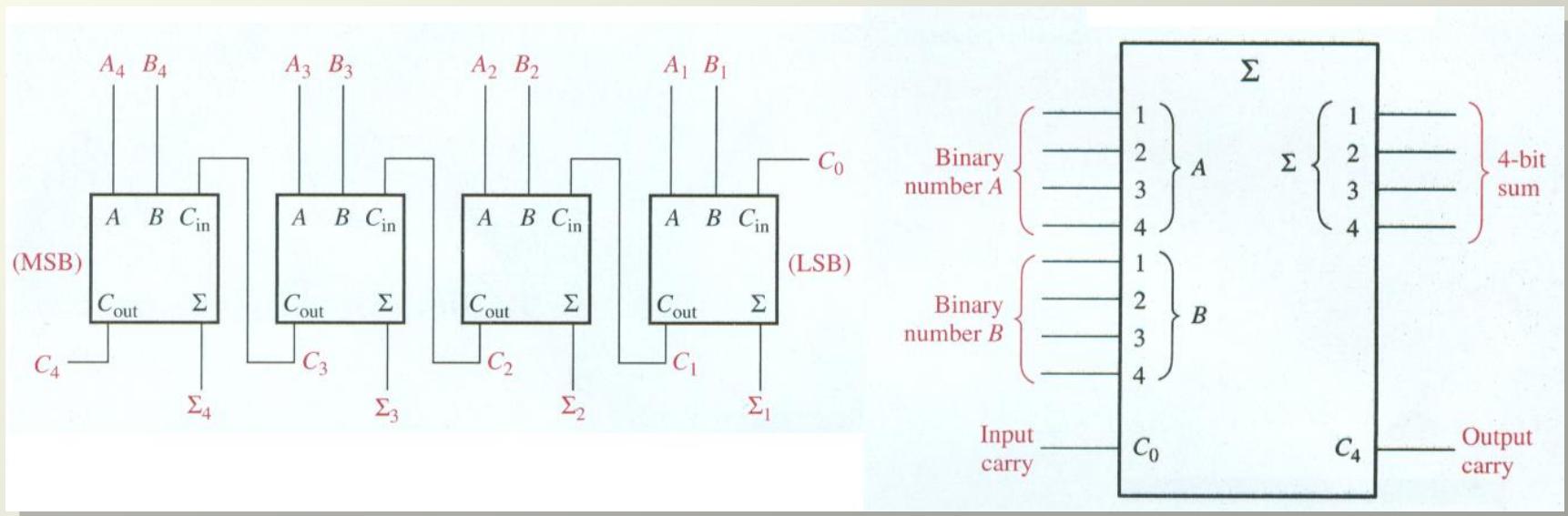
Parallel Binary Adders

- Two-bit parallel binary adder



Parallel Binary Adders

- Four-bit parallel binary adder

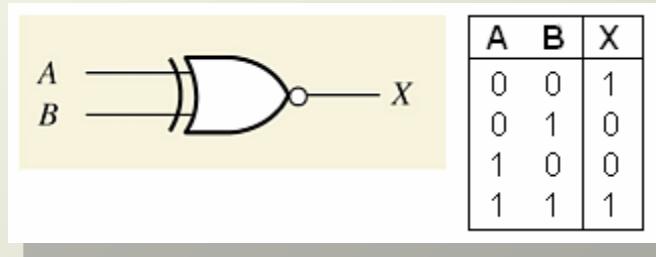


Comparators

- 1-Bit Comparator
- 2-Bit Comparator
- 4-Bit Comparator

Comparators

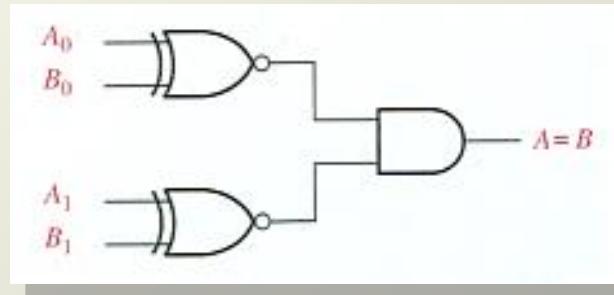
- 1-Bit Comparator



The output is 1 when the inputs are equal

Comparators

- 2-Bit Comparator



The output is 1 when $A_0 = B_0$ AND $A_1 = B_1$

Decoders

Decoders

- Binary decoder
- 4-bit decoder
- BCD-to-decimal decoder
- BCD-to-7-segment decoder

Decoders

- Binary decoder

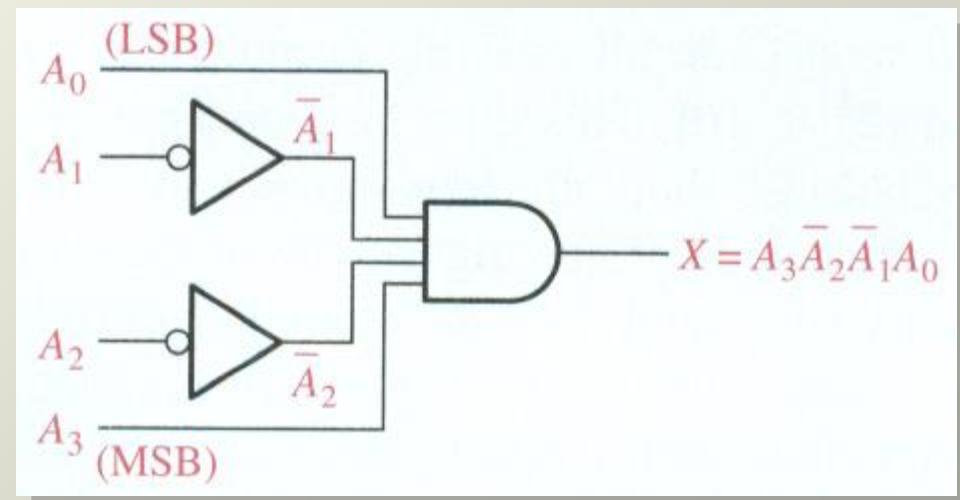
The output is 1 only when:

$$A_0 = 1$$

$$A_1 = 0$$

$$A_2 = 0$$

$$A_3 = 1$$



This is only one of an infinite number of examples

Decoders

- 4-bit decoder

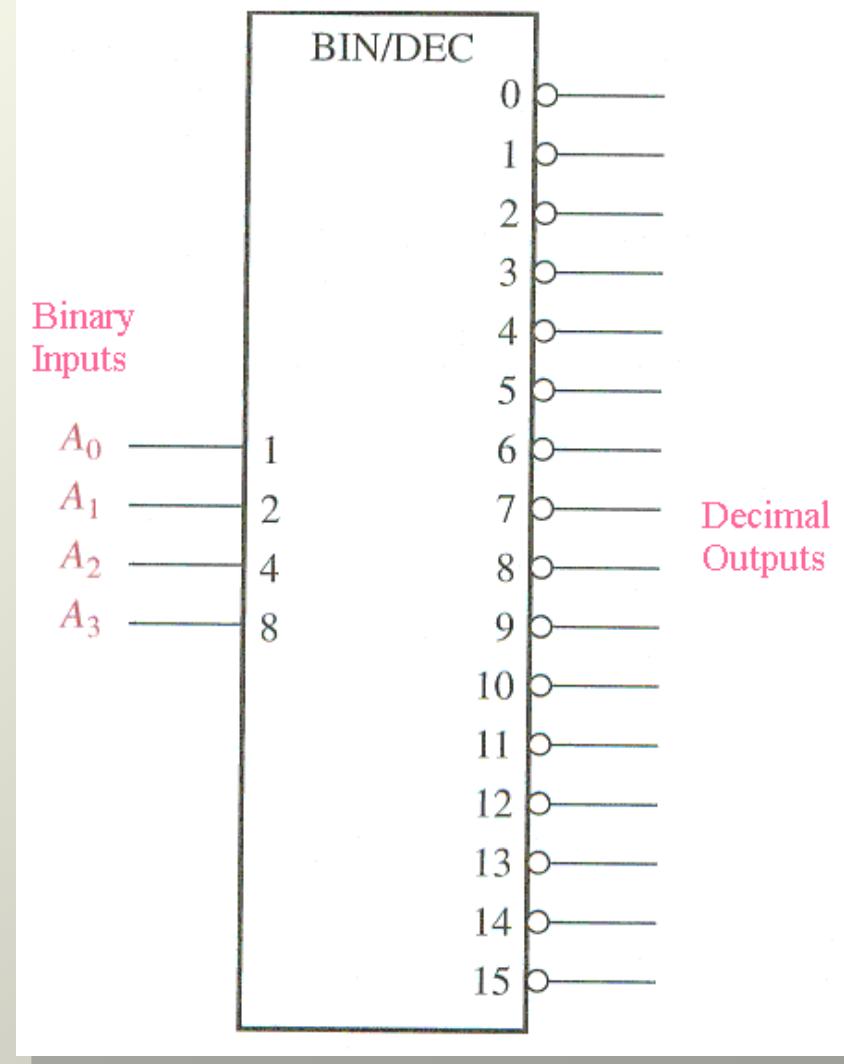
BINARY INPUTS			
A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Logic
Diagram

Decoders

- 4-bit decoder
 - Binary inputs
 - Active-low outputs

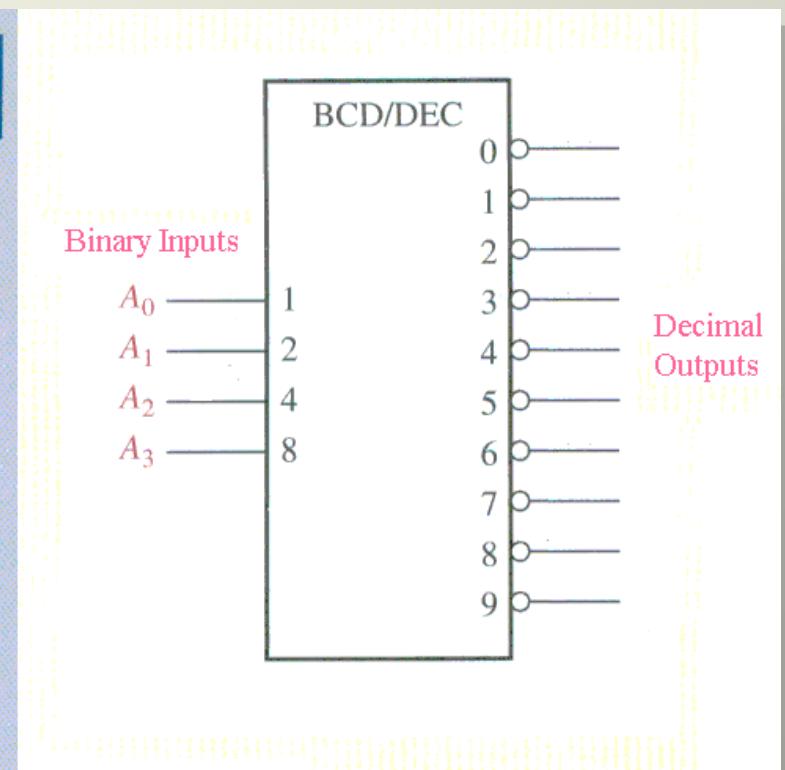
Truth
Table



Decoders

- BCD-to-decimal decoder

DECIMAL DIGIT	BCD CODE				DECODING FUNCTION
	A_3	A_2	A_1	A_0	
0	0	0	0	0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$
1	0	0	0	1	$\bar{A}_3\bar{A}_2\bar{A}_1A_0$
2	0	0	1	0	$\bar{A}_3\bar{A}_2A_1\bar{A}_0$
3	0	0	1	1	$\bar{A}_3\bar{A}_2A_1A_0$
4	0	1	0	0	$\bar{A}_3A_2\bar{A}_1\bar{A}_0$
5	0	1	0	1	$\bar{A}_3A_2\bar{A}_1A_0$
6	0	1	1	0	$\bar{A}_3A_2A_1\bar{A}_0$
7	0	1	1	1	$\bar{A}_3A_2A_1A_0$
8	1	0	0	0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$
9	1	0	0	1	$A_3\bar{A}_2\bar{A}_1A_0$



Decoders

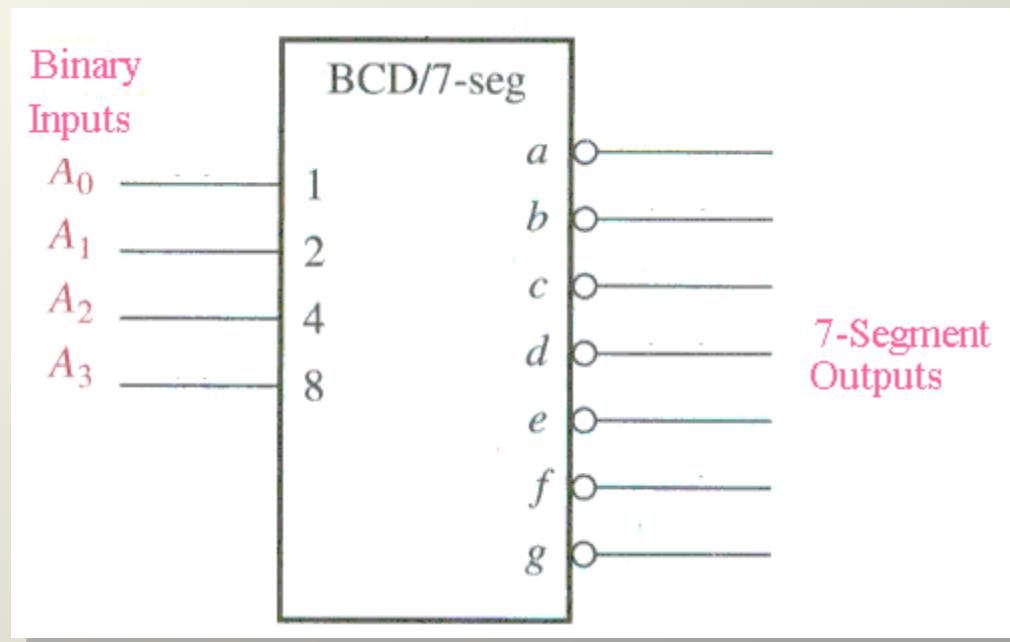
- BCD-to-7-segment decoder

DECIMAL DIGIT	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

Logic
Diagram

Decoders

- BCD-to-7-segment decoder



Truth
Table



Encoders

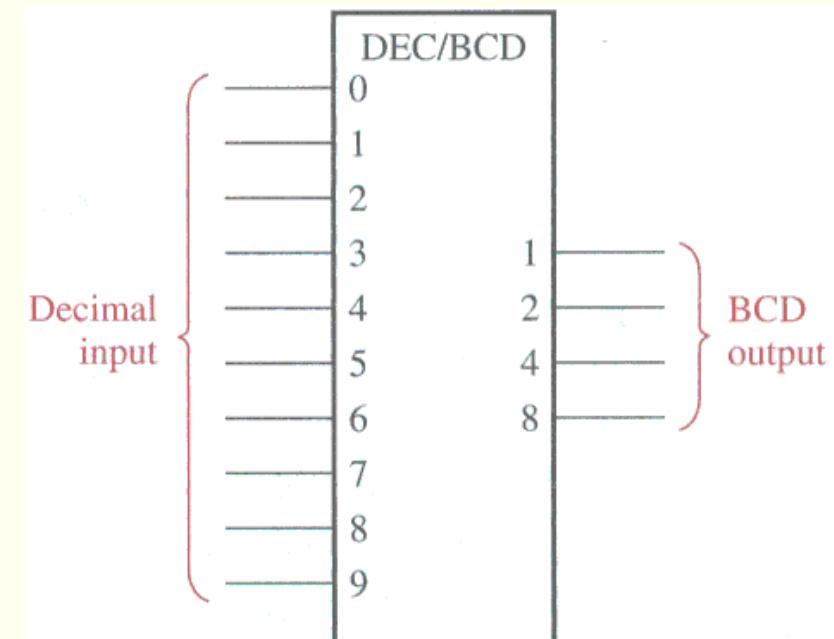
Encoders

- Decimal-to-BCD encoder
- 8-line-to-3-line encoder

Encoders

- Decimal-to-BCD encoder

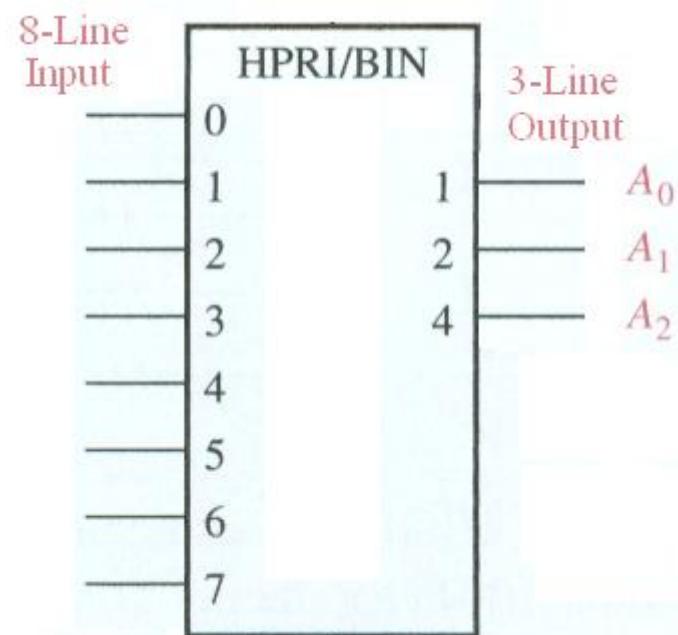
DECIMAL DIGIT	BCD CODE			
	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



Encoders

- 8-line-to-3-line encoder

8-LINE INPUT	3-LINE OUTPUT		
	A_2	A_1	A_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



Code Converters

Code Converters

- BCD-to-binary conversion
- Binary-Gray conversions

Code Converters

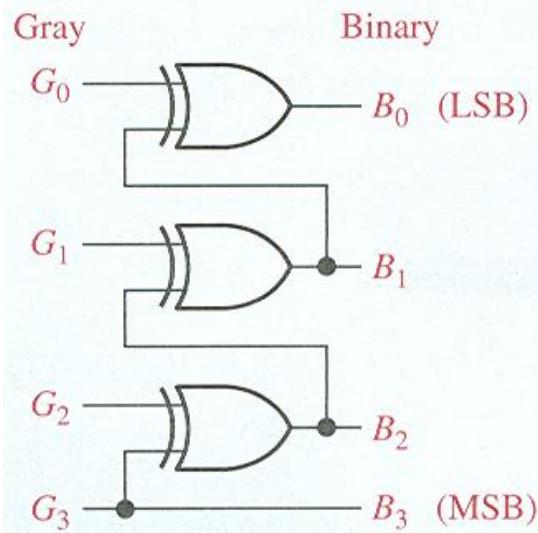
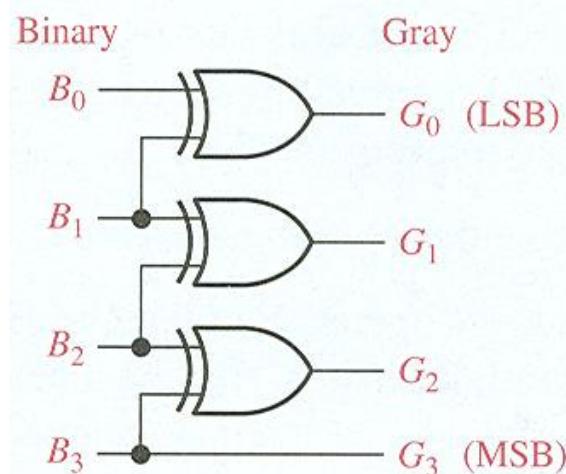
- BCD-to-binary conversion

BCD BIT	BCD WEIGHT	(MSB)		BINARY REPRESENTATION						(LSB)
		64	32	16	8	4	2	1		
A_0	1	0	0	0	0	0	0	0	1	
A_1	2	0	0	0	0	0	1	0	0	
A_2	4	0	0	0	0	1	0	0	0	
A_3	8	0	0	0	1	0	0	0	0	
B_0	10	0	0	0	1	0	1	0	0	
B_1	20	0	0	1	0	1	0	0	0	
B_2	40	0	1	0	1	0	0	0	0	
B_3	80	1	0	1	0	0	0	0	0	

	Tens Digit				Units Digit			
Weight:	80	40	20	10	8	4	2	1
Bit designation:	B_3	B_2	B_1	B_0	A_3	A_2	A_1	A_0

Code Converters

- Binary-Gray conversions



BINARY	GRAY CODE
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

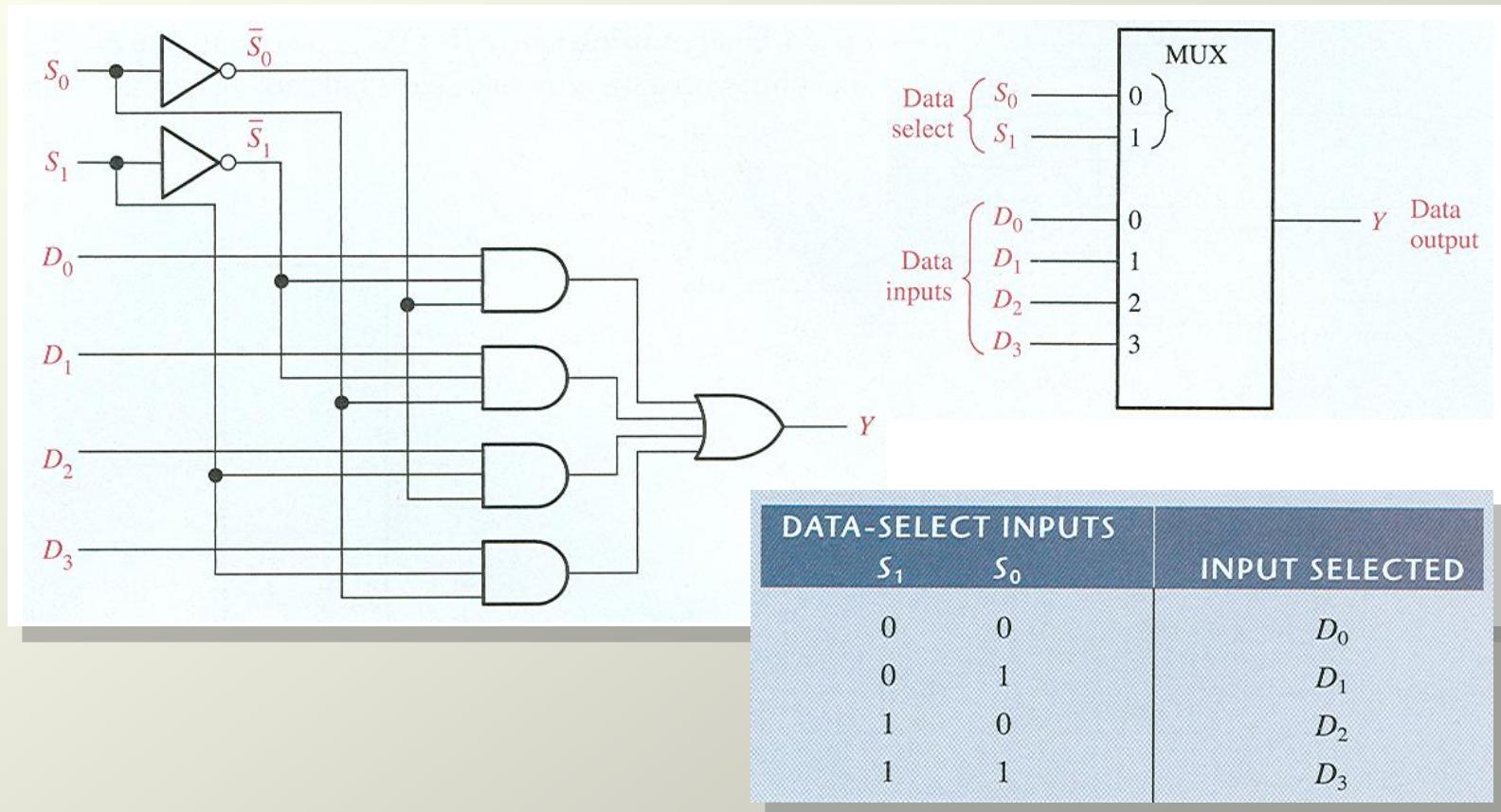
Multiplexers (Data Selectors)

Multiplexers (Data Selectors)

- 4-input multiplexer
- Expanded multiplexers

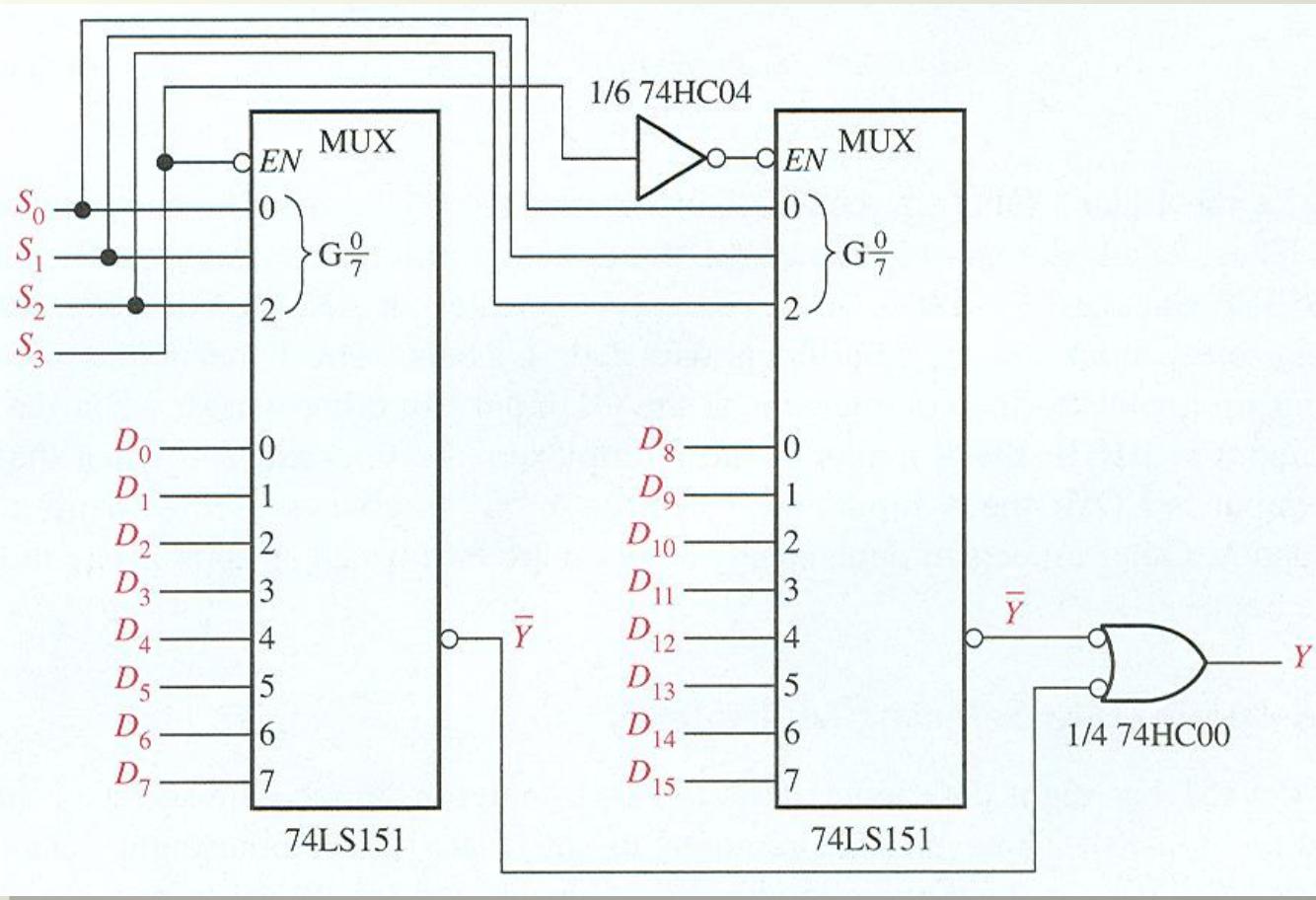
Multiplexers (Data Selectors)

- 4-input multiplexer



Multiplexers (Data Selectors)

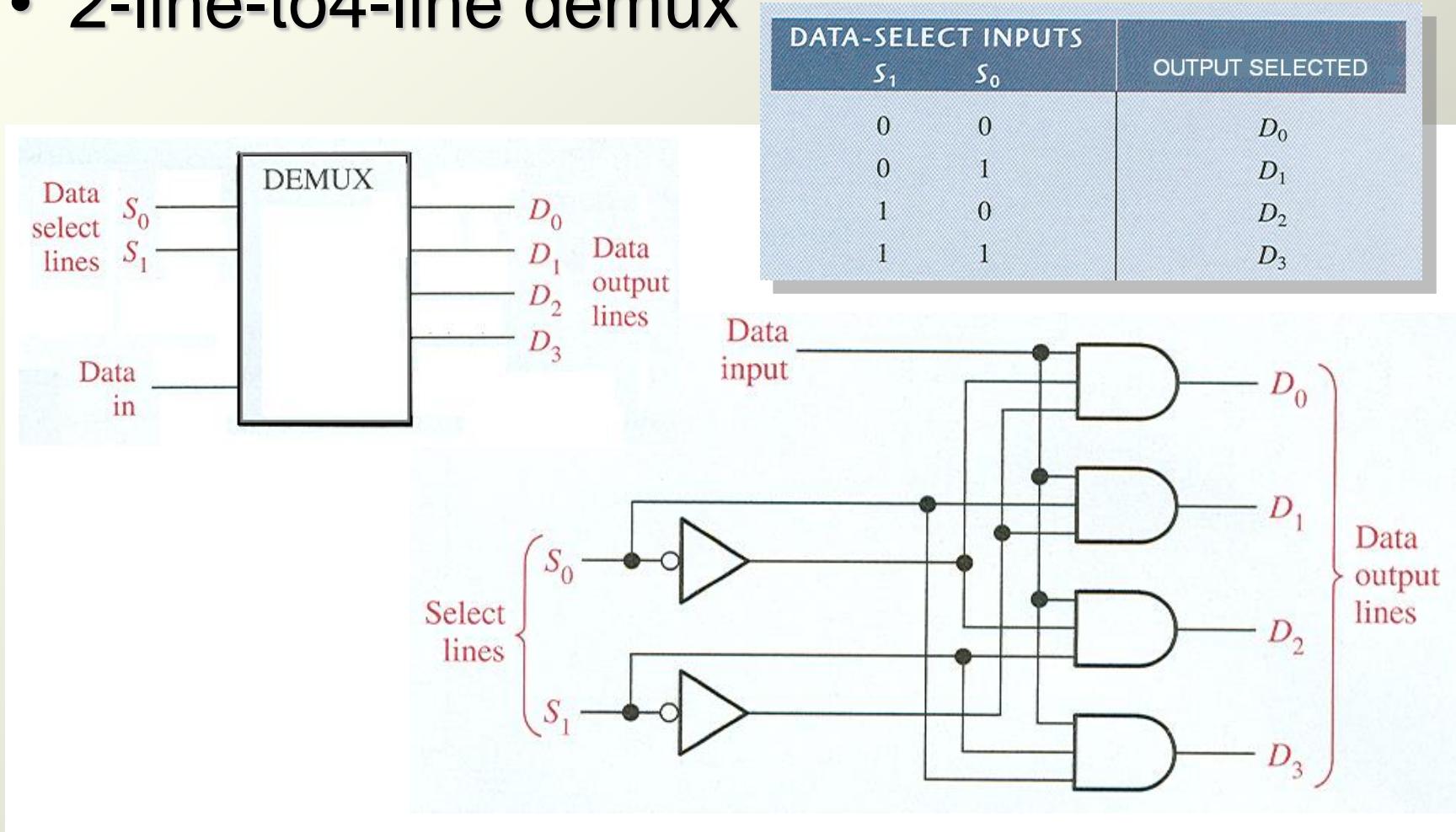
- Expanded multiplexers



Demultiplexers

Demultiplexers

- 2-line-to4-line demux



Parity Generator/Checker

Parity Generators/Checkers

- Parity generator/checker

