| m_counter Project Status (05/19/2021 - 08:10:08) | | | |
|---|---|---|---|
| **Project File:** | Q2.xise | **Parser Errors:** | No Errors |
| **Module Name:** | m_counter | **Implementation State:** | Placed and Routed |
| **Target Device:** | xc6slx16-3csg324 | • **Errors:** | |
| **Product Version:** | ISE 14.7 | • **Warnings:** | |
| **Design Goal:** | Balanced | • **Routing Results:** | All Signals Completely Routed |
| **Design Strategy:** | Xilinx Default (unlocked) | • **Timing Constraints:** | All Constraints Met |
| **Environment:** | System Settings | • **Final Timing Score:** | 0  (Timing Report) |

| Current Errors | [-] |
|---|---|
| No Errors Found | |

| Current Warnings | [-] |
|---|---|
| No Warnings Found | |

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Registers | 27 | 18,224 | 1% | |
| Number used as Flip Flops | 27 | | | |
| Number used as Latches | 0 | | | |
| Number used as Latch-thrus | 0 | | | |
| Number used as AND/OR logics | 0 | | | |
| Number of Slice LUTs | 35 | 9,112 | 1% | |
| Number used as logic | 33 | 9,112 | 1% | |
| Number using O6 output only | 6 | | | |
| Number using O5 output only | 13 | | | |
| Number using O5 and O6 | 14 | | | |
| Number used as ROM | 0 | | | |
| Number used as Memory | 0 | 2,176 | 0% | |
| Number used exclusively as route-thrus | 2 | | | |
| Number with same-slice register load | 0 | | | |
| Number with same-slice carry load | 2 | | | |
| Number with other load | 0 | | | |
| Number of occupied Slices | 14 | 2,278 | 1% | |
| Number of MUXCYs used | 32 | 4,556 | 1% | |
| Number of LUT Flip Flop pairs used | 40 | | | |
| Number with an unused Flip Flop | 13 | 40 | 32% | |
| Number with an unused LUT | 5 | 40 | 12% | |
| Number of fully used LUT-FF pairs | 22 | 40 | 55% | |
| Number of unique control sets | 4 | | | |
| Number of slice register sites lost to control set restrictions | 13 | 18,224 | 1% | |
| Number of bonded IOBs | 49 | 232 | 21% | |
| Number of RAMB16BWERs | 0 | 32 | 0% | |

| | | | | |
|---|---|---|---|---|
| Number of RAMB8BWERs | 0 | 64 | 0% | |
| Number of BUFIO2/BUFIO2_2CLKs | 0 | 32 | 0% | |
| Number of BUFIO2FB/BUFIO2FB_2CLKs | 0 | 32 | 0% | |
| Number of BUFG/BUFGMUXs | 1 | 16 | 6% | |
|    Number used as BUFGs | 1 | | | |
|    Number used as BUFGMUX | 0 | | | |
| Number of DCM/DCM_CLKGENs | 0 | 4 | 0% | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% | |
| Number of IODELAY2/IODRP2/IODRP2_MCBs | 0 | 248 | 0% | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% | |
| Number of BSCANs | 0 | 4 | 0% | |
| Number of BUFHs | 0 | 128 | 0% | |
| Number of BUFPLLs | 0 | 8 | 0% | |
| Number of BUFPLL_MCBs | 0 | 4 | 0% | |
| Number of DSP48A1s | 3 | 32 | 9% | |
| Number of ICAPs | 0 | 1 | 0% | |
| Number of MCBs | 0 | 2 | 0% | |
| Number of PCILOGICSEs | 0 | 2 | 0% | |
| Number of PLL_ADVs | 0 | 2 | 0% | |
| Number of PMVs | 0 | 1 | 0% | |
| Number of STARTUPs | 0 | 1 | 0% | |
| Number of SUSPEND_SYNCs | 0 | 1 | 0% | |
| Average Fanout of Non-Clock Nets | 1.60 | | | |

| Performance Summary | | | | [-] |
|---|---|---|---|---|
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | Pinout Report | |
| **Routing Results:** | All Signals Completely Routed | **Clock Data:** | Clock Report | |
| **Timing Constraints:** | All Constraints Met | | | |

| Failing Constraints | [-] |
|---|---|
| **All Constraints Were Met** | |

| Clock Report | [-] |
|---|---|
| **Data Not Yet Available** | |

| Detailed Reports | | | | | [-] |
|---|---|---|---|---|---|
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** |
| Synthesis Report | Current | Wed May 19 08:09:36 2021 | | | |
| Translation Report | Current | Wed May 19 08:09:45 2021 | 0 | 0 | 0 |
| Map Report | Current | Wed May 19 08:09:53 2021 | 0 | 0 | 6 Infos (0 new) |
| Place and Route Report | Current | Wed May 19 08:10:01 2021 | 0 | 0 | 3 Infos (0 new) |
| Power Report | | | | | |
| Post-PAR Static Timing Report | Current | Wed May 19 08:10:06 2021 | 0 | 0 | 4 Infos (0 new) |

| Bitgen Report | | | | | |
|---|---|---|---|---|---|

| Secondary Reports | |
|---|---|
| **Report Name** | **Status** | **Generated** |

**Date Generated:** 05/19/2021 - 17:24:03