Synthesis Report

Tue Jun 29 23:03:18 2021

```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Reading design: Game.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "Game.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "Game"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324
---- Source Options
Top Module Name                    : Game
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Winner.v" into library wo
Parsing module .
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Decision.v" into library
```

```
Parsing module .
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Correlation.v" into libra
Parsing module .
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Game.v" into library work
Parsing module .
=========================================================================
*                          HDL Elaboration                              *
=========================================================================
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:413 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Correlation.v" Line 12
Elaborating module .
Elaborating module .
=========================================================================
*                          HDL Synthesis                                *
=========================================================================
Synthesizing Unit .
    Related source file is "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Game.v".
        N = 8
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Correlation.v".
        N = 8
    Found 11-bit register for signal .
    Found 11-bit register for signal .
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 26.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 49.
    Found 11-bit adder for signal  created at line 27.
    Found 4-bit adder for signal  created at line 28.
    Found 4-bit comparator greater for signal  created at line 16
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
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    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 1-bit comparator equal for signal  created at line 47
    Found 8-bit comparator equal for signal  created at line 55
    Found 8-bit comparator equal for signal  created at line 55
    Summary:
        inferred  17 Adder/Subtractor(s).
        inferred  26 D-type flip-flop(s).
        inferred  19 Comparator(s).
        inferred  22 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Winner.v".
        N = 8
    Found 11-bit comparator greater for signal  created at line 5
    Found 11-bit comparator greater for signal  created at line 5
    Summary:
        inferred   2 Comparator(s).
        inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q1-s\Q1\Decision.v".
    Found 4-bit register for signal .
    Found 2-bit register for signal .
    Found 4-bit adder for signal  created at line 20.
    Found 4-bit comparator greater for signal  created at line 15
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred   6 D-type flip-flop(s).
        inferred   1 Comparator(s).
        inferred   5 Multiplexer(s).
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 18
 11-bit adder                                          : 16
 4-bit adder                                           : 2
```

```
# Registers                                          : 8
 1-bit register                                      : 4
 11-bit register                                     : 2
 2-bit register                                      : 1
 4-bit register                                      : 1
# Comparators                                        : 22
 1-bit comparator equal                              : 16
 11-bit comparator greater                           : 2
 4-bit comparator greater                            : 2
 8-bit comparator equal                              : 2
# Multiplexers                                       : 28
 11-bit 2-to-1 multiplexer                           : 18
 2-bit 2-to-1 multiplexer                            : 6
 4-bit 2-to-1 multiplexer                            : 4
==========================================================================
==========================================================================
*                        Advanced HDL Synthesis                          *
==========================================================================
==========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                 : 18
 11-bit adder                                        : 16
 4-bit adder                                         : 2
# Registers                                          : 32
 Flip-Flops                                          : 32
# Comparators                                        : 22
 1-bit comparator equal                              : 16
 11-bit comparator greater                           : 2
 4-bit comparator greater                            : 2
 8-bit comparator equal                              : 2
# Multiplexers                                       : 27
 11-bit 2-to-1 multiplexer                           : 18
 2-bit 2-to-1 multiplexer                            : 5
 4-bit 2-to-1 multiplexer                            : 4
==========================================================================
==========================================================================
*                         Low Level Synthesis                            *
==========================================================================
WARNING:Xst:3002 - This design contains one or more registers/latches that are directly
   incompatible with the Spartan6 architecture. The two primary causes of this is
   either a register or latch described with both an asynchronous set and
   asynchronous reset, or a register or latch described with an asynchronous
   set or reset which however has an initialization value of the opposite
   polarity (i.e. asynchronous reset with an initialization value of 1).
    While this circuit can be built, it creates a sub-optimal implementation
   in terms of area, power and performance. For a more optimal implementation
   Xilinx highly recommends one of the following:
          1) Remove either the set or reset from all registers and latches
             if not needed for required functionality
          2) Modify the code in order to produce a synchronous set
             and/or reset (both is preferred)
          3) Ensure all registers have the same initialization value as the
             described asynchronous set or reset polarity
          4) Use the -async_to_sync option to transform the asynchronous
             set/reset to synchronous operation
             (timing simulation highly recommended when using this option)
  Please refer to http://www.xilinx.com search string "Spartan6 asynchronous set/reset" for more details.
  List of register instances with asynchronous set and reset:
    counter_0 in unit
    counter_1 in unit
    counter_2 in unit
    counter_3 in unit
Optimizing unit  ...
Optimizing unit  ...
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Game, actual ratio is 1.
Final Macro Processing ...
==========================================================================
Final Register Report
Macro Statistics
# Registers                                          : 36
 Flip-Flops                                          : 36
==========================================================================
==========================================================================
*                           Partition Report                             *
==========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
==========================================================================
*                            Design Summary                              *
==========================================================================
Top Level Output File Name         : Game.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 198
#      GND                         : 1
#      LUT1                        : 13
#      LUT2                        : 22
#      LUT3                        : 9
#      LUT4                        : 27
#      LUT5                        : 9
#      LUT6                        : 57
#      MUXCY                       : 35
#      MUXF7                       : 2
#      VCC                         : 1
```

```
#      XORCY                       : 22
# FlipFlops/Latches                : 40
#      FDC                         : 32
#      FDP                         : 4
#      LDC                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 27
#      IBUF                        : 25
#      OBUF                        : 2
Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3
Slice Logic Utilization:
 Number of Slice Registers:              40  out of  18224     0%
 Number of Slice LUTs:                  137  out of   9112     1%
    Number used as Logic:               137  out of   9112     1%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    145
   Number with an unused Flip Flop:     105  out of    145    72%
   Number with an unused LUT:             8  out of    145     5%
   Number of fully used LUT-FF pairs:    32  out of    145    22%
   Number of unique control sets:        13
IO Utilization:
 Number of IOs:                         28
 Number of bonded IOBs:                 28  out of    232    12%
Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
-----------------------------------------------------+-------------------------+-------+
Clock Signal                                         | Clock buffer(FF name)   | Load  |
-----------------------------------------------------+-------------------------+-------+
Clock                                                | BUFGP                   | 36    |
c/Reset_counter[3]_AND_8_o(c/Reset_counter[3]_AND_8_o1:O)| NONE(*)(c/counter_0_LDC)| 1     |
c/Reset_counter[3]_AND_6_o(c/Reset_counter[3]_AND_6_o1:O)| NONE(*)(c/counter_1_LDC)| 1     |
c/Reset_counter[3]_AND_4_o(c/Reset_counter[3]_AND_4_o1:O)| NONE(*)(c/counter_2_LDC)| 1     |
c/Reset_counter[3]_AND_2_o(c/Reset_counter[3]_AND_2_o1:O)| NONE(*)(c/counter_3_LDC)| 1     |
-----------------------------------------------------+-------------------------+-------+
(*) These 4 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: 3.600ns (Maximum Frequency: 277.751MHz)
   Minimum input arrival time before clock: 9.775ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default period analysis for Clock 'Clock'
  Clock period: 3.600ns (frequency: 277.751MHz)
  Total number of paths / destination ports: 626 / 44
-------------------------------------------------------------------------
Delay:               3.600ns (Levels of Logic = 2)
  Source:            c/counter_1_P_1 (FF)
  Destination:       c/counter_3_C_3 (FF)
  Source Clock:      Clock rising
  Destination Clock: Clock rising
  Data Path: c/counter_1_P_1 to c/counter_3_C_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDP:C->Q              4   0.447   0.788  c/counter_1_P_1 (c/counter_1_P_1)
     LUT3:I1->O            4   0.203   0.912  c/counter_11_1 (c/counter_11)
     LUT5:I2->O            2   0.205   0.616  c/Reset_counter[3]_AND_3_o1 (c/Reset_counter[3]_AND_3_o)
     FDC:CLR                   0.430          c/counter_3_C_3
    ----------------------------------------
    Total                      3.600ns (1.285ns logic, 2.315ns route)
                               (35.7% logic, 64.3% route)
=========================================================================
Timing constraint: Default period analysis for Clock 'c/Reset_counter[3]_AND_8_o'
  Clock period: 2.661ns (frequency: 375.827MHz)
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Delay:               2.661ns (Levels of Logic = 1)
  Source:            c/counter_0_LDC (LATCH)
  Destination:       c/counter_0_LDC (LATCH)
  Source Clock:      c/Reset_counter[3]_AND_8_o falling
  Destination Clock: c/Reset_counter[3]_AND_8_o falling
  Data Path: c/counter_0_LDC to c/counter_0_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

```
    ----------------------------------------  ------------
     LDC:G->Q              4   0.498   0.912  c/counter_0_LDC (c/counter_0_LDC)
     LUT4:I1->O            2   0.205   0.616  c/Reset_counter[3]_AND_9_o1 (c/Reset_counter[3]_AND_9_o)
     LDC:CLR                   0.430          c/counter_0_LDC
    ----------------------------------------
    Total                      2.661ns (1.133ns logic, 1.528ns route)
                               (42.6% logic, 57.4% route)
=========================================================================
Timing constraint: Default period analysis for Clock 'c/Reset_counter[3]_AND_6_o'
  Clock period: 2.535ns (frequency: 394.508MHz)
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Delay:               2.535ns (Levels of Logic = 1)
  Source:            c/counter_1_LDC (LATCH)
  Destination:       c/counter_1_LDC (LATCH)
  Source Clock:      c/Reset_counter[3]_AND_6_o falling
  Destination Clock: c/Reset_counter[3]_AND_6_o falling
  Data Path: c/counter_1_LDC to c/counter_1_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDC:G->Q              4   0.498   0.788  c/counter_1_LDC (c/counter_1_LDC)
     LUT5:I3->O            2   0.203   0.616  c/Reset_counter[3]_AND_7_o1 (c/Reset_counter[3]_AND_7_o)
     LDC:CLR                   0.430          c/counter_1_LDC
    ----------------------------------------
    Total                      2.535ns (1.131ns logic, 1.404ns route)
                               (44.6% logic, 55.4% route)
=========================================================================
Timing constraint: Default period analysis for Clock 'c/Reset_counter[3]_AND_4_o'
  Clock period: 2.661ns (frequency: 375.827MHz)
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Delay:               2.661ns (Levels of Logic = 1)
  Source:            c/counter_2_LDC (LATCH)
  Destination:       c/counter_2_LDC (LATCH)
  Source Clock:      c/Reset_counter[3]_AND_4_o falling
  Destination Clock: c/Reset_counter[3]_AND_4_o falling
  Data Path: c/counter_2_LDC to c/counter_2_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDC:G->Q              4   0.498   0.912  c/counter_2_LDC (c/counter_2_LDC)
     LUT6:I3->O            2   0.205   0.616  c/Reset_counter[3]_AND_5_o1 (c/Reset_counter[3]_AND_5_o)
     LDC:CLR                   0.430          c/counter_2_LDC
    ----------------------------------------
    Total                      2.661ns (1.133ns logic, 1.528ns route)
                               (42.6% logic, 57.4% route)
=========================================================================
Timing constraint: Default period analysis for Clock 'c/Reset_counter[3]_AND_2_o'
  Clock period: 3.519ns (frequency: 284.192MHz)
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Delay:               3.519ns (Levels of Logic = 2)
  Source:            c/counter_3_LDC (LATCH)
  Destination:       c/counter_3_LDC (LATCH)
  Source Clock:      c/Reset_counter[3]_AND_2_o falling
  Destination Clock: c/Reset_counter[3]_AND_2_o falling
  Data Path: c/counter_3_LDC to c/counter_3_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDC:G->Q              2   0.498   0.845  c/counter_3_LDC (c/counter_3_LDC)
     LUT3:I0->O            2   0.205   0.721  c/counter_31_1 (c/counter_31)
     LUT5:I3->O            2   0.203   0.616  c/Reset_counter[3]_AND_3_o1 (c/Reset_counter[3]_AND_3_o)
     LDC:CLR                   0.430          c/counter_3_LDC
    ----------------------------------------
    Total                      3.519ns (1.336ns logic, 2.183ns route)
                               (38.0% logic, 62.0% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clock'
  Total number of paths / destination ports: 6606 / 72
-------------------------------------------------------------------------
Offset:              9.775ns (Levels of Logic = 16)
  Source:            Target_Num<1> (PAD)
  Destination:       c/Out_2_10 (FF)
  Destination Clock: Clock rising
  Data Path: Target_Num<1> to c/Out_2_10
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            10   1.222   1.201  Target_Num_1_IBUF (Target_Num_1_IBUF)
     LUT6:I1->O            5   0.203   1.079  c/Mmux_n015131 (c/Madd_GND_2_o_GND_2_o_add_37_OUT_lut<1>)
     LUT6:I0->O            1   0.203   0.944  c/Mmux_n0159411 (c/Mmux_n015941)
     LUT6:I0->O            1   0.203   0.000  c/Mmux_n015944_G (N19)
     MUXF7:I1->O           3   0.140   0.879  c/Mmux_n015944 (c/Madd_GND_2_o_GND_2_o_add_49_OUT_lut<2>)
     LUT3:I0->O            1   0.205   0.827  c/Mmux_n01626_SW0 (N6)
     LUT6:I2->O            1   0.203   0.684  c/Mmux_n01626 (c/n0162<4>)
     LUT2:I0->O            1   0.203   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_lut<4> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_lut<4>)
     MUXCY:S->O            1   0.172   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<4> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<4>)
     MUXCY:CI->O           1   0.019   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<5> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<5>)
     MUXCY:CI->O           1   0.019   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<6> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<6>)
     MUXCY:CI->O           1   0.019   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<7> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<7>)
     MUXCY:CI->O           1   0.019   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<8> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<8>)
     MUXCY:CI->O           0   0.019   0.000  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<9> (c/Madd_Out_2[10]_GND_2_o_add_51_OUT_cy<9>)
     XORCY:CI->O           1   0.180   0.827  c/Madd_Out_2[10]_GND_2_o_add_51_OUT_xor<10> (c/Out_2[10]_GND_2_o_add_51_OUT<10>)
     LUT6:I2->O            1   0.203   0.000  c/Mmux_GND_2_o_Out_2[10]_mux_57_OUT21 (c/GND_2_o_Out_2[10]_mux_57_OUT<10>)
     FDC:D                     0.102          c/Out_2_10
    ----------------------------------------
    Total                      9.775ns (3.334ns logic, 6.441ns route)
                               (34.1% logic, 65.9% route)
```

```
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'c/Reset_counter[3]_AND_8_o'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              4.067ns (Levels of Logic = 2)
  Source:            Reset (PAD)
  Destination:       c/counter_0_LDC (LATCH)
  Destination Clock: c/Reset_counter[3]_AND_8_o falling
  Data Path: Reset to c/counter_0_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            36   1.222   1.596  Reset_IBUF (Reset_IBUF)
     LUT4:I0->O            2   0.203   0.616  c/Reset_counter[3]_AND_9_o1 (c/Reset_counter[3]_AND_9_o)
     LDC:CLR                   0.430          c/counter_0_LDC
    ----------------------------------------
    Total                      4.067ns (1.855ns logic, 2.212ns route)
                                       (45.6% logic, 54.4% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'c/Reset_counter[3]_AND_6_o'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              4.164ns (Levels of Logic = 2)
  Source:            Reset (PAD)
  Destination:       c/counter_1_LDC (LATCH)
  Destination Clock: c/Reset_counter[3]_AND_6_o falling
  Data Path: Reset to c/counter_1_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            36   1.222   1.693  Reset_IBUF (Reset_IBUF)
     LUT5:I0->O            2   0.203   0.616  c/Reset_counter[3]_AND_7_o1 (c/Reset_counter[3]_AND_7_o)
     LDC:CLR                   0.430          c/counter_1_LDC
    ----------------------------------------
    Total                      4.164ns (1.855ns logic, 2.309ns route)
                                       (44.5% logic, 55.5% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'c/Reset_counter[3]_AND_4_o'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              4.184ns (Levels of Logic = 2)
  Source:            Reset (PAD)
  Destination:       c/counter_2_LDC (LATCH)
  Destination Clock: c/Reset_counter[3]_AND_4_o falling
  Data Path: Reset to c/counter_2_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            36   1.222   1.713  Reset_IBUF (Reset_IBUF)
     LUT6:I0->O            2   0.203   0.616  c/Reset_counter[3]_AND_5_o1 (c/Reset_counter[3]_AND_5_o)
     LDC:CLR                   0.430          c/counter_2_LDC
    ----------------------------------------
    Total                      4.184ns (1.855ns logic, 2.329ns route)
                                       (44.3% logic, 55.7% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'c/Reset_counter[3]_AND_2_o'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              4.164ns (Levels of Logic = 2)
  Source:            Reset (PAD)
  Destination:       c/counter_3_LDC (LATCH)
  Destination Clock: c/Reset_counter[3]_AND_2_o falling
  Data Path: Reset to c/counter_3_LDC
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            36   1.222   1.693  Reset_IBUF (Reset_IBUF)
     LUT5:I0->O            2   0.203   0.616  c/Reset_counter[3]_AND_3_o1 (c/Reset_counter[3]_AND_3_o)
     LDC:CLR                   0.430          c/counter_3_LDC
    ----------------------------------------
    Total                      4.164ns (1.855ns logic, 2.309ns route)
                                       (44.5% logic, 55.5% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clock'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              3.597ns (Levels of Logic = 1)
  Source:            d/Result_1 (FF)
  Destination:       Result<1> (PAD)
  Source Clock:      Clock rising
  Data Path: d/Result_1 to Result<1>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              1   0.447   0.579  d/Result_1 (d/Result_1)
     OBUF:I->O                 2.571          Result_1_OBUF (Result<1>)
    ----------------------------------------
    Total                      3.597ns (3.018ns logic, 0.579ns route)
                                       (83.9% logic, 16.1% route)
=========================================================================
Cross Clock Domains Report:
--------------------------
Clock to Setup on destination clock Clock
-------------------------+---------+---------+---------+---------+
                         | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock             |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-------------------------+---------+---------+---------+---------+
Clock                    |    3.600|         |         |         |
c/Reset_counter[3]_AND_2_o|         |    3.662|         |         |
```

```
c/Reset_counter[3]_AND_4_o|         |    3.728|         |         |
c/Reset_counter[3]_AND_6_o|         |    3.777|         |         |
c/Reset_counter[3]_AND_8_o|         |    3.696|         |         |
--------------------------+---------+---------+---------+---------+
Clock to Setup on destination clock c/Reset_counter[3]_AND_2_o
--------------------------+---------+---------+---------+---------+
                          | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock              |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
--------------------------+---------+---------+---------+---------+
Clock                     |         |         |    3.600|         |
c/Reset_counter[3]_AND_2_o|         |         |    3.519|         |
c/Reset_counter[3]_AND_4_o|         |         |    3.728|         |
c/Reset_counter[3]_AND_6_o|         |         |    3.777|         |
c/Reset_counter[3]_AND_8_o|         |         |    3.696|         |
--------------------------+---------+---------+---------+---------+
Clock to Setup on destination clock c/Reset_counter[3]_AND_4_o
--------------------------+---------+---------+---------+---------+
                          | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock              |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
--------------------------+---------+---------+---------+---------+
Clock                     |         |         |    3.519|         |
c/Reset_counter[3]_AND_4_o|         |         |    2.661|         |
c/Reset_counter[3]_AND_6_o|         |         |    3.651|         |
c/Reset_counter[3]_AND_8_o|         |         |    3.696|         |
--------------------------+---------+---------+---------+---------+
Clock to Setup on destination clock c/Reset_counter[3]_AND_6_o
--------------------------+---------+---------+---------+---------+
                          | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock              |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
--------------------------+---------+---------+---------+---------+
Clock                     |         |         |    3.519|         |
c/Reset_counter[3]_AND_6_o|         |         |    2.535|         |
c/Reset_counter[3]_AND_8_o|         |         |    3.696|         |
--------------------------+---------+---------+---------+---------+
Clock to Setup on destination clock c/Reset_counter[3]_AND_8_o
--------------------------+---------+---------+---------+---------+
                          | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock              |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
--------------------------+---------+---------+---------+---------+
Clock                     |         |         |    2.484|         |
c/Reset_counter[3]_AND_8_o|         |         |    2.661|         |
--------------------------+---------+---------+---------+---------+
=========================================================================
Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.70 secs

-->
Total memory usage is 4487492 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```