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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.34 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.35 secs

--> Reading design: sequence_detector.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "sequence_detector.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "sequence_detector"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : sequence_detector
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
```

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Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

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=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q3\Q3_1.
v" into library work
Parsing module <sequence_detector>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <sequence_detector>.

=========================================================================
*                           HDL Synthesis                               *
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```
Synthesizing Unit <sequence_detector>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q3\Q3_1.
v".
        s0 = 2'b00
        s1 = 2'b01
        s2 = 2'b10
        s3 = 2'b11
    Found 5-bit register for signal <str>.
    Found 16-bit register for signal <dseq_count>.
    Found 1-bit register for signal <seq_detected>.
    Found 16-bit adder for signal <temp_dseq_count[15]_GND_1_o_add_17_OUT> created at line
79.
    Found 1-bit 4-to-1 multiplexer for signal <GND_1_o_input_seq_MUX_20_o> created at line
64.
    Found 16-bit 4-to-1 multiplexer for signal
<temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT> created at line 64.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred  22 D-type flip-flop(s).
        inferred   7 Multiplexer(s).
Unit <sequence_detector> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 16-bit adder                                         : 1
# Registers                                            : 3
 1-bit register                                       : 1
 16-bit register                                      : 1
 5-bit register                                       : 1
# Multiplexers                                         : 7
 1-bit 4-to-1 multiplexer                             : 1
 16-bit 2-to-1 multiplexer                            : 5
 16-bit 4-to-1 multiplexer                            : 1

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=========================================================================
*                      Advanced HDL Synthesis                           *
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=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 16-bit adder                                         : 1
# Registers                                            : 22
 Flip-Flops                                           : 22
# Multiplexers                                         : 7
 1-bit 4-to-1 multiplexer                             : 1
 16-bit 2-to-1 multiplexer                            : 5
 16-bit 4-to-1 multiplexer                            : 1

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*                      Low Level Synthesis                      *
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Optimizing unit <sequence_detector> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block sequence_detector, actual ratio is 0.
FlipFlop str_4 has been replicated 1 time(s) to handle iob=true attribute.

Final Macro Processing ...

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Final Register Report

Macro Statistics
# Registers                                          : 23
 Flip-Flops                                          : 23

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================================================================================
*                        Partition Report                        *
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Partition Implementation Status
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  No Partitions were found in this design.

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================================================================================
*                         Design Summary                         *
================================================================================

Top Level Output File Name         : sequence_detector.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 71
#      GND                         : 1
#      INV                         : 1
#      LUT1                        : 15
#      LUT3                        : 2
#      LUT4                        : 16
#      LUT6                        : 3
#      MUXCY                       : 15
#      MUXF7                       : 1
#      VCC                         : 1
#      XORCY                       : 16
# FlipFlops/Latches                : 23
#      FD_1                        : 23
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 26
#      IBUF                        : 4
#      OBUF                        : 22

Device utilization summary:
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```

Selected Device : 6slx16csg324-3

Slice Logic Utilization:
 Number of Slice Registers: 22 out of 18224   0%
 Number of Slice LUTs: 37 out of   9112   0%
    Number used as Logic: 37 out of   9112   0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 42
   Number with an unused Flip Flop: 20 out of   42   47%
   Number with an unused LUT: 5 out of   42   11%
   Number of fully used LUT-FF pairs: 17 out of   42   40%
   Number of unique control sets: 1

IO Utilization:
 Number of IOs: 27
 Number of bonded IOBs: 27 out of   232   11%
    IOB Flip Flops/Latches: 1

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs: 1 out of   16   6%

Partition Resource Summary:

  No Partitions were found in this design.

==
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

+-----------------------------------+------------------------+-------+
Clock Signal | Clock buffer(FF name) | Load |
+-----------------------------------+------------------------+-------+
clk | BUFGP | 23 |
+-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

   Minimum period: 3.211ns (Maximum Frequency: 311.468MHz)
   Minimum input arrival time before clock: 3.966ns
   Maximum output required time after clock: 3.762ns
   Maximum combinational path delay: No path found

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Timing Details:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.211ns (frequency: 311.468MHz)
  Total number of paths / destination ports: 274 / 21
-------------------------------------------------------------------------
Delay:               3.211ns (Levels of Logic = 3)
  Source:            str_3 (FF)
  Destination:       temp_dseq_count_0 (FF)
  Source Clock:      clk falling
  Destination Clock: clk falling

  Data Path: str_3 to temp_dseq_count_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD_1:C->Q             6   0.447   1.109  str_3 (str_3)
     LUT6:I0->O            1   0.203   0.000
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17_G (N11)
     MUXF7:I1->O          16   0.140   1.005
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17
(Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17)
     LUT4:I3->O            1   0.205   0.000
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT161
(temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT<9>)
     FD_1:D                    0.102          temp_dseq_count_9
    ----------------------------------------
    Total                      3.211ns (1.097ns logic, 2.114ns route)
                                       (34.2% logic, 65.8% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 118 / 19
-------------------------------------------------------------------------
Offset:              3.966ns (Levels of Logic = 4)
  Source:            input_seq (PAD)
  Destination:       temp_dseq_count_0 (FF)
  Destination Clock: clk falling

  Data Path: input_seq to temp_dseq_count_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   1.222   1.089  input_seq_IBUF (input_seq_IBUF)
     LUT6:I1->O            1   0.203   0.000
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17_G (N11)
     MUXF7:I1->O          16   0.140   1.005
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17
(Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT17)
     LUT4:I3->O            1   0.205   0.000
Mmux_temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT161
(temp_dseq_count[15]_temp_dseq_count[15]_mux_22_OUT<9>)
     FD_1:D                    0.102          temp_dseq_count_9
    ----------------------------------------
    Total                      3.966ns (1.872ns logic, 2.094ns route)
                                       (47.2% logic, 52.8% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 22 / 22
--------------------------------------------------------------------------------
Offset:              3.762ns (Levels of Logic = 1)
  Source:            str_3 (FF)
  Destination:       str<3> (PAD)
  Source Clock:      clk falling

  Data Path: str_3 to str<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD_1:C->Q             6   0.447   0.744  str_3 (str_3)
     OBUF:I->O                 2.571          str_3_OBUF (str<3>)
    ----------------------------------------
    Total                      3.762ns (3.018ns logic, 0.744ns route)
                                       (80.2% logic, 19.8% route)

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Cross Clock Domains Report:
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Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |         |         |    3.211|         |
---------------+---------+---------+---------+---------+

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Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.78 secs

-->

Total memory usage is 4487500 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```