Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.24 secs

--> Reading design: m_counter.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "m_counter.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "m_counter"
Output Format   : NGC
Target Device   : xc6slx16-3-csg324

---- Source Options
Top Module Name   : m_counter
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q2\Q2_1.
v" into library work
Parsing module <m_counter>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <m_counter>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================
```

```
Synthesizing Unit <m_counter>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q2\Q2_1.
v".
    Found 1-bit register for signal <temp_pulse2000>.
    Found 1-bit register for signal <temp_pulse5000>.
    Found 9-bit register for signal <c_1000>.
    Found 8-bit register for signal <c_2000>.
    Found 7-bit register for signal <c_5000>.
    Found 1-bit register for signal <temp_pulse1000>.
    Found 19-bit adder for signal <n0068> created at line 49.
    Found 19-bit adder for signal <c_1000[8]_c_5000[6]_add_7_OUT> created at line 49.
    Found 9-bit adder for signal <temp_c_1000[8]_GND_1_o_add_12_OUT> created at line 65.
    Found 8-bit adder for signal <temp_c_2000[7]_GND_1_o_add_16_OUT> created at line 68.
    Found 7-bit adder for signal <temp_c_5000[6]_GND_1_o_add_20_OUT> created at line 71.
    Found 9x10-bit multiplier for signal <n0065> created at line 49.
    Found 8x11-bit multiplier for signal <n0066> created at line 49.
    Found 7x13-bit multiplier for signal <n0048> created at line 49.
    Found 19-bit comparator lessequal for signal <n0008> created at line 49
    Summary:
        inferred   3 Multiplier(s).
        inferred   5 Adder/Subtractor(s).
        inferred  27 D-type flip-flop(s).
        inferred   1 Comparator(s).
Unit <m_counter> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Multipliers                                          : 3
 10x9-bit multiplier                                   : 1
 11x8-bit multiplier                                   : 1
 13x7-bit multiplier                                   : 1
# Adders/Subtractors                                   : 5
 19-bit adder                                          : 2
 7-bit adder                                           : 1
 8-bit adder                                           : 1
 9-bit adder                                           : 1
# Registers                                            : 6
 1-bit register                                        : 3
 7-bit register                                        : 1
 8-bit register                                        : 1
 9-bit register                                        : 1
# Comparators                                          : 1
 19-bit comparator lessequal                           : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


Synthesizing (advanced) Unit <m_counter>.
The following registers are absorbed into counter <temp_c_1000>: 1 register on signal
<temp_c_1000>.
The following registers are absorbed into counter <temp_c_2000>: 1 register on signal
<temp_c_2000>.
The following registers are absorbed into counter <temp_c_5000>: 1 register on signal
<temp_c_5000>.
```

Multiplier <Mmult_n0048> in block <m_counter> and adder/subtractor <Madd_c_1000[8]_c_5000[6]_add_7_OUT> in block <m_counter> are combined into a MAC<Maddsub_n0048>.
Multiplier <Mmult_n0065> in block <m_counter> and adder/subtractor <Madd_n0068> in block <m_counter> are combined into a MAC<Maddsub_n0065>.
Unit <m_counter> synthesized (advanced).

===
Advanced HDL Synthesis Report

Macro Statistics
MACs : 2
 10x9-to-19-bit MAC : 1
 13x7-to-19-bit MAC : 1
Multipliers : 1
 11x8-bit multiplier : 1
Counters : 3
 7-bit up counter : 1
 8-bit up counter : 1
 9-bit up counter : 1
Registers : 3
 Flip-Flops : 3
Comparators : 1
 19-bit comparator lessequal : 1

===

===
*   Low Level Synthesis   *
===

Optimizing unit <m_counter> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block m_counter, actual ratio is 0.

Final Macro Processing ...

===
Final Register Report

Macro Statistics
Registers : 27
 Flip-Flops : 27

===

===
*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Design Summary   *

```
=========================================================================

Top Level Output File Name         : m_counter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 91
#      GND                         : 1
#      INV                         : 4
#      LUT1                        : 15
#      LUT2                        : 4
#      LUT3                        : 3
#      LUT4                        : 19
#      LUT5                        : 2
#      LUT6                        : 1
#      MUXCY                       : 24
#      VCC                         : 1
#      XORCY                       : 17
# FlipFlops/Latches                : 27
#      FDR                         : 3
#      FDRE                        : 24
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 48
#      IBUF                        : 23
#      OBUF                        : 25
# DSPs                             : 3
#      DSP48A1                     : 3

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              27  out of  18224     0%
 Number of Slice LUTs:                   48  out of   9112     0%
    Number used as Logic:                48  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     48
   Number with an unused Flip Flop:      21  out of     48    43%
   Number with an unused LUT:             0  out of     48     0%
   Number of fully used LUT-FF pairs:    27  out of     48    56%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                          49
 Number of bonded IOBs:                  49  out of    232    21%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
 Number of DSP48A1s:                     3  out of     32     9%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.
```

```
--------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
Clock                              | BUFGP                  | 28    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.228ns (Maximum Frequency: 309.823MHz)
   Minimum input arrival time before clock: 3.671ns
   Maximum output required time after clock: 15.598ns
   Maximum combinational path delay: 6.742ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'Clock'
  Clock period: 3.228ns (frequency: 309.823MHz)
  Total number of paths / destination ports: 162 / 56
-------------------------------------------------------------------------
Delay:               3.228ns (Levels of Logic = 2)
  Source:            temp_c_5000_4 (FF)
  Destination:       Maddsub_n0048 (DSP)
  Source Clock:      Clock rising
  Destination Clock: Clock rising

  Data Path: temp_c_5000_4 to Maddsub_n0048
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             4   0.447   1.028  temp_c_5000_4 (temp_c_5000_4)
     LUT5:I0->O            1   0.203   0.580  Mcount_temp_c_5000_cy<4>11
(Mcount_temp_c_5000_cy<4>)
     LUT3:I2->O            2   0.205   0.616  Mcount_temp_c_5000_xor<6>11 (Result<6>2)
     DSP48A1:A6                0.149          Maddsub_n0048
    ----------------------------------------
    Total                      3.228ns (1.004ns logic, 2.224ns route)
                                       (31.1% logic, 68.9% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clock'
```

```
  Total number of paths / destination ports: 56 / 56
--------------------------------------------------------------------------
Offset:              3.671ns (Levels of Logic = 2)
  Source:            Reset (PAD)
  Destination:       temp_pulse2000 (FF)
  Destination Clock: Clock rising

  Data Path: Reset to temp_pulse2000
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.579  Reset_IBUF (Reset_IBUF)
     INV:I->O             28   0.206   1.234  Reset_inv1_INV_0 (Reset_inv)
     FDR:R                     0.430          temp_pulse2000
    ----------------------------------------
    Total                      3.671ns (1.858ns logic, 1.813ns route)
                                       (50.6% logic, 49.4% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clock'
  Total number of paths / destination ports: 698029 / 25
--------------------------------------------------------------------------
Offset:              15.598ns (Levels of Logic = 15)
  Source:            temp_c_2000_7 (FF)
  Destination:       Out (PAD)
  Source Clock:      Clock rising

  Data Path: temp_c_2000_7 to Out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             3   0.447   0.650  temp_c_2000_7 (temp_c_2000_7)
     DSP48A1:A7->PCOUT47    1   4.469   0.000  Mmult_n0066
(Mmult_n0066_PCOUT_to_Maddsub_n0065_PCIN_47)
     DSP48A1:PCIN47->PCOUT47    1   2.265   0.000  Maddsub_n0065
(Maddsub_n0065_PCOUT_to_Maddsub_n0048_PCIN_47)
     DSP48A1:PCIN47->P0    2   2.264   0.845  Maddsub_n0048
(c_1000[8]_c_5000[6]_add_7_OUT<0>)
     LUT4:I1->O            1   0.205   0.000  Mcompar_Out_lut<0> (Mcompar_Out_lut<0>)
     MUXCY:S->O            1   0.172   0.000  Mcompar_Out_cy<0> (Mcompar_Out_cy<0>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<1> (Mcompar_Out_cy<1>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<2> (Mcompar_Out_cy<2>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<3> (Mcompar_Out_cy<3>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<4> (Mcompar_Out_cy<4>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<5> (Mcompar_Out_cy<5>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<6> (Mcompar_Out_cy<6>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<7> (Mcompar_Out_cy<7>)
     MUXCY:CI->O           1   0.213   0.580  Mcompar_Out_cy<8> (Mcompar_Out_cy<8>)
     LUT3:I2->O            1   0.205   0.579  Mcompar_Out_cy<9> (Out_OBUF)
     OBUF:I->O                 2.571          Out_OBUF (Out)
    ----------------------------------------
    Total                     15.598ns (12.944ns logic, 2.654ns route)
                                       (83.0% logic, 17.0% route)

==========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 37 / 1
--------------------------------------------------------------------------
Delay:               6.742ns (Levels of Logic = 13)
  Source:            Count_m<0> (PAD)
  Destination:       Out (PAD)
```

```
  Data Path: Count_m<0> to Out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.222   0.864  Count_m_0_IBUF (Count_m_0_IBUF)
     LUT4:I0->O            1   0.203   0.000  Mcompar_Out_lut<0> (Mcompar_Out_lut<0>)
     MUXCY:S->O            1   0.172   0.000  Mcompar_Out_cy<0> (Mcompar_Out_cy<0>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<1> (Mcompar_Out_cy<1>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<2> (Mcompar_Out_cy<2>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<3> (Mcompar_Out_cy<3>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<4> (Mcompar_Out_cy<4>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<5> (Mcompar_Out_cy<5>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<6> (Mcompar_Out_cy<6>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_Out_cy<7> (Mcompar_Out_cy<7>)
     MUXCY:CI->O           1   0.213   0.580  Mcompar_Out_cy<8> (Mcompar_Out_cy<8>)
     LUT3:I2->O            1   0.205   0.579  Mcompar_Out_cy<9> (Out_OBUF)
     OBUF:I->O                 2.571          Out_OBUF (Out)
    ----------------------------------------
    Total                      6.742ns (4.719ns logic, 2.023ns route)
                                       (70.0% logic, 30.0% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock Clock
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clock          |    3.228|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 6.19 secs

-->

Total memory usage is 4492192 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```