Synthesis Report

Tue Jun 29 23:31:17 2021

```
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.24 secs

--> Reading design: testCorrelation_32.prj
TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report
=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "testCorrelation_32.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "testCorrelation_32"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324
---- Source Options
Top Module Name                    : testCorrelation_32
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\Correlation_32.v" into li
Parsing module .
Analyzing Verilog file "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v" int
```

```
Parsing module .
=========================================================================
*                            HDL Elaboration                            *
=========================================================================
Elaborating module .
WARNING:HDLCompiler:872 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v"
WARNING:HDLCompiler:817 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v"
WARNING:HDLCompiler:872 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v"
Elaborating module .
WARNING:HDLCompiler:413 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\Correlation_32.v" Line
WARNING:HDLCompiler:1127 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v"
WARNING:Xst:2972 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v" line 9.
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Synthesizing Unit .
    Related source file is "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v"
        N = 32
INFO:Xst:3210 - "C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw4_9816603\Q2-s\Q2\TestCorrelation_32.v" line 9: Ou
    Summary:
        no macro.
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Found no macro
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Found no macro
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block testCorrelation_32, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                            Partition Report                           *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                            Design Summary                             *
=========================================================================
Top Level Output File Name         : testCorrelation_32.ngc
Primitive and Black Box Usage:
------------------------------
Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3
Slice Logic Utilization:
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      0
   Number with an unused Flip Flop:       0  out of      0
   Number with an unused LUT:             0  out of      0
   Number of fully used LUT-FF pairs:     0  out of      0
   Number of unique control sets:         0
IO Utilization:
 Number of IOs:                           0
 Number of bonded IOBs:                   0  out of    232     0%
Specific Feature Utilization:
-----------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: No path found
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Cross Clock Domains Report:
```

```
-------------------------
=========================================================================
Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.18 secs

-->
Total memory usage is 4503684 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    6 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```