Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.44 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.44 secs

--> Reading design: myReg.prj

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===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "myReg.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "myReg"
Output Format   : NGC
Target Device   : xc6slx16-3-csg324

---- Source Options
Top Module Name   : myReg
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_1.
v" into library work
Parsing module <myReg>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <myReg>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================
```

```
Synthesizing Unit <myReg>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_1.
v".
    Found 1-bit register for signal <serial_out>.
    Found 8-bit register for signal <qdata>.
    Summary:
        inferred   9 D-type flip-flop(s).
        inferred   3 Multiplexer(s).
Unit <myReg> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                          : 2
 1-bit register                                      : 1
 8-bit register                                      : 1
# Multiplexers                                       : 3
 1-bit 2-to-1 multiplexer                            : 1
 8-bit 2-to-1 multiplexer                            : 2

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                          : 9
 Flip-Flops                                          : 9
# Multiplexers                                       : 3
 1-bit 2-to-1 multiplexer                            : 1
 8-bit 2-to-1 multiplexer                            : 2

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <myReg> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block myReg, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 9
 Flip-Flops                                          : 9

=========================================================================
```

```
================================================================================
*                            Partition Report                                  *
================================================================================

Partition Implementation Status
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  No Partitions were found in this design.

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================================================================================
*                             Design Summary                                   *
================================================================================

Top Level Output File Name         : myReg.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 11
#      LUT2                        : 1
#      LUT3                        : 2
#      LUT5                        : 8
# FlipFlops/Latches                : 9
#      FDRE                        : 9
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 22
#      IBUF                        : 13
#      OBUF                        : 9

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              9  out of  18224     0%
 Number of Slice LUTs:                  11  out of   9112     0%
    Number used as Logic:               11  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    11
   Number with an unused Flip Flop:      2  out of     11    18%
   Number with an unused LUT:            0  out of     11     0%
   Number of fully used LUT-FF pairs:    9  out of     11    81%
   Number of unique control sets:        2

IO Utilization:
 Number of IOs:                         23
 Number of bonded IOBs:                 23  out of    232     9%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:              1  out of     16     6%

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Partition Resource Summary:
---------------------------
```

```
  No Partitions were found in this design.

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=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 9     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.507ns (Maximum Frequency: 663.460MHz)
   Minimum input arrival time before clock: 3.663ns
   Maximum output required time after clock: 3.668ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.507ns (frequency: 663.460MHz)
  Total number of paths / destination ports: 16 / 9
-------------------------------------------------------------------------
Delay:               1.507ns (Levels of Logic = 1)
  Source:            qdata_2 (FF)
  Destination:       qdata_1 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: qdata_2 to qdata_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             3   0.447   0.755  qdata_2 (qdata_2)
     LUT5:I3->O            1   0.203   0.000  Mmux_qdata[7]_pdata[7]_mux_3_OUT21
(qdata[7]_pdata[7]_mux_3_OUT<1>)
     FDRE:D                    0.102          qdata_1
    ----------------------------------------
    Total                      1.507ns (0.752ns logic, 0.755ns route)
                                       (49.9% logic, 50.1% route)

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```
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 64 / 27
-------------------------------------------------------------------------
Offset:              3.663ns (Levels of Logic = 2)
  Source:            shift_right (PAD)
  Destination:       qdata_0 (FF)
  Destination Clock: clk rising

  Data Path: shift_right to qdata_0
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            10   1.222   1.085  shift_right_IBUF (shift_right_IBUF)
     LUT3:I0->O            9   0.205   0.829  _n0020_inv11 (_n0020_inv1)
     FDRE:CE                   0.322          serial_out
    ----------------------------------------
    Total                      3.663ns (1.749ns logic, 1.914ns route)
                                       (47.8% logic, 52.2% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 9 / 9
-------------------------------------------------------------------------
Offset:              3.668ns (Levels of Logic = 1)
  Source:            qdata_7 (FF)
  Destination:       qdata<7> (PAD)
  Source Clock:      clk rising

  Data Path: qdata_7 to qdata<7>
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             3   0.447   0.650  qdata_7 (qdata_7)
     OBUF:I->O                 2.571          qdata_7_OBUF (qdata<7>)
    ----------------------------------------
    Total                      3.668ns (3.018ns logic, 0.650ns route)
                                       (82.3% logic, 17.7% route)

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Cross Clock Domains Report:
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Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    1.507|         |         |         |
---------------+---------+---------+---------+---------+

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Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 8.20 secs

-->

Total memory usage is 4487500 kilobytes
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```
Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```