```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.58 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.59 secs

--> Reading design: SixtyFourThirtyTwoBitMyReg.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "SixtyFourThirtyTwoBitMyReg.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "SixtyFourThirtyTwoBitMyReg"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : SixtyFourThirtyTwoBitMyReg
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
```

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_1.
v" into library work
Parsing module <myReg>.
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_2.
v" into library work
Parsing module <thirtyTwoBitMyReg>.
Parsing module <SixtyFourThirtyTwoBitMyReg>.

=========================================================================
*                          HDL Elaboration                              *
=========================================================================

Elaborating module <SixtyFourThirtyTwoBitMyReg>.
```

```
Elaborating module <thirtyTwoBitMyReg>.

Elaborating module <myReg>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <SixtyFourThirtyTwoBitMyReg>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_2.
v".
    Found 1-bit 64-to-1 multiplexer for signal <serial_out_reg> created at line 69.
    Found 32-bit 64-to-1 multiplexer for signal <data_out_reg> created at line 71.
    Found 1-bit tristate buffer for signal <data_out<0>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<1>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<2>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<3>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<4>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<5>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<6>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<7>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<8>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<9>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<10>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<11>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<12>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<13>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<14>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<15>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<16>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<17>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<18>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<19>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<20>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<21>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<22>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<23>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<24>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<25>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<26>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<27>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<28>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<29>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<30>> created at line 85
    Found 1-bit tristate buffer for signal <data_out<31>> created at line 85
    Found 1-bit tristate buffer for signal <serial_out> created at line 88
    Summary:
        inferred   8 Multiplexer(s).
        inferred  33 Tristate(s).
Unit <SixtyFourThirtyTwoBitMyReg> synthesized.

Synthesizing Unit <thirtyTwoBitMyReg>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_2.
v".
    Summary:
        no macro.
Unit <thirtyTwoBitMyReg> synthesized.
```

```
Synthesizing Unit <myReg>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q1\Q1_1.
v".
    Found 1-bit register for signal <serial_out>.
    Found 8-bit register for signal <qdata>.
    Summary:
        inferred   9 D-type flip-flop(s).
        inferred   3 Multiplexer(s).
Unit <myReg> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                          : 512
 1-bit register                                     : 256
 8-bit register                                     : 256
# Multiplexers                                       : 776
 1-bit 2-to-1 multiplexer                           : 256
 1-bit 64-to-1 multiplexer                          : 1
 32-bit 64-to-1 multiplexer                         : 1
 64-bit 2-to-1 multiplexer                          : 6
 8-bit 2-to-1 multiplexer                           : 512
# Tristates                                          : 33
 1-bit tristate buffer                              : 33

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                          : 2304
 Flip-Flops                                         : 2304
# Multiplexers                                       : 776
 1-bit 2-to-1 multiplexer                           : 256
 1-bit 64-to-1 multiplexer                          : 1
 32-bit 64-to-1 multiplexer                         : 1
 64-bit 2-to-1 multiplexer                          : 6
 8-bit 2-to-1 multiplexer                           : 512

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================

Optimizing unit <SixtyFourThirtyTwoBitMyReg> ...

Optimizing unit <myReg> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block SixtyFourThirtyTwoBitMyReg, actual ratio
is 56.
```

```
Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                             : 2304
 Flip-Flops                                             : 2304

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : SixtyFourThirtyTwoBitMyReg.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 5125
#      INV                         : 1
#      LUT2                        : 2
#      LUT3                        : 16
#      LUT5                        : 2370
#      LUT6                        : 2479
#      MUXF7                       : 257
# FlipFlops/Latches                : 2304
#      FDRE                        : 2304
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 78
#      IBUF                        : 45
#      OBUFT                       : 33

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:            2304  out of  18224    12%
 Number of Slice LUTs:                 4868  out of   9112    53%
    Number used as Logic:              4868  out of   9112    53%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   4868
   Number with an unused Flip Flop:    2564  out of   4868    52%
   Number with an unused LUT:             0  out of   4868     0%
```

```
   Number of fully used LUT-FF pairs:  2304  out of   4868    47%
   Number of unique control sets:       128

IO Utilization:
 Number of IOs:                          79
 Number of bonded IOBs:                  79  out of    232    34%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 2304  |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.296ns (Maximum Frequency: 435.635MHz)
   Minimum input arrival time before clock: 9.590ns
   Maximum output required time after clock: 7.851ns
   Maximum combinational path delay: 13.725ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=================================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.296ns (frequency: 435.635MHz)
  Total number of paths / destination ports: 4863 / 2304
-------------------------------------------------------------------------
Delay:               2.296ns (Levels of Logic = 2)
  Source:            generate_block_identifier_1[0].RegisterBank/fourth_reg/serial_out (FF)
  Destination:       generate_block_identifier_1[0].RegisterBank/third_reg/qdata_7 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

```
  Data Path: generate_block_identifier_1[0].RegisterBank/fourth_reg/serial_out to
generate_block_identifier_1[0].RegisterBank/third_reg/qdata_7
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             2   0.447   0.721
generate_block_identifier_1[0].RegisterBank/fourth_reg/serial_out
(generate_block_identifier_1[0].RegisterBank/fourth_reg/serial_out)
     LUT6:I4->O            2   0.203   0.617
generate_block_identifier_1[0].RegisterBank/temp_serial_in<2>1
(generate_block_identifier_1[0].RegisterBank/temp_serial_in<2>)
     LUT5:I4->O            1   0.205   0.000
generate_block_identifier_1[0].RegisterBank/third_reg/Mmux_qdata[7]_pdata[7]_mux_3_OUT11
(generate_block_identifier_1[0].RegisterBank/third_reg/qdata[7]_pdata[7]_mux_3_OUT<0>)
     FDRE:D                    0.102
generate_block_identifier_1[0].RegisterBank/third_reg/qdata_0
    ----------------------------------------
    Total                      2.296ns (0.957ns logic, 1.339ns route)
                                       (41.7% logic, 58.3% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 123732 / 6912
--------------------------------------------------------------------------
Offset:              9.590ns (Levels of Logic = 4)
  Source:            reg_select<2> (PAD)
  Destination:       generate_block_identifier_1[4].RegisterBank/first_reg/serial_out (FF)
  Destination Clock: clk rising

  Data Path: reg_select<2> to
generate_block_identifier_1[4].RegisterBank/first_reg/serial_out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           140   1.222   2.211  reg_select_2_IBUF (reg_select_2_IBUF)
     LUT3:I0->O          262   0.205   2.412  _n0117<5>21 (_n0117<5>2)
     LUT5:I0->O           44   0.203   1.463  Mmux_load_all591 (load_all<62>)
     LUT5:I4->O           36   0.205   1.348
generate_block_identifier_1[62].RegisterBank/first_reg/_n0020_inv11
(generate_block_identifier_1[62].RegisterBank/first_reg/_n0020_inv1)
     FDRE:CE                   0.322
generate_block_identifier_1[62].RegisterBank/first_reg/serial_out
    ----------------------------------------
    Total                      9.590ns (2.157ns logic, 7.433ns route)
                                       (22.5% logic, 77.5% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 2176 / 33
--------------------------------------------------------------------------
Offset:              7.851ns (Levels of Logic = 5)
  Source:            generate_block_identifier_1[26].RegisterBank/fourth_reg/serial_out (FF)
  Destination:       serial_out (PAD)
  Source Clock:      clk rising

  Data Path: generate_block_identifier_1[26].RegisterBank/fourth_reg/serial_out to
serial_out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```

```
     FDRE:C->Q             2   0.447   0.961
generate_block_identifier_1[26].RegisterBank/fourth_reg/serial_out
(generate_block_identifier_1[26].RegisterBank/fourth_reg/serial_out)
     LUT6:I1->O            1   0.203   0.827
generate_block_identifier_1[26].RegisterBank/serial_out1 (serial_out_all<26>)
     LUT6:I2->O            1   0.203   0.827  Mmux_serial_out_reg_122
(Mmux_serial_out_reg_122)
     LUT6:I2->O            1   0.203   0.827  Mmux_serial_out_reg_7 (Mmux_serial_out_reg_7)
     LUT6:I2->O            1   0.203   0.579  reg_select<5>341 (serial_out_reg)
     OBUFT:I->O                2.571          serial_out_OBUFT (serial_out)
    ----------------------------------------
    Total                      7.851ns (3.830ns logic, 4.021ns route)
                                       (48.8% logic, 51.2% route)

==========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 2316 / 33
--------------------------------------------------------------------------
Delay:               13.725ns (Levels of Logic = 8)
  Source:            reg_select<2> (PAD)
  Destination:       serial_out (PAD)

  Data Path: reg_select<2> to serial_out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           140   1.222   2.211  reg_select_2_IBUF (reg_select_2_IBUF)
     LUT3:I0->O          264   0.205   2.412  _n0149<5>11 (_n0149<5>1)
     LUT5:I0->O            4   0.203   1.048  Mmux_shift_left_all241 (shift_left_all<30>)
     LUT6:I0->O            1   0.203   0.827
generate_block_identifier_1[30].RegisterBank/serial_out1 (serial_out_all<30>)
     LUT6:I2->O            1   0.203   0.808  Mmux_serial_out_reg_13
(Mmux_serial_out_reg_13)
     LUT6:I3->O            1   0.205   0.827  Mmux_serial_out_reg_7 (Mmux_serial_out_reg_7)
     LUT6:I2->O            1   0.203   0.579  reg_select<5>341 (serial_out_reg)
     OBUFT:I->O                2.571          serial_out_OBUFT (serial_out)
    ----------------------------------------
    Total                     13.725ns (5.015ns logic, 8.710ns route)
                                       (36.5% logic, 63.5% route)

==========================================================================

Cross Clock Domains Report:
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Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.296|         |         |         |
---------------+---------+---------+---------+---------+

==========================================================================


Total REAL time to Xst completion: 40.00 secs
Total CPU time to Xst completion: 40.28 secs

-->
```

```
Total memory usage is 4558628 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```