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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.54 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.54 secs

--> Reading design: Binary_Divisibility_By_7.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "Binary_Divisibility_By_7.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Binary_Divisibility_By_7"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : Binary_Divisibility_By_7
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
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Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

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=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q4\Q4_1.
v" into library work
Parsing module <Binary_Divisibility_By_7>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <Binary_Divisibility_By_7>.

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*                           HDL Synthesis                               *
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```
Synthesizing Unit <Binary_Divisibility_By_7>.
    Related source file is
"C:\Users\Alireza\Desktop\Programming\Verilog-Digital-System-Design\HWs\Hw3_9816603\Q4\Q4_1.
v".
    Found 1-bit register for signal <Divisible>.
    Found 3-bit register for signal <Remainder>.
    Found 5-bit adder for signal <n0017> created at line 41.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred   4 D-type flip-flop(s).
Unit <Binary_Divisibility_By_7> synthesized.

Synthesizing Unit <mod_5u_3u>.
    Related source file is "".
    Found 8-bit adder for signal <GND_2_o_b[2]_add_1_OUT> created at line 0.
    Found 7-bit adder for signal <GND_2_o_b[2]_add_3_OUT> created at line 0.
    Found 6-bit adder for signal <GND_2_o_b[2]_add_5_OUT> created at line 0.
    Found 5-bit adder for signal <a[4]_b[2]_add_7_OUT> created at line 0.
    Found 5-bit adder for signal <a[4]_GND_2_o_add_9_OUT> created at line 0.
    Found 5-bit adder for signal <a[4]_GND_2_o_add_11_OUT> created at line 0.
    Found 8-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 7-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 5-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 5-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 5-bit comparator lessequal for signal <BUS_0006> created at line 0
    Summary:
        inferred   6 Adder/Subtractor(s).
        inferred   6 Comparator(s).
        inferred  26 Multiplexer(s).
Unit <mod_5u_3u> synthesized.

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HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 7
 5-bit adder                                          : 4
 6-bit adder                                          : 1
 7-bit adder                                          : 1
 8-bit adder                                          : 1
# Registers                                            : 2
 1-bit register                                       : 1
 3-bit register                                       : 1
# Comparators                                          : 6
 5-bit comparator lessequal                           : 3
 6-bit comparator lessequal                           : 1
 7-bit comparator lessequal                           : 1
 8-bit comparator lessequal                           : 1
# Multiplexers                                         : 26
 1-bit 2-to-1 multiplexer                             : 25
 3-bit 2-to-1 multiplexer                             : 1

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=========================================================================
*                      Advanced HDL Synthesis                           *
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Advanced HDL Synthesis Report

Macro Statistics
Adders/Subtractors : 7
 3-bit adder : 1
 5-bit adder : 6
Registers : 4
 Flip-Flops : 4
Comparators : 6
 5-bit comparator lessequal : 3
 6-bit comparator lessequal : 1
 7-bit comparator lessequal : 1
 8-bit comparator lessequal : 1
Multiplexers : 26
 1-bit 2-to-1 multiplexer : 25
 3-bit 2-to-1 multiplexer : 1

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* Low Level Synthesis *
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Optimizing unit <Binary_Divisibility_By_7> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Binary_Divisibility_By_7, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Macro Statistics
Registers : 4
 Flip-Flops : 4

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* Partition Report *
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Partition Implementation Status

  No Partitions were found in this design.

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* Design Summary *
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Top Level Output File Name : Binary_Divisibility_By_7.ngc

Primitive and Black Box Usage:

BELS : 4

```
#      LUT4                          : 3
#      LUT5                          : 1
# FlipFlops/Latches                  : 4
#      FD                            : 1
#      FDR                           : 3
# Clock Buffers                      : 1
#      BUFGP                         : 1
# IO Buffers                         : 6
#      IBUF                          : 2
#      OBUF                          : 4

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              4  out of  18224     0%
 Number of Slice LUTs:                   4  out of   9112     0%
    Number used as Logic:                4  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     8
   Number with an unused Flip Flop:      4  out of      8    50%
   Number with an unused LUT:            4  out of      8    50%
   Number of fully used LUT-FF pairs:    0  out of      8     0%
   Number of unique control sets:        2

IO Utilization:
 Number of IOs:                          7
 Number of bonded IOBs:                  7  out of    232     3%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%

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Partition Resource Summary:
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  No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
Clock                              | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
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---------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.714ns (Maximum Frequency: 583.431MHz)
   Minimum input arrival time before clock: 2.555ns
   Maximum output required time after clock: 3.732ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'Clock'
  Clock period: 1.714ns (frequency: 583.431MHz)
  Total number of paths / destination ports: 12 / 4
-------------------------------------------------------------------------
Delay:               1.714ns (Levels of Logic = 1)
  Source:            temp_remainder_0 (FF)
  Destination:       temp_remainder_1 (FF)
  Source Clock:      Clock rising
  Destination Clock: Clock rising

  Data Path: temp_remainder_0 to temp_remainder_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.962  temp_remainder_0 (temp_remainder_0)
     LUT4:I0->O            1   0.203   0.000  BUS_0001_PWR_1_o_mod_3/Mmux_o21
(BUS_0001_PWR_1_o_mod_3_OUT<1>)
     FDR:D                 0.102          temp_remainder_1
    ----------------------------------------
    Total                      1.714ns (0.752ns logic, 0.962ns route)
                                       (43.9% logic, 56.1% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clock'
  Total number of paths / destination ports: 8 / 7
-------------------------------------------------------------------------
Offset:              2.555ns (Levels of Logic = 2)
  Source:            String (PAD)
  Destination:       temp_divisible (FF)
  Destination Clock: Clock rising

  Data Path: String to temp_divisible
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   1.222   1.028  String_IBUF
(BUS_0001_PWR_1_o_mod_3/Madd_a[4]_GND_2_o_add_11_OUT_Madd_cy<0>)
     LUT5:I0->O            1   0.203   0.000  temp_divisible_glue_set
(temp_divisible_glue_set)
     FD:D                  0.102          temp_divisible
    ----------------------------------------
    Total                      2.555ns (1.527ns logic, 1.028ns route)
                                       (59.8% logic, 40.2% route)
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==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clock'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              3.732ns (Levels of Logic = 1)
  Source:            temp_remainder_2 (FF)
  Destination:       Remainder<2> (PAD)
  Source Clock:      Clock rising

  Data Path: temp_remainder_2 to Remainder<2>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.714  temp_remainder_2 (temp_remainder_2)
     OBUF:I->O                 2.571          Remainder_2_OBUF (Remainder<2>)
    ----------------------------------------
    Total                      3.732ns (3.018ns logic, 0.714ns route)
                                       (80.9% logic, 19.1% route)

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Cross Clock Domains Report:
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Clock to Setup on destination clock Clock
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clock          |    1.714|         |         |         |
---------------+---------+---------+---------+---------+

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Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.91 secs

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Total memory usage is 4487500 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```