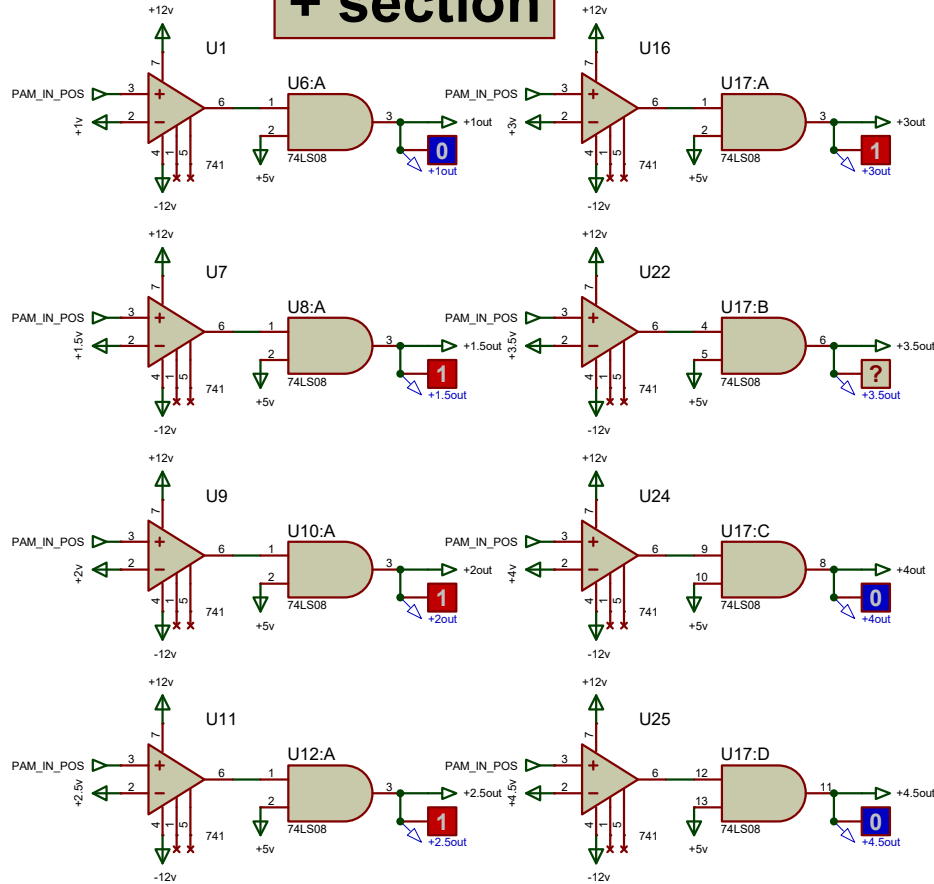


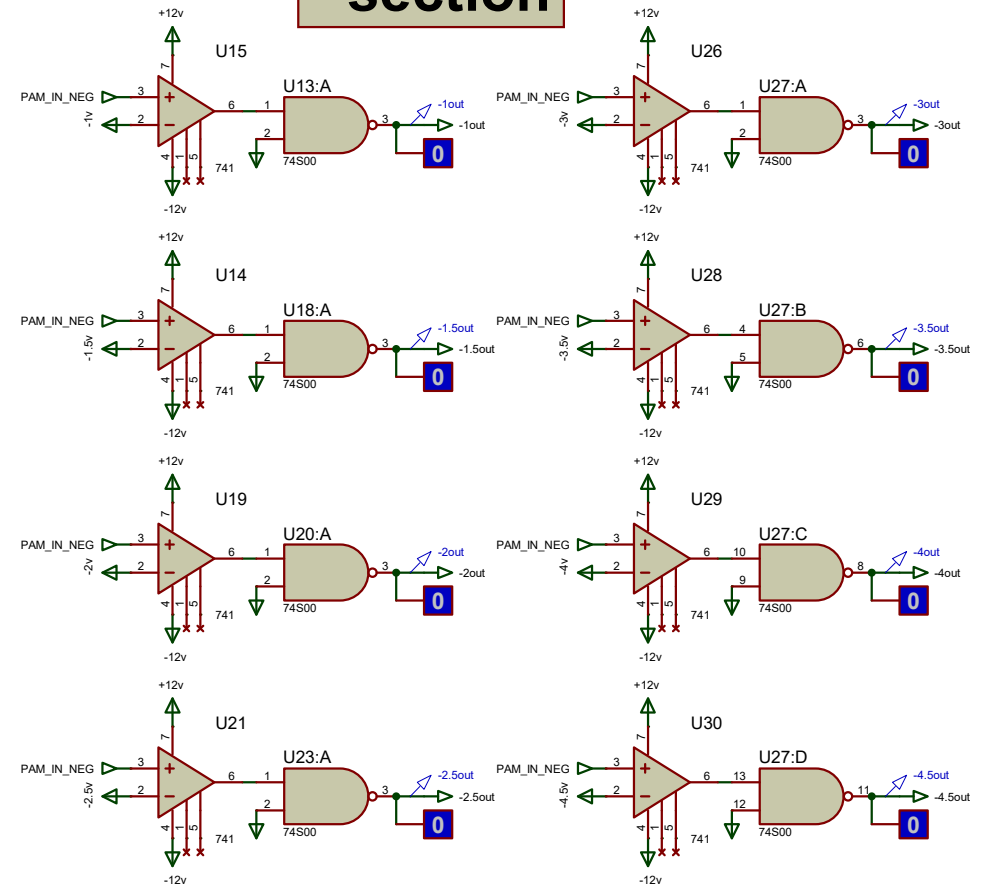
child sheet logical voltage comparator sub circuit 2

desined by Alireza Sotoodeh

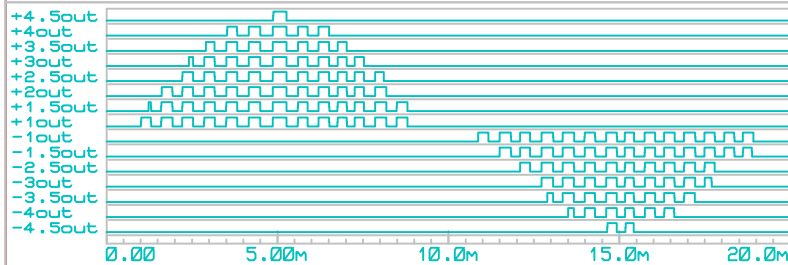
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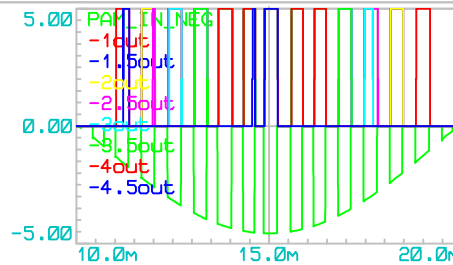
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DIGITAL ANALYSIS



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