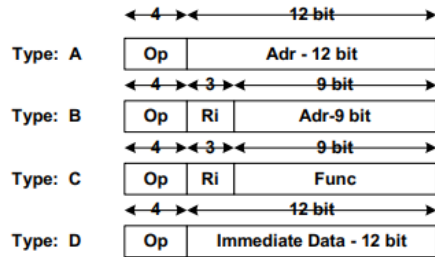


Multi-cycle Mips processor

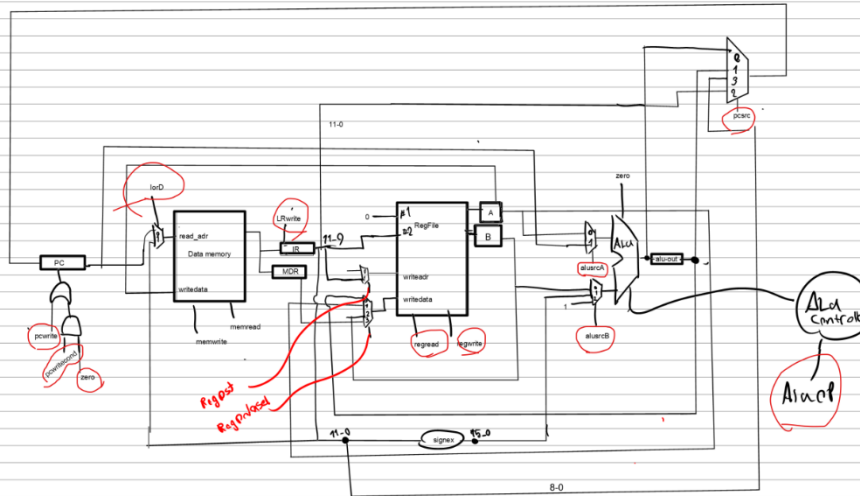
Instructions:



Mnemonic		Description	Opcode	Function	Type
Load	adr-12	$R0 \leftarrow M[\text{adr-12}]$	0000	-	A
Store	adr-12	$M[\text{adr-12}] \leftarrow R0$	0001	-	A
Jump	adr-12	$PC \leftarrow \text{adr-12}$	0010	-	A
BranchZ	Ri, adr-9	If ($R0=Ri$) $PC[8:0] \leftarrow \text{adr-9}$	0100	-	B
MoveTo	Ri	$Ri \leftarrow R0$	1000	000000001	C
MoveFrom	Ri	$R0 \leftarrow Ri$	1000	000000010	C
Add	Ri	$R0 \leftarrow R0 + Ri$	1000	000000100	C
Sub	Ri	$R0 \leftarrow R0 - Ri$	1000	000001000	C
And	Ri	$R0 \leftarrow R0 \text{ AND } Ri$	1000	000010000	C
Or	Ri	$R0 \leftarrow R0 \text{ OR } Ri$	1000	000100000	C
Not	Ri	$R0 \leftarrow \text{NOT } Ri$	1000	001000000	C
Nop	-	No Operation	1000	010000000	C
Addi	Imm-12	$R0 \leftarrow R0 + \text{Imm-12}$	1100	-	D
Subi	Imm-12	$R0 \leftarrow R0 - \text{Imm-12}$	1101	-	D
Andi	Imm-12	$R0 \leftarrow R0 \text{ AND Imm-12}$	1110	-	D
Ori	Imm-12	$R0 \leftarrow R0 \text{ OR Imm-12}$	1111	-	D

Datapath Schematic:

DataPath

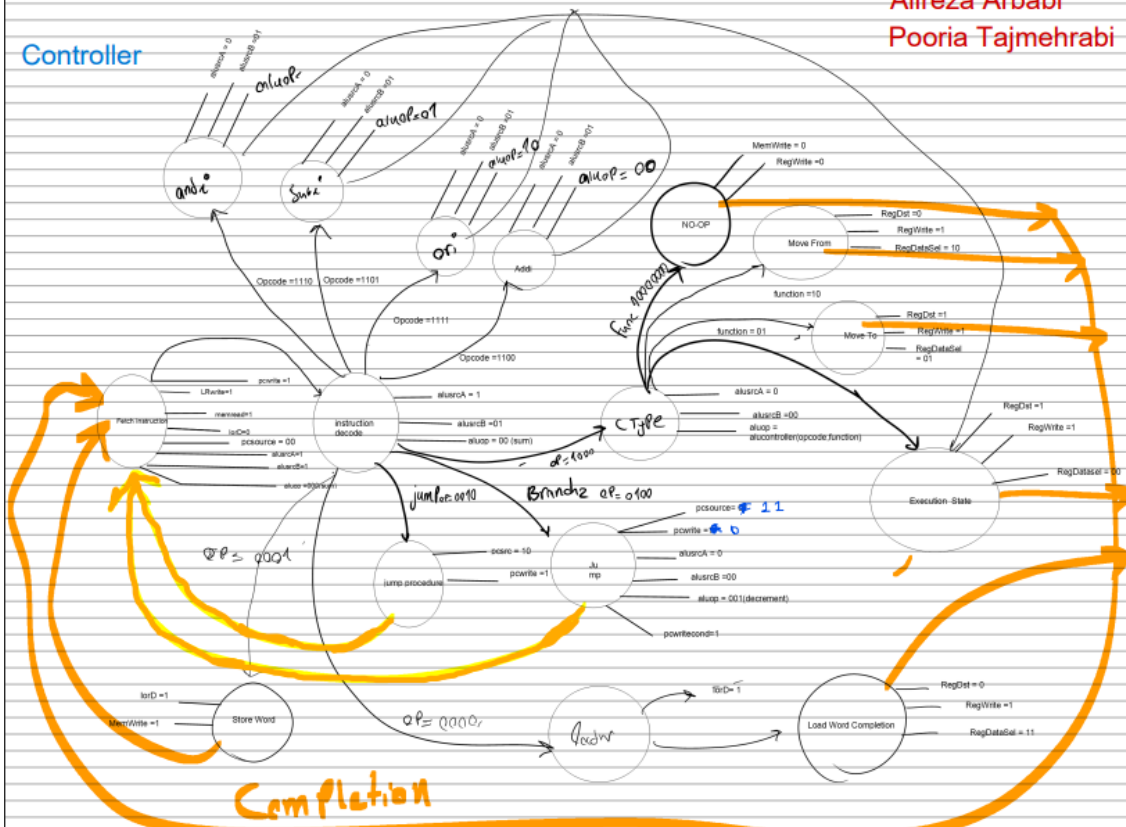


Controller state machine:

Midterm#2

Controller

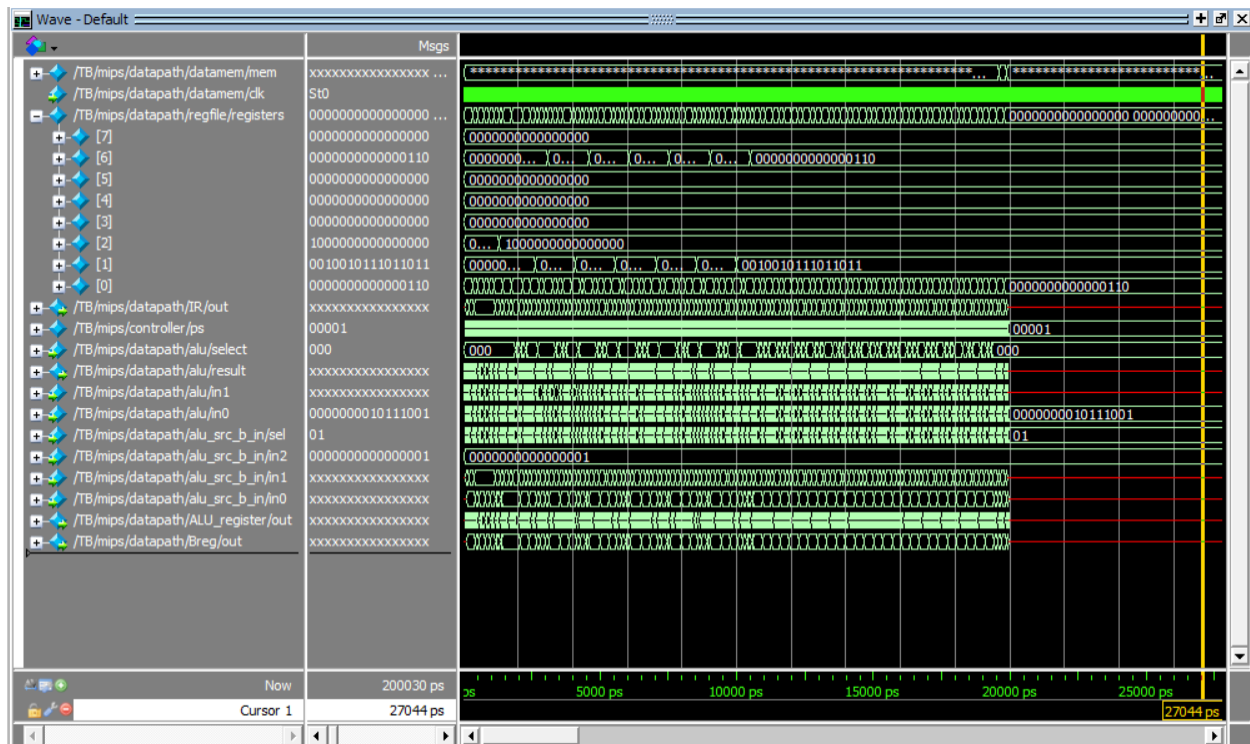
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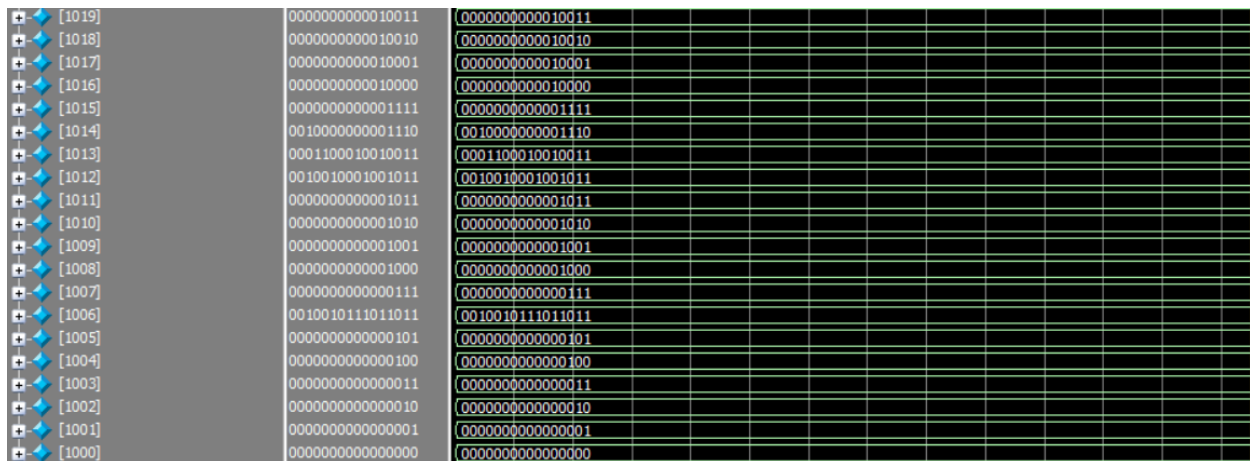
Test Bench description:

Instructions are stored in the first 200 cells of memory, test numbers are stored in cells 1000 to 1019, The processor read 20 numbers and store the value and index of the Maximum number in cell 2000 and 2001.

Processor Waveform:



Output waves:



Value and index of Maximum element:

[illegible]