Instruction/signal	Jsel0	Jlselr	Jsel	jrsel	Alusrc	RegDst	RegWrite	MemRead	MemWrite	PCsrc	MemtoReg	ALUop
Add	0	0	0	-	0	1	1	-	-	0	0	000
Addi	0	0	0	-	1	0	1	-	-	0	0	000
Sub	0	0	0	-	0	1	1	-	-	0	0	001
Slt	0	0	0	-	0	1	1	-	-	0	0	100
Slti	0	0	0	-	1	0	1	-	-	0	0	100
and	0	0	0	-	0	1	1	-	-	0	0	010
Or	0	0	0	-	0	1	1	-	-	0	0	011
Load Word	0	0	0	-	1	0	1	1	0	0	1	000
Store Word	0	0	0	-	1	0	0	0	1	0	-	000
Jump	-	-	1	0	-	-	-	-	-	-	-	-
Jump & link	-	1	1	0	-	-	-	-	-	-	-	-
Jump Register	-	-	1	1	-	-	-	-	-	-	-	-
Branch equal	0	0	0	-	0	-	0	-	-	is_zero	-	001

0 : signal 0
1 : signal 1
- : Don’t care