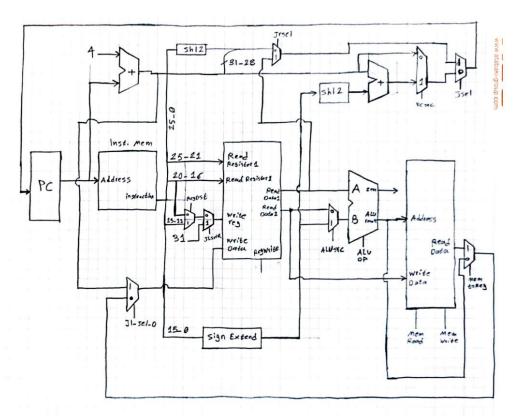
Single-cycle Mips Processor

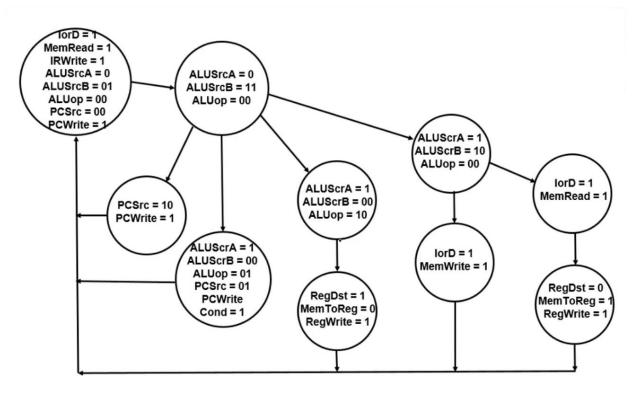
Instructions Format:

| ALU Carge Alu | | | | | | | | | | | | | | |
|--|-------------------|--|--------------------|-------|----|-------|----|-------|--------|------|-----|-----|----|--|
| Multipage Mult | Instruction Type | Example | Instruction Coding | | | | | | | | | | | |
| Manual M | | ALU Usage | | | | | | | | | | | | |
| Non-Jump R-Type | Non-Jump R-Type | add rd, rs, rt | | 31 26 | 15 | 21 20 | | 16 15 | | 1 10 | | 6.5 | | |
| Manual M | | | | ор | rs | | rt | | rd | | sa | | fn | |
| Manie Mani | | The ALU performs the operation indicated by the mnemonic, which is coded into the fit field. | | | | | | | | | | | | |
| Manual Language | Immediate | addi rt, rs, imm | I | 31 26 | 15 | 21 20 | | 16 15 | | | | | | |
| Para | | | | op | rs | | rt | | | | imm | | | |
| Register | | The ALU performs the operation indicated by the minemonic, which is coded into the op field. | | | | | | | | | | | | |
| Final Fina | Branch | beq Srs, Srt, imm | | 31 26 | 25 | 21 20 | | 16 15 | | | | | | |
| Load Load | | | I | op | rs | | rt | | | | imm | | | |
| Lead wrt, mm(s) | | The ALU subtracts rt from rs for comparison. | | | | | | | | | | | | |
| Load The ALU adds rs and immediate address. Store The ALU adds rs and immediate address. The ALU adds rs and immediate a | Load | lw rt, imm(rs) | | 31 26 | 16 | 21 20 | | 16 15 | | | | | | |
| Store Nort, mm(r) T | | | | op | rs | | rt | | | | imm | | | |
| Norn-Register Jump Face | | The ALU adds rs and imm to get the address. | | | | | | | | | | | | |
| Stoce Text | Store | sw rt, imm(rs) | | 31 26 | 25 | 21 20 | | 16 15 | | | | | | |
| Non-Register Jump Jal target Jal target | | | | ор | rs | | rt | | | | imm | | | |
| Non-Register Jump Register 2 J op State 120 State 1 St | | The ALU adds rs and imm to get the address. | | | | | | | | | | | | |
| The ALU is not used. | Non-Register Jump | jal target | | 31 26 | 16 | | | | | | | | | |
| Jump Register jair rd, rs R 31 26 25 21 20 16 16 11 10 6 6 | | | ı | ор | | | | | target | | | | | |
| Jump Register Jahr rd, rs R op rs rt rd sd sa fin | | The ALU is not used. | | | | | | | | | | | | |
| Jump Register op rs rt r0 sa In | Jump Register | jalr rd, rs | | 31 26 | 26 | 21 20 | | 16 15 | 1 | 1 10 | | 6 5 | | |
| The ALLI is not used | | | | ор | rs | | rt | | rd | | sa | | fn | |
| *************************************** | | | | | | | | | | | | | | |

Datapath Schematic:



Controller state machine:



Controller Signal Guides:

| Instruction/signal | Jsel0 | Jiselr | Jsel | jrsel | Alusrc | RegDst | RegWrite | MemRead | MemWrite | PCsrc | MemtoReg | ALUop |
|--------------------|-------|--------|------|-------|--------|--------|----------|---------|----------|---------|----------|-------|
| Add | 0 | 0 | 0 | - | 0 | 1 | 1 | - | - | 0 | 0 | 000 |
| Addi | 0 | 0 | 0 | - | 1 | 0 | 1 | - | - | 0 | 0 | 000 |
| Sub | 0 | 0 | 0 | - | 0 | 1 | 1 | - | - | 0 | 0 | 001 |
| SIt | 0 | 0 | 0 | - | 0 | 1 | 1 | - | - | 0 | 0 | 100 |
| Slti | 0 | 0 | 0 | - | 1 | 0 | 1 | - | - | 0 | 0 | 100 |
| and | 0 | 0 | 0 | - | 0 | 1 | 1 | - | - | 0 | 0 | 010 |
| Or | 0 | 0 | 0 | - | 0 | 1 | 1 | - | - | 0 | 0 | 011 |
| Load Word | 0 | 0 | 0 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 000 |
| Store Word | 0 | 0 | 0 | - | 1 | 0 | 0 | 0 | 1 | 0 | - | 000 |
| Jump | - | - | 1 | 0 | - | - | - | - | - | - | - | - |
| Jump & link | - | 1 | 1 | 0 | - | - | - | - | - | - | - | - |
| Jump Register | - | - | 1 | 1 | - | - | - | - | - | - | - | - |
| Branch equal | 0 | 0 | 0 | - | 0 | - | 0 | - | - | is_zero | - | 001 |

0: signal 0 1: signal 1 -: Don't care