Alish Kanani

Pre-final Year (B.Tech)
Electrical Engineering
Indian Institute of Technology (IIT) Jodhpur

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Education

B.Tech - Electrical Engineering
IIT Jodhpur
Expected 2021
CGPA : 8.75/10 (Till 5th Semester)

Higher Secondary (HSC)
Ashadeep Science Bhavan
2017 | Surat, Gujrat
Percentage: 94.4%

Secondary (SSC)
M N J Patel High School
2015 | Surat, Gujrat
Percentage: 87.66%

Relevant Courses

Electrical Core
Digital Logic and Design
Microprocessors and Microcontrollers
Analog Electronics
Signal and Power Integrity*
Power Electronics
Circuit Theory
Communication Systems
Signals and Systems
Electrical Machine
Power System
Physics of Semiconductor Device
Digital Signal Processing*
Control Systems*
(* Ongoing courses)

Fundamental Mathematics
Real Analysis and Linear Algebra
Complex Analysis and Differential Equations
Probability and Statistics

Skills

Language
C
Python (Basic)
MATLAB
Perl(Basic)

HDL
Verilog

Software
Xilinx (ISE)
Synopsys DC
Cadence Virtuoso(Basic)
Simulink
Iverilog
Arduino

Internship

Accuracy Configurable Arithmetic Circuit | IIT Ropar
Research Intern | May 2019 - July 2019 | Guide: Dr Neeraj Goel
- Studied various existing approximate binary adders and multipliers
- Proposed **An Accuracy Configurable Adder** and helped in **An Accuracy-Configurable Rounding-Based Multiplier**
- Compared proposed algorithms with state of the art algorithms in Synopsys Design Compiler and in octave.

Projects

DHVANIK - Wearable Tympanometric Diagnostic Tool for Middle Ear Ailments
Inter IIT Project | Sep 2019 - Dec 2019 | Guide: Dr Arpit Khandelwal
- Developed a low-cost, user-friendly, IoT enabled, head-phone sized tympanometer that detects middle ear problem
- Made business model for IICDC 2019 and Inter IIT 2019

Optimisation of 32 bit adders
B.Tech Project | Jan 2019 - Apr 2019 | Guide: Dr S. P. Tiwari
- Studied six different algorithms to add two binary numbers
- Compared delay, area and power of these algorithms in **Xilinx-ise**
- Project report and code: github.com/AlishKanani/32bitAdders/

AES Data Encryption on FPGA
Gymkhana Project | Sep 2018 - May 2019
- The aim of the project was to develop an FPGA based encryption engine to facilitate massive data encryption and decryption.
- Project link: github.com/AlishKanani/AES/

NETRA- Indoor Navigator for Visually Impaired
Texas Instruments IICDC Competition | Aug 2018 - May 2019
- Applied dead reckoning for indoor navigation without expensive infrastructure.
- Implemented on **Beaglebone black** using 9 axis **IMU**
- Audio and haptic feedback for navigation especially for the visually impaired

Positions of Responsibility

CAPTAIN Electronics Club | Aug 2018 - May 2019
- Coordinated and managed year round activities and finance of the Electronics Club at IIT Jodhpur

STUDENT GUIDE Counselling Service | Aug 2018 - May 2019
- Mentored freshmen students as a Student Guide for their smooth transitioning into college/hostel life.

Achievements

- Accepted oral presentation on Approximate Multiplication at Research Conclave, IIT Guwahati.
- Presented a poster on DHVANIK at Industry Day, IIT Jodhpur.
- Secured **Bronze** medal in Inter IIT Techmeet 2019
- Led the team of project NETRA and DHVANIK which reached the **semi-finals** of **DST** and **Texas Instruments** IICDC 2018 and 2019.
- Won First Place in the Analog Designs - an online contest by **Texas Instruments University Program.**
- Placed among the top **0.5% of 1.4 million** applicants in JEE Advanced 2017