# Alish Kanani

Pre-final Year (B.Tech)
Electrical Engineering
Indian Institute of Technology (IIT) Jodhpur

Mob. : +91 9664515665 Email. : kanani.1@iitj.ac.in Website : aliskanani.github.io

Github: github.com/AlishKanani

LinkedIn: www.linkedin.com/in/alishkanani

### Education

B.TECH. IN ELECTRICAL ENGINEERING

IIT Jodhpur EXPECTED 2021

CGPA: 8.73/10 (Till 4th Semester)

HIGHER SECONDARY (HSC) Ashadeep Science Bhavan 2017 | Surat, Gujrat

Percentage: 94.4%

SECONDARY (SSC) M N J Patel High School 2015 | Surat, Gujrat Percentage: 87.66%

**Relevant Courses** 

### **ELECTRICAL CORE**

Digital Logic and Design
Microprocessors and Microcontrollers\*
Analog Electronics\*
Circuit Theory
Communication Systems\*
Signals and Systems
(\* Ongoing courses)

### **FUNDAMENTAL MATHEMATICS**

Real Analysis and Linear Algebra Complex Analysis and Differential Equations Probability and Statistics

### Skills

### **LANGUAGE**

C

Python (Basic) MATLAB

**HDL** 

Verilog

### **SOFTWARE**

Xilinx (ISE)

Synopsys DC (Basic)

Simulink

Octave

Arduino

Energia

Photoshop (Basic)

## Internship

### Accuracy Configurable Arithmetic Circuit | IIT Ropar

Research Intern | May 2019 - July 2019 | Guide: Dr Neeraj Goel

- Studied various existing approximate binary adders and multipliers
- Proposed An Accuracy Configurable Adder and helped in An Accuracy-Configurable Rounding-Based Multiplier
- Submitted two papers in The IEEE International Symposium on Circuits and Systems (ISCAS), 2020

### **Projects**

### **Optimisation of 32 bit adders**

B.Tech Project | Jan 2019 - Apr 2019 | Guide: Dr Shree Prakash Tiwari

- Studied six different algorithms to add two binary numbers
- Compared delay, area and power of these algorithms in Xilinx-ise
- Project report and code: github.com/AlishKanani/32bitAdders/

### **AES Data Encryption on FPGA**

Gymkhana Project | Sep 2018 - May 2019

- The aim of the project was to develop an FPGA based encryption engine to facilitate massive data encryption and decryption.
- Project link: github.com/AlishKanani/AES/

### **NETRA- Indoor Navigator for Visually Impaired**

Texas Instruments IICDC Competition | Aug 2018 - May 2019

- Applied dead reckoning for indoor navigation without expensive infrastructure.
- Implemented on Beaglebone black using 9 axis IMU
- Audio and haptic feedback for navigation especially for the visually impaired

# Positions of Responsibility

### CAPTAIN Electronics Club | Aug 2018 - May 2019

 Coordinated and managed year round activities and finance of the Electronics Club at IIT Jodhpur

### STUDENT GUIDE Counselling Service | Aug 2018 - May 2019

• Mentored freshmen students as a Student Guide for their smooth transitioning into college/hostel life.

### **Achievements**

- Led the team of project NETRA and reached semi-finals of DST and Texas Instruments India Innovation Challenge Design Contest 2018 among 10,146 teams comprising of 26511 students from 1760 colleges
- Won First Place in the Analog Designs an online contest by **Texas Instruments University Program.**
- Placed among the top 0.5% of 1.4 million applicants in JEE Advanced 2017