Alish Kanani

Final Year (B.Tech)
Electrical Engineering
IIT Jodhpur

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Education

B.Tech - Electrical Engineering
IIT Jodhpur
Expected 2021
CGPA:8.9/10 (Till 6th Semester)

Higher Secondary (HSC)
Ashadeep Science Bhavan
2017 | Surat, Gujrat
Percentage: 94.4%

Secondary (SSC)
M N J Patel High School
2015 | Surat, Gujrat
Percentage: 87.66%

Relevant Courses

Electrical Core
Digital Logic and Design
Microprocessors & controllers
Analog Electronics
Signal and Power Integrity
Memory Architecture
Power Electronics
Circuit Theory
Communication Systems
Signals and Systems
Electrical Machine
Power System
Physics of Semiconductor Device
Digital Signal Processing
Control Systems

Fundamental Mathematics
Real Analysis and Linear Algebra
Complex Analysis and Differential Equations
Probability and Statistics

Skills

Languages
C
Python (Basic)
MATLAB
Perl(Basic)

HDL
Verilog
HLS

Softwares
Vitis AI
ABC Synthesis Tool
Vitis (Basic)
Synopsys DC
Cadence Virtuoso(Basic)
Simulink

Others
Deep Neural Network(Basic)
LaTex
Arduino

Publications

- Alish Kanani, Jigar Mehta, Neeraj Goel "**ACA-CSU: A Carry Selection Based Accuracy Configurable Approximate Adder Design** ", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020, pp. 434-439. **Paper**
- Rajat Bhattacharjya, Alish Kanani, Neeraj Goel "**ReARM: A Reconfigurable Approximate Rounding-Based Multiplier for Image Processing** ", VLSI Design and Test 24rd International Symposium (VDAT), Bhubaneswar, India, 2020.

Internships

FPGA Implementation of CRAFT Algorithm | TCS Research & Innovation
Research Intern | May 2020 - Aug 2020
- Suggested implementation methods to speedup CRAFT text detection network on Alveo FPGA.
- Learned **Vitis AI** and **HLS** for different kind of speedup technique.

Approximate 8bit Parallel Prefix Adder | TU Wien
Research Intern | May 2020-July 2020 | Guide:Prof. Muhammad Shafique
- Proposed **1.4 Million** approximate adders from 4 different Prefix tree.
- Automated process to extract performance and error matrix for each configuration using **ABC synthesis tool** and **python** .

Accuracy Configurable Arithmetic Circuit | IIT Ropar
Research Intern | May 2019 - July 2019 | Guide: Dr Neeraj Goel
- Proposed Accuracy Configurable Adder and Multiplier
- Compared proposed algorithms with state of the art algorithms using **Synopsys Design Compiler** and **octave** .

Projects

DHVANIK - Wearable Tympanometric Diagnostic Tool for Middle Ear Ailments
Inter IIT Project | Sep 2019 - Dec 2019 | Guide: Dr Arpit Khandelwal
- Developed a low-cost, user-friendly, IoT enabled, head-phone sized **tympanometer** that detects middle ear problem.
- Made business model for IICDC 2019 and Inter IIT 2019.

Optimisation of 32 bit adders | Code and Project Report
B.Tech Project | Jan 2019 - Apr 2019 | Guide: Dr S. P. Tiwari
- Studied six different algorithms to add two binary numbers
- Compared delay, area and power of these algorithms in **Xilinx-ise**

AES Data Encryption on FPGA | Code
Gymkhana Project | Sep 2018 - May 2019
- developed an FPGA based encryption-decryption engine to facilitate speed up AES encryption.

NETRA- Indoor Navigator for Visually Impaired
Texas Instruments IICDC Competition | Aug 2018 - May 2019
- Applied dead reckoning for indoor navigation and implemented on **Beaglebone black** using 9 axis **IMU**
- Audio and haptic feedback for navigation for the visually impaired.

Positions of Responsibility

Captain | Electronics Club | Aug 2018 - May 2019
Student Guide | Counselling Service | Aug 2018 - May 2019

Achievements

- Presented a poster of DHVANIK on Industry Day, IIT Jodhpur.
- Secured **Bronze** medal in Inter IIT Techmeet 2019.
- Led the team of project NETRA and DHVANIK which reached the **semi-finals** of **DST** and **Texas Instruments** IICDC 2018 and 2019.
- Secured First Place in the Analog Designs - an online contest by **Texas Instruments University Program.**