# Alish Kanani

Pre-final Year (B.Tech)
Electrical Engineering
Indian Institute of Technology (IIT) Jodhpur

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## Education

B.TECH. IN ELECTRICAL ENGINEERING
IIT Jodhpur
*EXPECTED 2021*
CGPA : 8.73/10 (Till 4th Semester)

HIGHER SECONDARY (HSC)
Ashadeep Science Bhavan
*2017* | Surat, Gujrat
Percentage: 94.4%

SECONDARY (SSC)
M N J Patel High School
*2015* | Surat, Gujrat
Percentage: 87.66%

## Relevant Courses

**ELECTRICAL CORE**
Digital Logic and Design
Microprocessors and Microcontrollers*
Analog Electronics*
Circuit Theory
Communication Systems*
Signals and Systems
(* Ongoing courses)

**FUNDAMENTAL MATHEMATICS**
Real Analysis and Linear Algebra
Complex Analysis and Differential Equations
Probability and Statistics

## Skills

**LANGUAGE**
C
Python (Basic)
MATLAB

**HDL**
Verilog

**SOFTWARE**
Xilinx (ISE)
Synopsys DC (Basic)
Simulink
Octave
Arduino
Energia
Photoshop (Basic)

## Internship

**Accuracy Configurable Arithmetic Circuit | IIT Ropar**
Research Intern | May 2019 - July 2019 | Guide: Dr Neeraj Goel

- Studied various existing approximate binary adders and multipliers
- Proposed **A Control Unit Based Accuracy Configurable Adder for Error Tolerant Application** and helped in **ACRoM: An Accuracy-Configurable Rounding-Based Multiplier Design** (Under Review)
- Compared proposed circuits with state of the art circuits in Synopsys Design Compiler and in octave (1 million times) to calculate error matrix.
- Submitted two papers in The 33rd International Conference on VLSI Design and 19th International Conference on Embedded Systems

## Projects

**Optimisation of 32 bit adders**
B.Tech Project | Jan 2019 - Apr 2019 | Guide: Dr Shree Prakash Tiwari

- Studied six different algorithms to add two binary numbers
- Compared delay, area and power of these algorithms in Xilinx-ise
- Project report and code: github.com/AlishKanani/32bitAdders/

**AES Data Encryption on FPGA**
Gymkhana Project | Sep 2018 - May 2019

- The aim of the project was to develop an FPGA based encryption engine to facilitate massive data encryption and decryption.
- Project link: github.com/AlishKanani/AES/

**NETRA- Indoor Navigator for Visually Impaired**
Texas Instruments IICDC Competition | Aug 2018 - May 2019

- Worked on cost effective solution to assist visually impaired using dead reckoning and IMU.
- The project was selected for semi-finals of IICDC-2018

## Positions of Responsibility

**Captain**
Electronics CLUB | Aug 2018 - May 2019

- Coordinating and managing year round activities of the Electronics Club at IIT Jodhpur and working for technical development for the club members.

**Student Guide**
Counselling Service | Aug 2018 - May 2019

- Mentored 9 freshmen students as a Student Guide for their smooth transitioning into college/hostel life.

## Achievements

- Led the team of project 'NETRA - Indoor Navigation for Visually Impaired' and reached **semi-finals** of IICDC 2018 organised by **Texas Instruments** and **Department of Science and Technology (DST)**
- Won First Place in the Analog Designs - an online contest by Texas Instruments University Program.
- Placed among the top **0.5% of 1.4 million** applicants in JEE Advanced 2017