Alish Kanani

Final Year B.Tech, Electrical Engineering
Indian Institute of Technology Jodhpur
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Education

B.Tech - Electrical Engineering
IIT Jodhpur | *CGPA:8.86/10 (Till 7th Semester)* — *2017 – 2021*

Higher Secondary (HSC)
Ashadeep Science Bhavan | *Percentage: 94.4%* — *2015 – 17*

Secondary (SSC)
M N J Patel High School | *Percentage: 87.66%* — *2014 – 15*

Publications

- A. Kanani, J. Mehta and N. Goel, "ACA-CSU: A Carry Selection Based Accuracy Configurable Approximate Adder Design," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020. **Paper**
- R. Bhattacharjya, A. Kanani and N. Goel, "ReARM: A Reconfigurable Approximate Rounding-Based Multiplier for Image Processing," 24th International Symposium on VLSI Design and Test (VDAT), Bhubaneswar, India, 2020. **Paper**

Experience

FPGA Implementation of CRAFT Algorithm — May 2020 – Aug 2020
TCS Research & Innovation | *Research Intern*
- Suggested implementation methods to speedup CRAFT text detection network on Alveo FPGA.
- **3 to 100X** speedup achieved using different approaches.
- Learned **Vitis AI** and **HLS** for different kind of speedup technique.

Design Space Exploration of 8-bit Approximate Prefix Adders — May 2020 – July 2020
Vienna University of Technology (TU Wien) | *Research Intern* — *Prof. Muhammad Shafique*
- Proposed **1.4 Million** approximate adders from 4 different Prefix tree.
- Automated process to extract performance and error matrix for each configuration using **ABC synthesis tool** and **python**.
- Extracting all the **Pareto Optimal** adders using different performance and error matrix curve and assembling all the adders to make the library.

Accuracy Configurable Arithmetic Circuit — May 2019 – July 2019
IIT Ropar | *Research Intern* — *Dr Neeraj Goel*
- Studied various existing approximate binary adders and multipliers.
- Proposed **An Accuracy Configurable Adder** and helped in **An Accuracy-Configurable Rounding-Based Multiplier**.
- Compared proposed algorithms with state of the art algorithms using **Synopsys Design Compiler** and **octave**.

Projects

LightFPGA : Acceleration of LightGBM by FPGA Implementation — Sep 2020 – Nov 2020
B.Tech Project — *Guide:Dr Harshit Agarwal*
- Automated the **Verilog** generation of decision tree-based LightGBM for FPGA implementation.
- Made the **LightFPGA** library in Python which performs all the required steps for Verilog Generation and testing form extracted LightGBM classification model.
- On Alveo u280 FPGA, around **700 to 1000X** speedup achieved for different data-sets.

Improving DLS method for rain-interrupted limited over Cricket matches — Sep 2020 - Present
Self Project
- Cleaned the dataset of over 1900 ODI and 1700 T20 matches.
- Incorporating dynamics of Cricket into ML based regression model to get a realistic & fair value of revised target score.

DHVANIK - Wearable Tympanometric Diagnostic Tool for Middle Ear Ailments — Sep 2019 - Dec 2019
Inter IIT Tech Meet Competition — *Guide: Dr Arpit Khandelwal*
- Developed a low-cost, user-friendly, IoT enabled, head-phone sized **tympanometer** that detects middle ear problems.
- Made business model for IICDC 2019 and Inter IIT 2019.

Optimisation of 32 bit adders on FPGA Jan 2019 - Apr 2019

B.Tech Project *Guide: Dr S. P. Tiwari*

- Studied six different algorithms to add two binary numbers.
- Compared delay, area and power of these algorithms in **Xilinx-ise**.
- Project report and code: github.com/AlishKanani/32bitAdders/

AES Data Encryption on FPGA Sep 2018 - May 2019

Gymkhana Project

- Developed an FPGA based encryption-decryption engine to facilitate speed up in AES encryption.
- Project link: github.com/AlishKanani/AES

NETRA- Indoor Navigator for Visually Impaired Aug 2018 - May 2019

Texas Instruments IICDC Competition *Guide: Dr Arpit Khandelwal*

- Applied dead reckoning for indoor navigation without expensive infrastructure.
- Implemented on **Beaglebone black** using 9 axis **IMU**.
- Audio and haptic feedback for navigation especially for the visually impaired.

Technical Skills

Programming Languages: C • Python • MATLAB • Perl(Basic)
HDL: Verilog • HLS
Softwares: Vivado • Vitis AI • ABC Synthesis Tool • Vitis HLS • Synopsys DC • Cadence Virtuoso(Basic) • Simulink
Others: Deep Neural Network(Basic) • LaTex • Arduino

Relevant Courses

Digital Logic and Design	Communication Systems	Power Electronics
Microprocessors controllers	Signals and Systems	Power System
Analog Electronics	Digital Signal Processing	Control Systems
Circuit Theory	Digital Image Analysis*	Sensors and Measurement
Circuit Theory	*ongoing	

Positions of Responsibility

Captain | Electronics Club Aug 2018 – May 2019
Student Guide | Counselling Service May 2018 – July 2019
Core Membor | Career Development Cell Aug 2020 – Present

Achievements

- Presented poster on Approximate Multiplication at Research Conclave, IIT Guwahati.
- Presented a poster of DHVANIK on Industry Day, IIT Jodhpur.
- Secured **Bronze** medal in Inter IIT Techmeet 2019.
- Led the team of project NETRA and DHVANIK which reached the **semi-finals** of DST and Texas Instruments IICDC 2018 and 2019.
- Placed among the top 0.5% of 1.4 million applicants in JEE Advanced 2017.