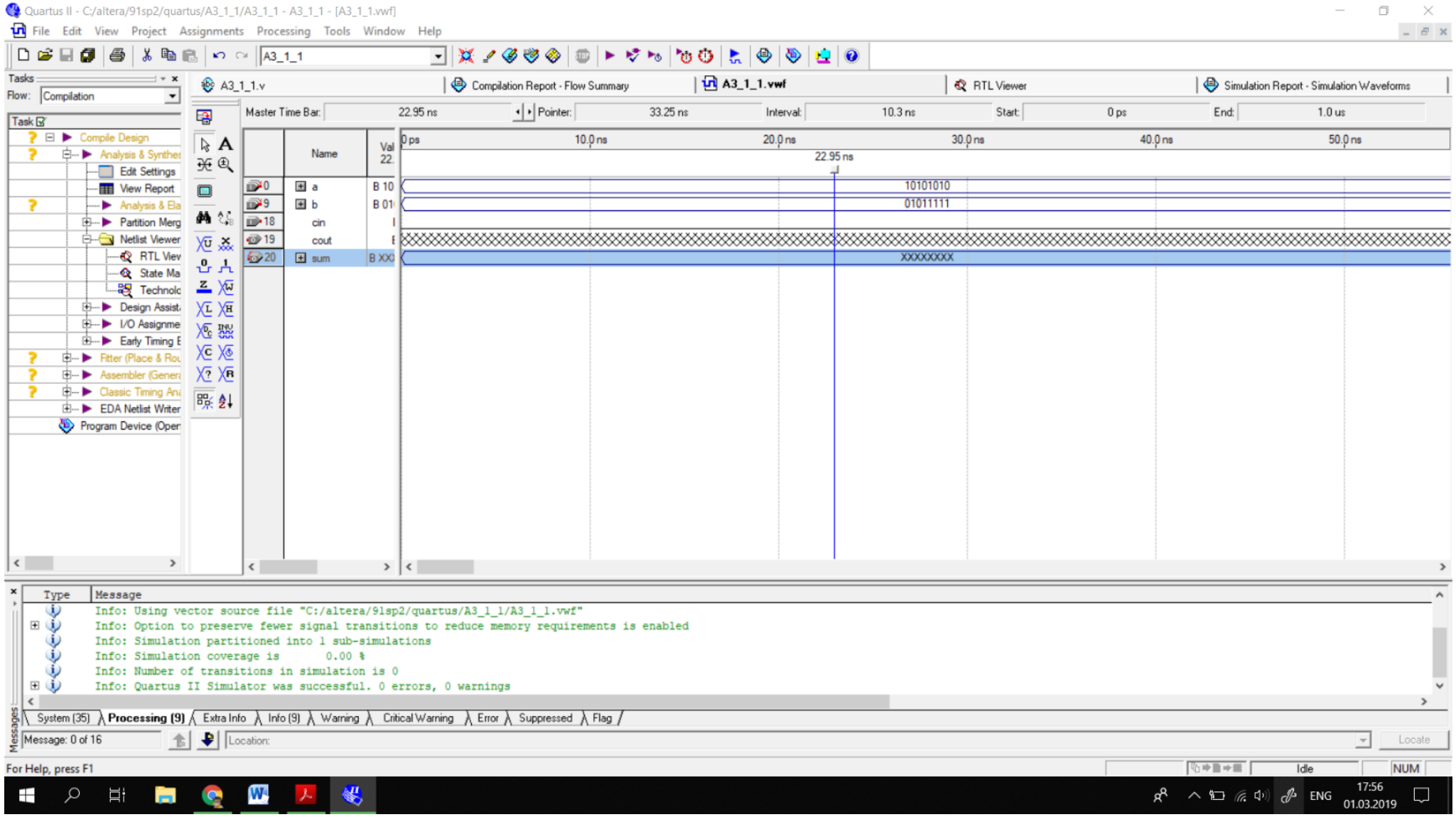
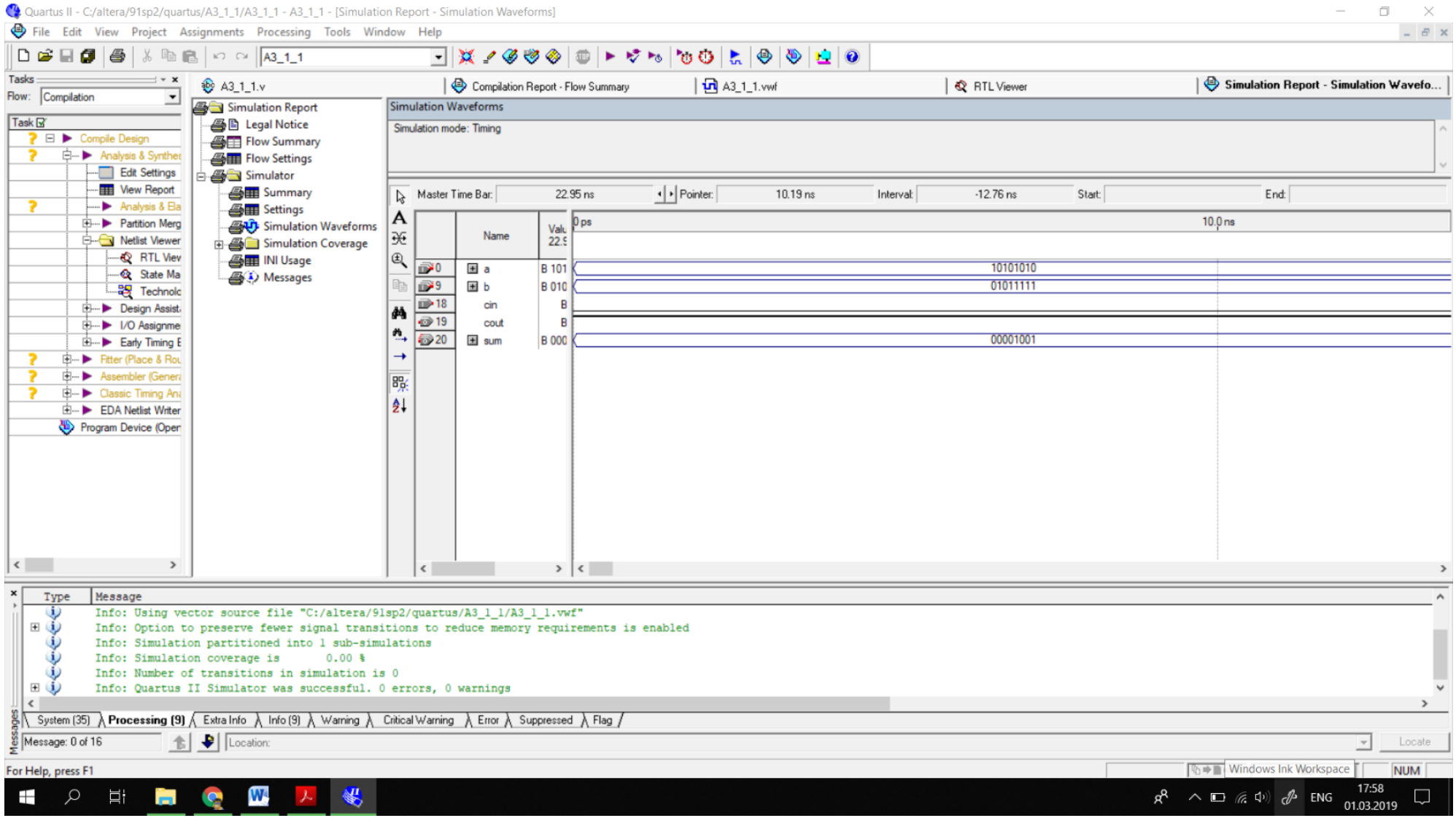
8-bit Ripple Carry Adder using Verilog HDL




Quartus II - C:/altera/91sp2/quartus/A3_1_1/A3_1_1 - A3_1_1 - [Simulation Report - Simulation Waveforms]
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22.9
0 ps
10.0 ns
0 a B 101 10101010
9 b B 010 01011111
18 cin B
19 cout B
20 sum B 000 00001001
Type Message
Info: Using vector source file "C:/altera/91sp2/quartus/A3_1_1/A3_1_1.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 0.00 %
Info: Number of transitions in simulation is 0
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
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Message: 0 of 16
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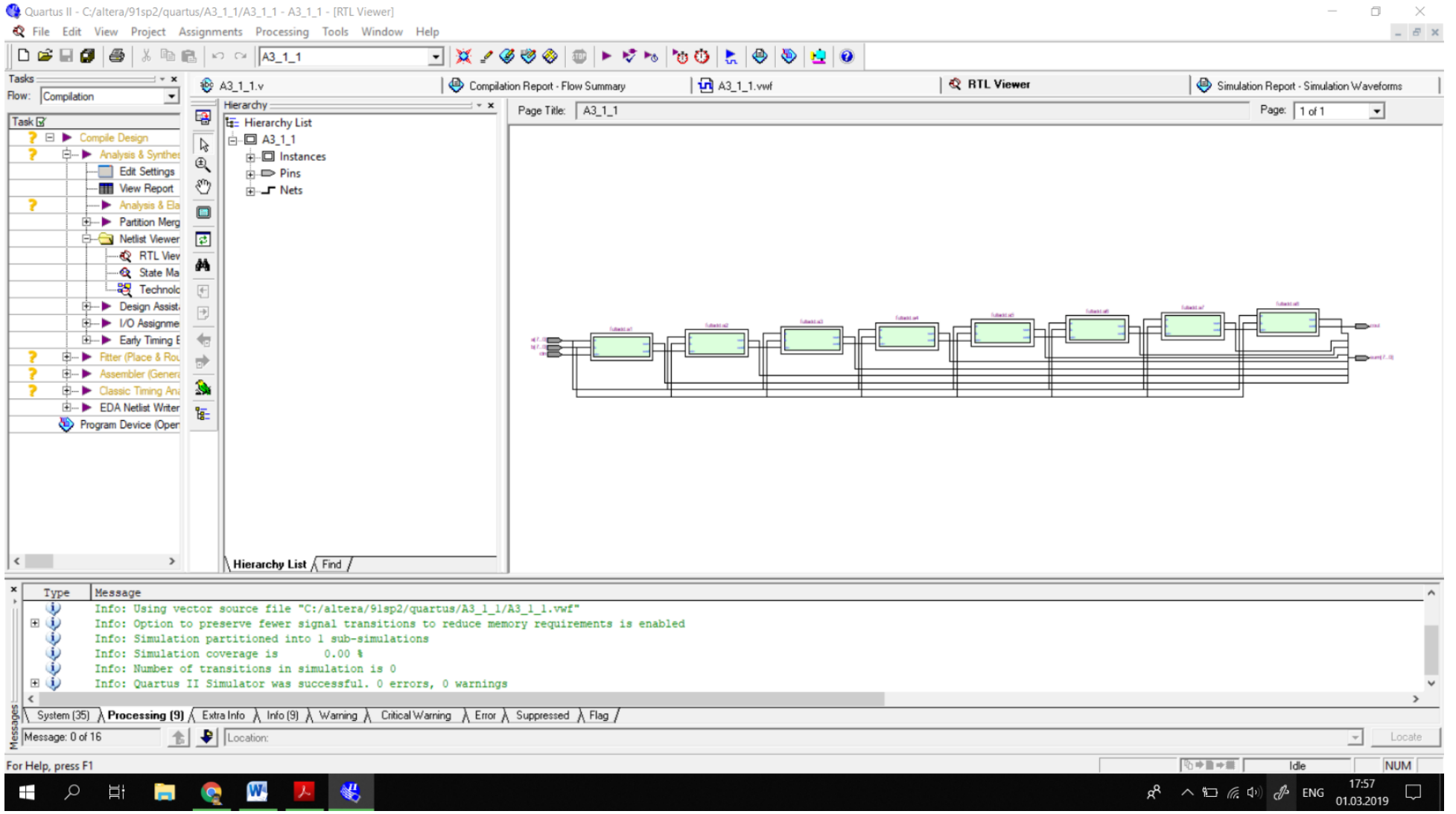
Quartus II - C:/altera/91sp2/quartus/A3_1_1/A3_1_1 - A3_1_1 - [RTL Viewer]
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Page: 1 of 1
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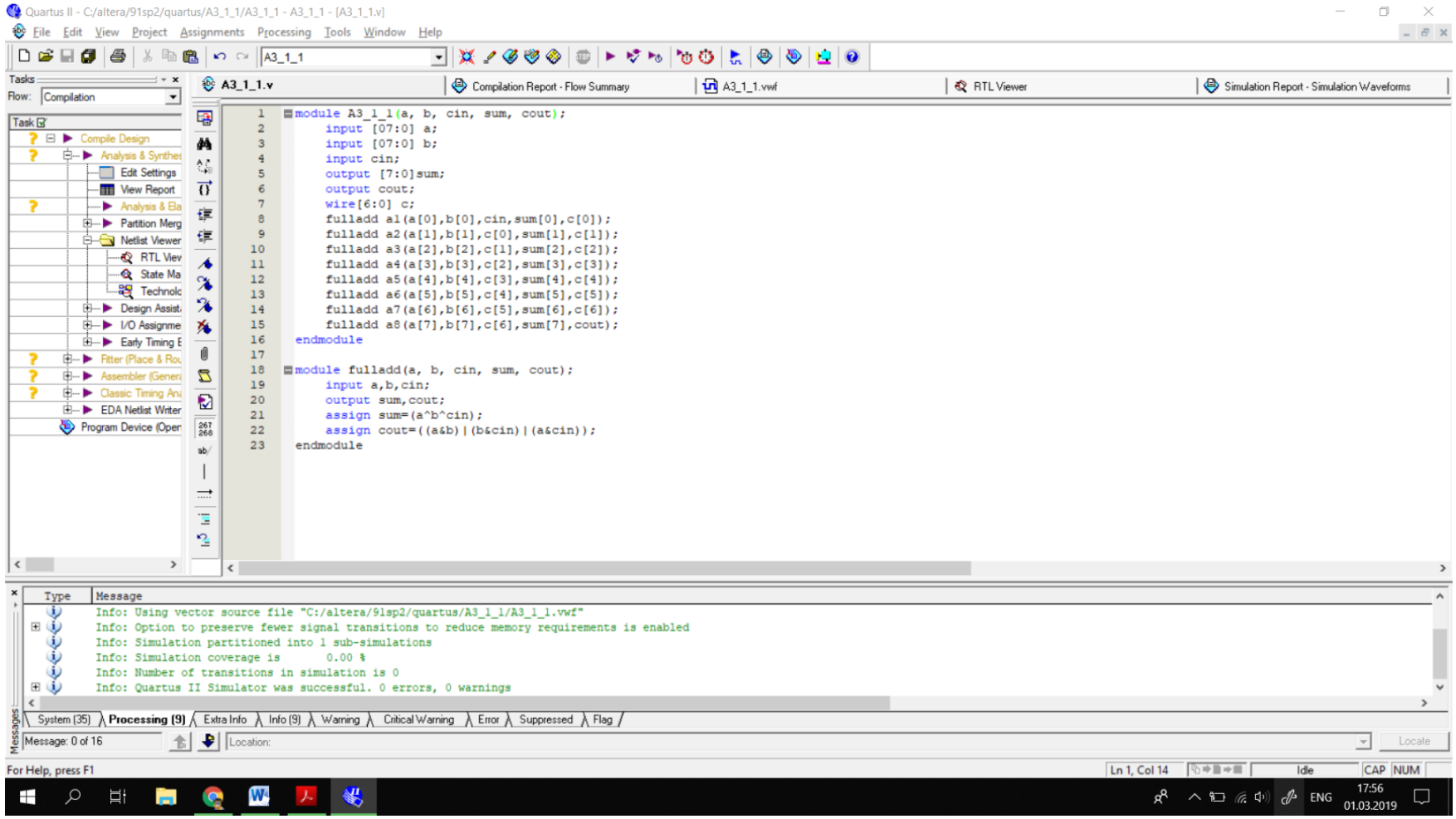
Quartus II - C:/altera/91sp2/quartus/A3_1_1/A3_1_1 - A3_1_1 - [A3_1_1.v]
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Simulation Report - Simulation Waveforms
1 module A3_1_1(a, b, cin, sum, cout);
2 input [07:0] a;
3 input [07:0] b;
4 input cin;
5 output [7:0]sum;
6 output cout;
7 wire[6:0] c;
8 fulladd a1(a[0],b[0],cin,sum[0],c[0]);
9 fulladd a2(a[1],b[1],c[0],sum[1],c[1]);
10 fulladd a3(a[2],b[2],c[1],sum[2],c[2]);
11 fulladd a4(a[3],b[3],c[2],sum[3],c[3]);
12 fulladd a5(a[4],b[4],c[3],sum[4],c[4]);
13 fulladd a6(a[5],b[5],c[4],sum[5],c[5]);
14 fulladd a7(a[6],b[6],c[5],sum[6],c[6]);
15 fulladd a8(a[7],b[7],c[6],sum[7],cout);
16 endmodule
17
18 module fulladd(a, b, cin, sum, cout);
19 input a,b,cin;
20 output sum,cout;
21 assign sum=(a^b^cin);
22 assign cout=((a&b)|(b&cin)|(a&cin));
23 endmodule
Type Message
Info: Using vector source file "C:/altera/91sp2/quartus/A3_1_1/A3_1_1.vwf"
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01.03.2019