MARIE ANNAËLLE ALISON EMILIEN

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PROFESSIONAL SUMMARY

- **Electrical engineering and computer technology student** passionate about hardware verification and the development of solutions for embedded systems, FPGAs, ASICs and Mixed-signal designs.
- Experience in digital design, simulation, and verification with **Quartus, Modelsim** and **Virtuoso XL** software gained through university projects and involvement as a teaching assistant in **digital systems** and **C programming.**
- I am looking to apply my engineering skills in an innovative and challenging environment.

EDUCATION

BASc Electrical Engineering and BSc Computing Technology **2020 – 2026**

University of Ottawa, Ottawa, Ontario

- **Scholarship**: Recipient of the Differential Tuition Fee Exemption Scholarship.
- **Relevant courseworks included**:
  - Fundamentals of Semiconductor Devices
  - Principles and Applications of VLSI Design
  - Digital Systems I and II
  - Advanced C++ Programming

SKILLS

- **Programming Languages**: Verilog, VHDL, C, C++, Python, TCL, CLI, Shell scripting.
- **Tools**: ModelSim, Jenkins, Quartus II, Altera, Cadence Virtuoso.
- **Development Environments**: Linux, Git, Jira, Agile.

ENGINEERING UNIVERSITY PROJECTS

Personal Portfolio Website Prototype *- https://alistrics.netlify.app/* ***May 2024 – Present***

- Created an interactive website to showcase my background and engineering projects (in progress).
- Developed and deployed an interactive website with Vite and React, reducing load time by 40% through efficient rendering and bundling optimization.

FPGA Calculator Verification in VHDL ***Sept 2024 – Dec 2024***

- Developed and simulated a testbench in VHDL to validate the operations of an Arithmetic and Logic Unit (ALU).
- Demonstrated skills in digital design, RTL synthesis, and hardware validation on FPGA.

Design and Simulation of Logic Gates in VLSI ***Jan 2024 – Apr 2024***

- Created optimized logic gates at the physical level, emphasizing delay reduction to enhance performance.
- Utilized Cadence Virtuoso for layout design, simulation, and verification, gaining hands-on experience in timing optimization.

WORK EXPERIENCE

University of Ottawa - Teaching Assistant - GNG 1106 and ITI 1500 ***Jan 2024 – Apr 2025***

- Guided students in learning **digital systems** and **C programming.**
- Provided individualized support to troubleshoot coding issues and debug digital system designs and scripts.

University of Ottawa - Pension and Benefits Assistant ***May 2023 – Apr 2025***

- Automated and archived administrative documents according to university standards.
- Supported employees through TOPdesk to address questions regarding pensions and benefits.
- Automated data entry and validation in Excel, reducing manual processing time by 50% and minimizing human errors.

CERTIFICATIONS

System Design and Verification Learning Map certification by Cadence

- Upon completion, gained familiarity in Cadence tools, including Jasper and Xcelium, with hands-on experience in their application.

Verilog HDL Fundamentals for Digital Design and Verification - Udemy

- In-depth study of structural, combinational, and behavioral design concepts, as well as fundamental memory architectures and Verilog functions/tasks, with hands-on practice in ModelSim.