(MARIE ANNAËLLE) ALISON EMILIEN

***Email**: aliemi@ieee.org |**LinkedIn**: /in/alison-emilien/ |**GitHub:** Alison0704 |**Website**:aliemi.com*

CAREER OBJECTIVE

- **Electrical engineering and computer technology student** passionate about hardware verification and the development of solutions for embedded systems, FPGAs, ASICs, and mixed-signal designs and various types of electronic designs.
- Experienced in **circuit design**, **simulation**, and **verification** using tools such as **Quartus**, **ModelSim**, **MATLAB**, **Virtuoso XL** and **AWR Cadence** through university projects and roles as a **teaching assistant** in digital systems and C programming.
- Proficient in **Verilog** and **C programming**, with fluency in both French and English.

Seeking to apply my problem-solving skills in an innovative environment to contribute to cutting-edge engineering solutions.

EDUCATION

BASc Electrical Engineering and BSc Computing Technology **2020 – 2026**

University of Ottawa, Ottawa, Ontario

- **Scholarship**: Recipient of the Differential Tuition Fee Exemption Scholarship.

SKILLS

- **Programming Languages**: Verilog, VHDL, C, C++, Python, TCL, CLI, Shell scripting, Web development languages.
- **Tools and Frameworks**: ModelSim, Quartus II, Altera, MATLAB, Cadence Virtuoso XL, Cadence AWR, JetBrains apps, Vite, React.
- **Development Environments**: Linux, Git, Jira, Agile, AWS.

WORK EXPERIENCE

University of Ottawa - Teaching Assistant - GNG 1106 and ITI 1500 ***Jan 2024 – Apr 2025***

- Guided students in understanding core concepts of **digital systems** and **C programming**, fostering an engaging learning environment.
- Provided individualized support to troubleshoot coding issues and debug digital system designs and scripts.

University of Ottawa - Pension and Benefits Assistant ***May 2023 – Apr 2025***

- Automated data entry, manipulation and validation in Excel, reducing manual processing time by 60% and minimizing human errors.
- Supported employees through TOPdesk to address questions regarding pensions and benefits, developing communication skills.

ENGINEERING UNIVERSITY PROJECTS

Personal Portfolio Website Prototype** – aliemi.com* ***Mar 2025 – Present

- Creating an interactive website to showcase my engineering projects using **git** best practices and **AWS** tools.
- Developing an interactive website using **Vite** and **React**, optimizing rendering and bundling to reduce load time by 40%.

FPGA Calculator Verification in VHDL ***Sept 2024 – Dec 2024***

- Debugged hardware implementation by analyzing signal waveforms and performing in-circuit testing on the **Altera FPGA.**
- Verified functionality through simulation and hardware debugging using **Algorithmic State Machines (ASM**) for structured design.

Circuit Design Microwave Amplifier ***Jan 2024 – Apr 2024***

- Designed, simulated, fabricated, and tested a microwave amplifier in a 50Ω system using an assigned NPN BJT using AWR Cadence.
- Assembled and characterized the amplifier to meet gain, stability, reflection coefficient, and bandwidth specifications.

Design and Simulation of Logic Gates in VLSI ***Jan 2024 – Apr 2024***

- Designed and implemented combinational logic gates using Cadence Virtuoso, following the full custom VLSI design flow.
- Performed post-layout verification, including DRC, LVS, and parasitic extraction, to ensure manufacturability.

Electronic design ***Jan 2023 – Dec 2023***

- Designed and analyzed various electronic circuits, including current mirrors, cascode amplifiers, buck/boost converters and op-amps.
- Developed low-pass, high-pass, and band-pass filters, analyzing frequency response and cutoff characteristics.

Analysis on signal modulation ***Jan 2023 – Apr 2024***

- Simulated and evaluated the impact of noise and filtering on modulated signals using Fourier transforms, and time-frequency analysis.
- Verified modulation and demodulation performance through **MATLAB**-based signal processing techniques.

EXTRACURRICULAR ACTIVITIES

Certificate: System Design and Verification Learning Map certification by Cadence (Ongoing)

Certificate: *Verilog HDL Fundamentals for Digital Design and Verification – Udemy* (completed Jan 2025)