Si4010 Antenna Interface and Matching Network Guide

1. Introduction

This document provides guidelines and design examples for the high impedance matching networks and loop antennas necessary for the proper usage of the Si4010 transmitter.

Section “2. High Impedance Differential Power Amplifier” gives a brief overview of the differential high impedance PA used in this chip. It also describes the method for determining the optimum termination impedance necessary to acquire the maximum power with the best efficiency.

Section “3. Inductively Tapped Loop Antenna Design Example”describes basic design steps, simulation, and measurement results for an inductively tapped printed loop antenna working at 434 MHz with the Si4010 chip and with the SOIC package. It also gives measurement data and dimensions for a 868 MHz loop antenna version.

Section “3.1. 434 MHz Antenna Dimensions and Measured Data”shows the realized loop antenna with dimensions and the test results. This section is devoted to readers who are not greatly interested in the design details of the antenna; rather, they are concerned with quickly obtaining dimension, layout, and measurement data.

Section “3.2. 868 MHz Antenna Dimensions and Measured Data with Si4010-C2-GS”briefly summarizes the measured results and dimensions of the 868 MHz tapped loop antenna.

Section “4. Matching Balun Design for Si4010 with 50 Ω Single-Ended Output” describes the design steps for the matching balun, which matches the high impedance differential outputs of the Si4010 chip to a 50 Ω single-ended termination or antenna such as monopole, spiral, ILA, etc.

Section “4.1. Matching Baluns for Si4010_B1 with SOIC and MSOP Package”gives the matching network schematic and measured results for both the SOIC and MSOP packages. These sections are useful for readers who are not greatly interested in the theoretical development of the matching network but who are concerned with quickly obtaining a set of component values for a given desired frequency of operation.

Section “5. Design of High Q Discrete Matching Baluns” describes the design procedure and operation of the matching.

2. High Impedance Differential Power Amplifier

This section discusses the operation of the high impedance class A power amplifier used in the Si4010 chips. In theory the delivered power to the load is maximum if the RF generator is terminated by the complex conjugate of its generator impedance. This is called optimum conjugate matching. However, it is true only if no constraints for voltage swing are given.

Operation of the high impedance PA is illustrated in Figure 1. High impedance PAs usually have open drain outputs and behave like a RF current generator. The TX generator impedance is represented by its parallel RC equivalent while the termination by its parallel RL equivalent. The L_{AP} and C_{TX} work in high impedance parallel resonance at the operation frequency and thus the voltage swing is determined by the residual equivalent resistance of the termination (R_{AP}) and the TX internal loss (EPR).

The drain voltage is limited by the CMOS technology. With a fixed current magnitude I_{RF}, if the generator impedance is too high, the voltage swing would exceed the limit with complex conjugate termination.

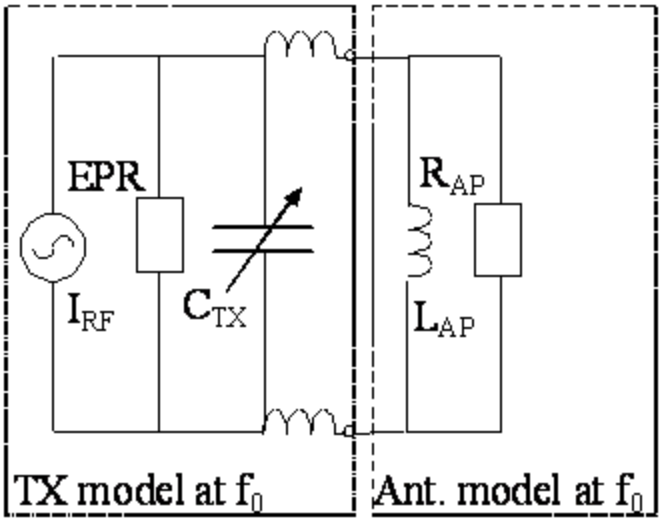


Figure 1. Operation of the High Impedance PA

In this case lower termination impedance has to be used (i.e., R_{AP}<EPR) in order to keep the voltage swing below the allowed maximum. This lower termination impedance is called "the optimum termination impedance" which achieves the maximum allowed swing and thus the maximum power with the given current magnitude. This "voltage limited" operation type is advantageous as more than 50% of the RF current flows through the parallel connected lower impedance termination and less than 50% through the internal loss. In this way the efficiency is increased. It has to be noted that the achieved power is still lower than what would be possible with the same current, applying the complex conjugate termination. However, with conjugate match, the maximum voltage limit would exceed, which may cause damage of the driver transistors.

Assuming 3.5 V differential voltage magnitude (Vmax) and square wave current waveform (i.e., switched current), the optimum resulted parallel impedance (EPR x R_{AP}) is given by Equation 1:

$$Rlo = EPR \times \frac{R_{AP}}{EPR + R_{AP}} = \frac{Vmax}{\frac{4}{\pi} \times \frac{I_{RF}}{2}} = \frac{3.5\pi}{2I_{RF}} \cong \frac{5.5}{I_{RF}}$$

Equation 1.

From this the optimum parallel equivalent resistance of the termination is given by Equation 2:

$$R_{AP} = Rlo \times \frac{EPR}{EPR - Rlo}$$

Equation 2.

It is in the range 500–600 Ω in the highest power state (max. current) with low cap bank settings.

However, this calculation is valid only in the internal die drain points. Due to the series parasitic inductances (bond wire+leadframe+pcb) the allowed voltage swing and thus the optimum impedance is lower between the external TX pins. Typical total (two arm together) value of this parasitic inductance is 2.9 nH and 1.3 nH for the SOIC and MSOP package, respectively.

Table 1 and Table 2 give the external optimum termination impedance, admittance, and the parallel RL equivalent for the testcards with SOIC and MSOP packages at maximum power state operation. The optimum cap bank settings are also given.

The voltage limited operation mode is typical at the highest power settings (highest current) of the Si4010 chip, where the delivered power to the optimum differential termination is ~ +10 dBm.

A second important operation mode is when the current magnitude is reduced (e.g. to reduce the power) and thus the maximum allowed voltage swing is not achieved even if the conjugate complex termination is applied. In this case the PA is "current limited". This is the typical case when the Si4010 chip works in a strongly reduced power state or when the internal capacitance bank state is high (close to maximum at low bands and above ~100 in high bands). In this operation mode the optimum termination is the complex conjugate.

A third, non-optimum mode is when the current is maximum, but the termination impedance is so low that the maximum swing is not achieved. In this case the termination is not the optimum, and the power and efficiency is lower than the possible maximum. All operation modes are covered and the parameters can be calculated easily by the 401x calculator: e.g., the parallel equivalent of the optimum termination can be found in the “Antenna Target” fields. More details about this calculator can be found in AN457.

Table 1. SOIC Maximum Power Operation

Freq [MHz] SOIC	Opt. load imp. [Ω]	Opt. load adm. [mSie]	Parallel Eqv. R_{AP} [Ω]	Parallel Eqv. L_{AP} [nH]	Cap. bank state & TX equivalent capacitance (CTX)	Power to the differential load [dBm]
315	28.6+j114	2.07-j8.25	483	61.2	99, 4.17 pF	10.7
434	32.5+j120	2.09-j7.74	479	47.4	23, 2.84 pF	10.6
868	8.1+j58	2.39-j17	419	10.8	17; 3.12 pF	9.7
915	7.1+j54	2.45-j18.3	409	9.7	17, 3.19 pF	9.6

Table 2. MSOP Maximum Power Operation

Freq [MHz] MSOP	Opt. load imp. [Ω]	Opt. load adm. [mSie]	Parallel Eqv. R_{AP} [Ω]	Parallel Eqv. L_{AP} [nH]	Cap. bank state & TX equivalent capacitance	Power to the differential load [dBm]
315	27+j114	1.98-j8.3	505	60.8	105, 4.2 pF	10.7
434	32.3+j124	19.7-j7.6	508	48.5	23, 2.77 pF	10.6
868	8.3+j66	1.88-j14.9	532	12.3	13, 2.73 pF	9.8
915	7.3+j62	1.87-j15.9	535	11	13, 2.76 pF	9.7

3. Inductively Tapped Loop Antenna Design Example

3.1. 434 MHz Antenna Dimensions and Measured Data

This antenna design uses the Si4010-C2-GS version of the Si4010 chip. The designed antenna top layout with final outer dimensions is shown in Figure 2. The bottom layout is shown in Figure 3. The schematic is shown in Figure 4. The manufacturing pack (including CAM/CAD/PDF files and the BOM) is available at www.silabs.com. The whole unit is encapsulated by the Polycase FB-20 plastic enclosure as shown in Figure 5 and Figure 6.

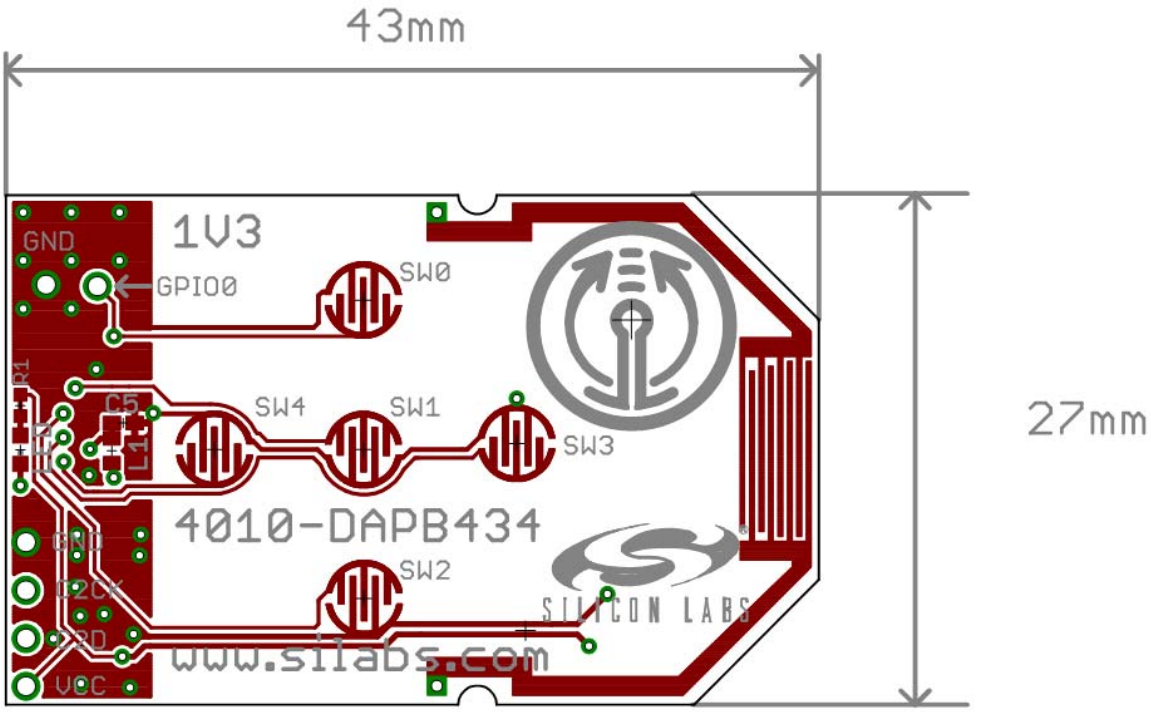


Figure 2. Antenna Top Layout with Final Outer Dimensions

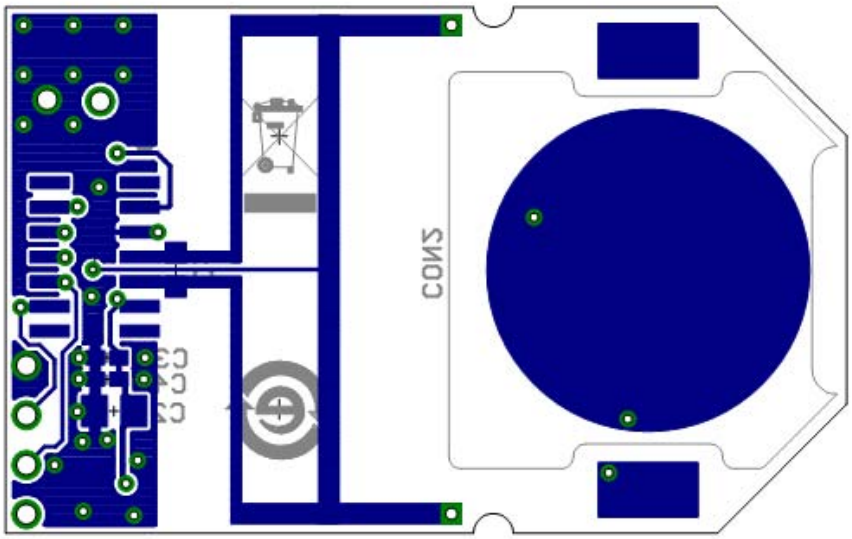


Figure 3. Antenna Bottom Layout with Final Outer Dimensions

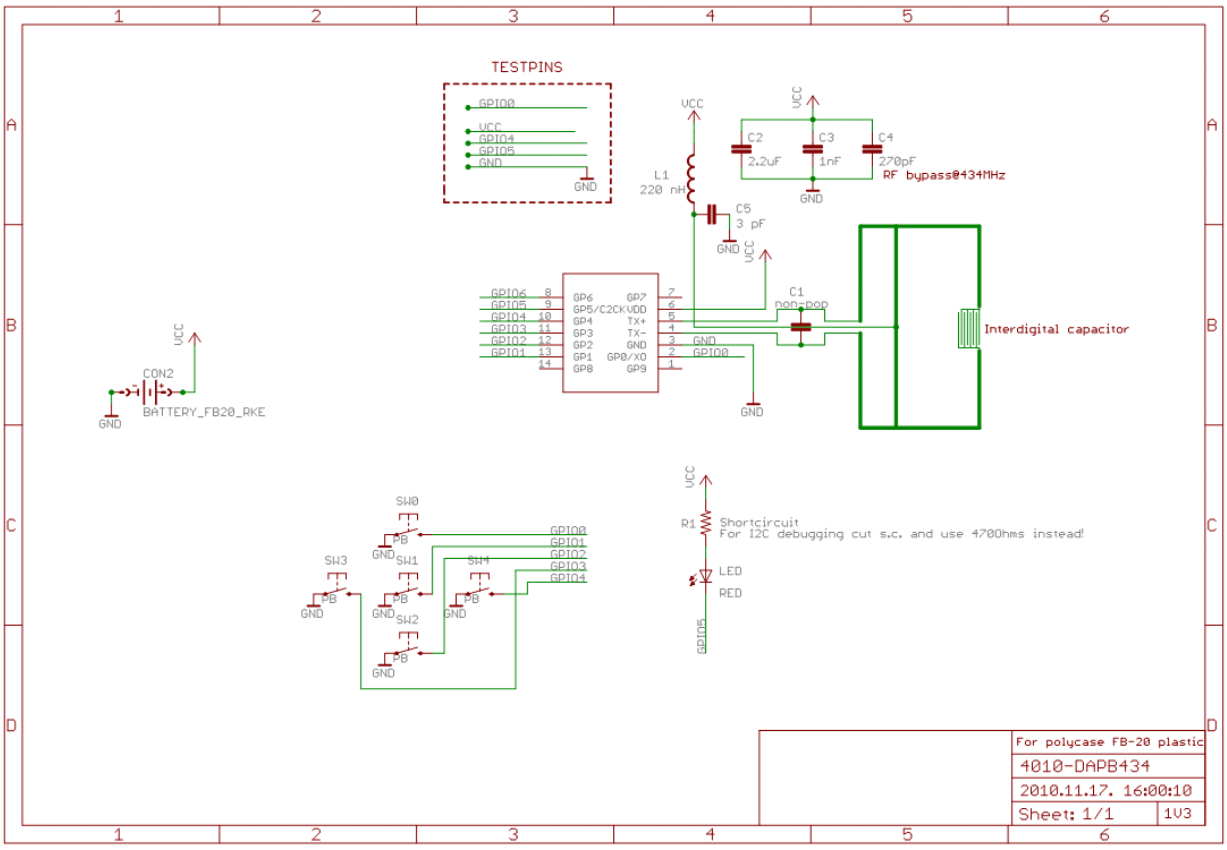


Figure 4. 4010-DAPB434 Schematic

The maximum of the radiated fundamental, second and third harmonic power in 10 mA (PA boost function) tail current state are given in Table 3. During the measurements the direction and the orientation of the unit are turned until the maximum is found.

In these measurements the maximum at three cuts and with different receiver antenna polarizations is given.

Table 3. Maximum of the Radiated Fundamental, Second and Third Harmonic Power of the 4010-DAPB434 Board

EIRP [dBm]			
H-pol receiver, 10 mA			
	Plane		
	XY	**ZY**	**ZX**
434 MHz	–11.39	–19.37	–19.83
868 MHz	–54.3	–55.4	–58.6
1302 MHz	–43.65	–48.5	–57.15
V-pol receiver, 10mA			
	Plane		
	XY	**ZY**	**ZX**
434 MHz	–30.61	–17.67	–18.42
868 MHz	–58.6	–52.3	–50.8
1302 MHz	–51.75	–42.75	–37

Figure 5. Si4010-DAPB434 in the Plastic Enclosure (Bottom)

Figure 6. Si4010-DAPB434 in the Plastic Enclosure (Top)

3.2. 868 MHz Antenna Dimensions and Measured Data with Si4010-C2-GS

This antenna design uses the Si4010-C2-GS version of the Si4010 chip. The designed antenna top layout with final outer dimensions is shown in Figure 7. The bottom layout is shown in Figure 8. The schematic is shown in Figure 9. The manufacturing pack (including CAD/CAM/PDF files and the BOM) is available at www.silabs.com. The whole unit is encapsulated by the Polycase FB-20 plastic enclosure as shown in Figure 10 and Figure 11.

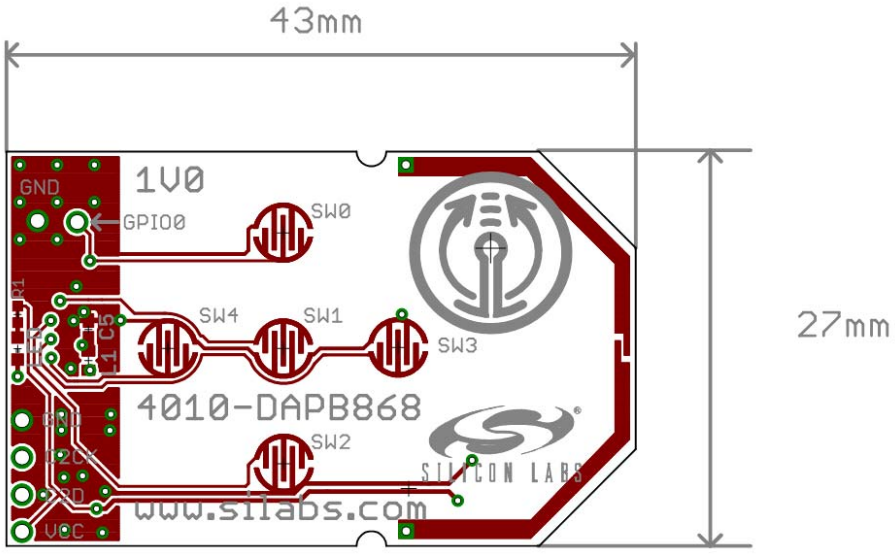


Figure 7. Antenna Layout with Final Outer Dimensions

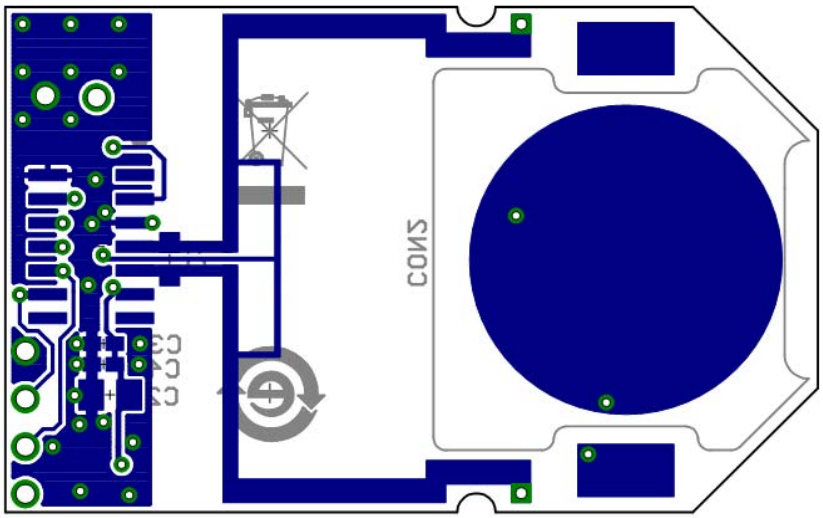


Figure 8. Antenna Bottom Layout

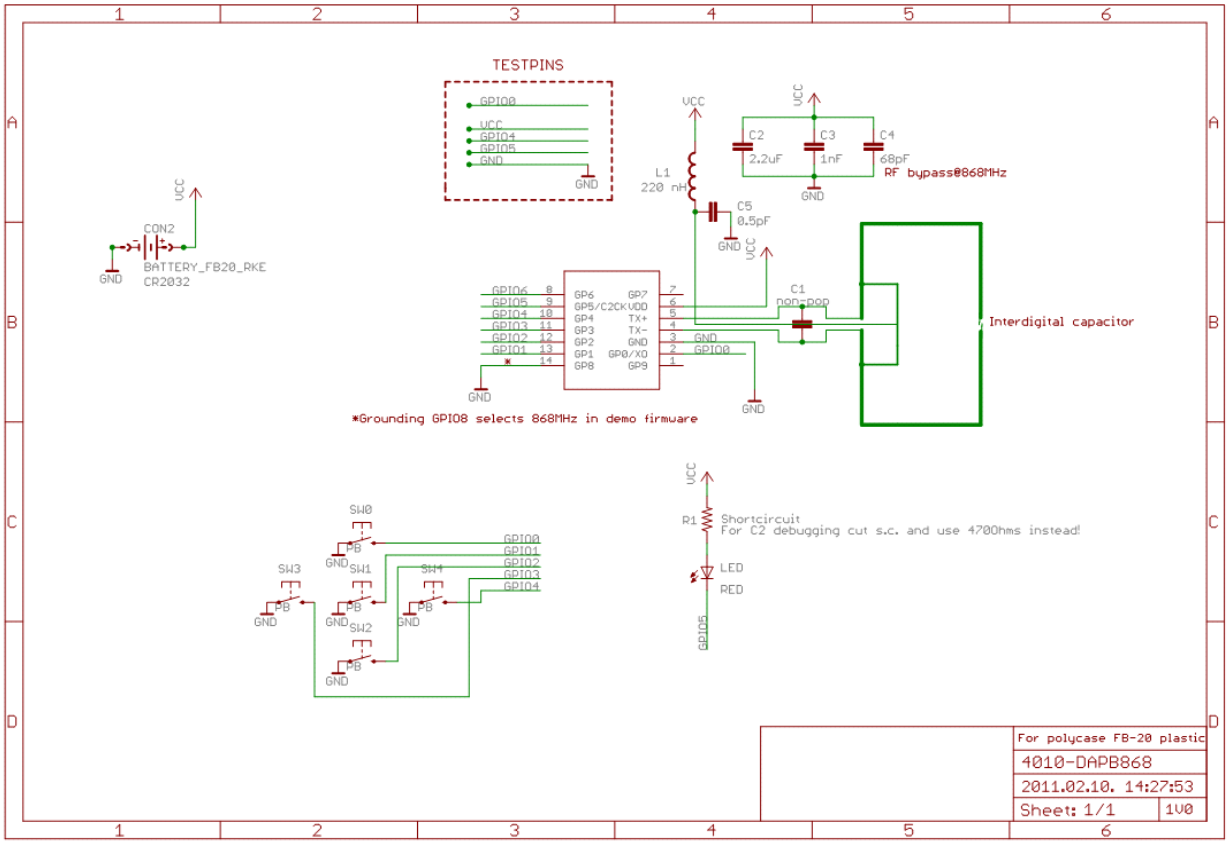


Figure 9. 4010-DAPB868 Schematic

Figure 10. 4010-DAPB868 in the Plastic Enclosure (TOP)

Figure 11. 4010-DAPB868 in the Plastic Enclosure (BOT)

The maximum of the radiated fundamental, second and third harmonic power in 10mA (PA boost function) tail current state are given in Table 4. During the measurements the direction and orientation of the unit are turned until the maximum is found. In these measurements the maximum at three cuts and with different receiver antenna polarization is given.

Table 4: Maximum of the Radiated Fundamental, Second, and Third Harmonic of the 4010-DAP868 Board

EIRP [dBm]			
H-pol receiver, 10 mA plane			
	XY	**ZY**	**ZX**
868 MHz	–1.9	–12.7	–8.0
1736 MHz	–32.3	–26.7	–27.5
2604 MHz	–25.2	–28.2	–33.2
V-pol receiver, 10 mA plane			
	XY	**ZY**	**ZX**
868 MHz	–19.6	2.2	–0.6
1736 MHz	–32.7	–27.5	–23.7
2604 MHz	–37.5	–31.0	–28.0

However the unit pass ETSI/FCC regulations in +10 dBm (PA boost function) setting it is advised to use it in +7 dBm mode (PA max drive level off) to keep safety margin to the regulation limits.

3.3. Detailed Antenna Design Steps Using a Planar EM Simulator (Sonnet)

For the antenna design the Sonnet 2.5D EM simulator is used. The goal is to design the optimum antenna impedance for the PA which results in the maximum power delivery to the antenna at cap bank state 80. The reactance of this optimum antenna impedance is resonating with the PA output capacitance at internal capacitance bank state of 80. That is close to the lower edge of the output capacitance tuning range of the Si4010 (0–511) in order to increase the Q factor of the PA and thus decrease the internal losses. A basic EM simulated planar structure is shown in Figures 12–14.

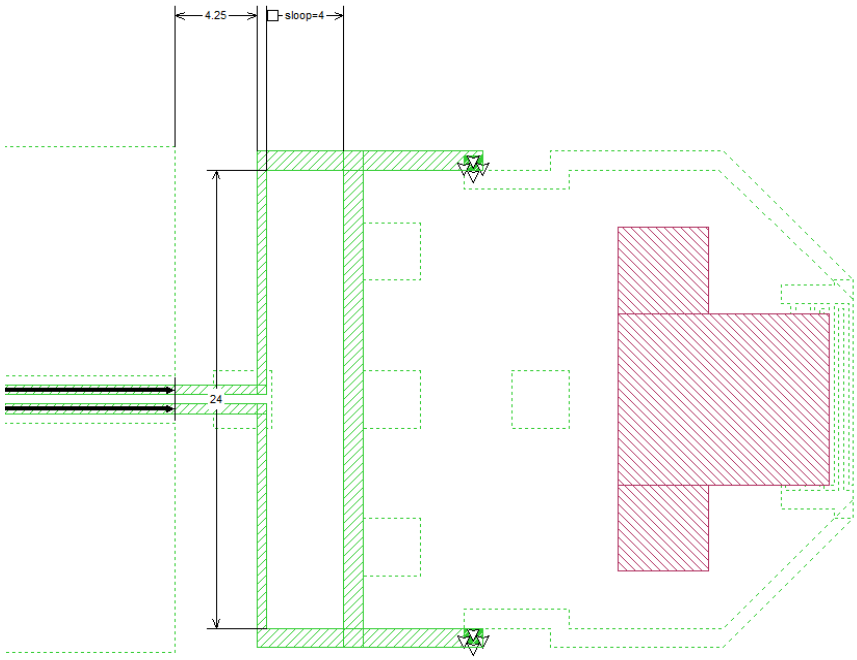


Figure 12. Antenna Simulation (Bottom)

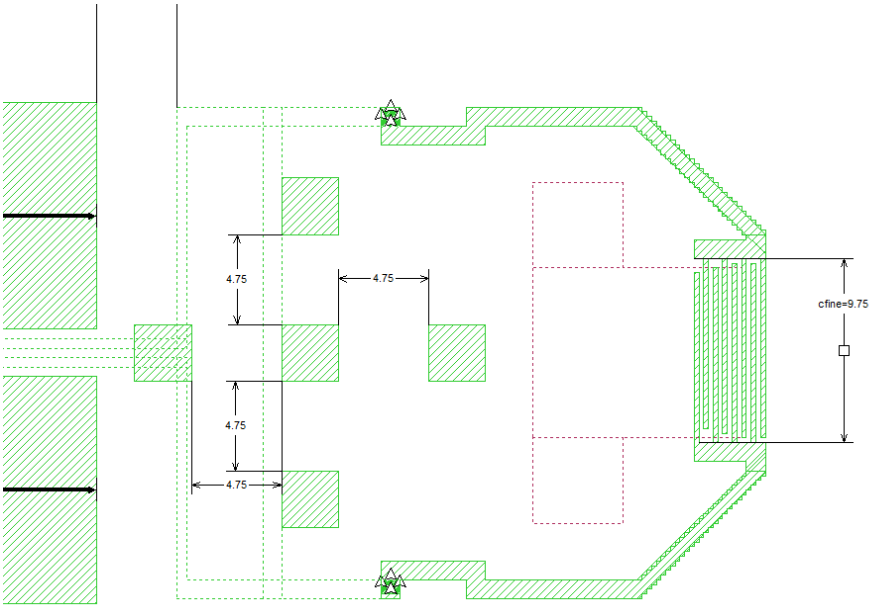


Figure 13. Antenna Simulation (Top)

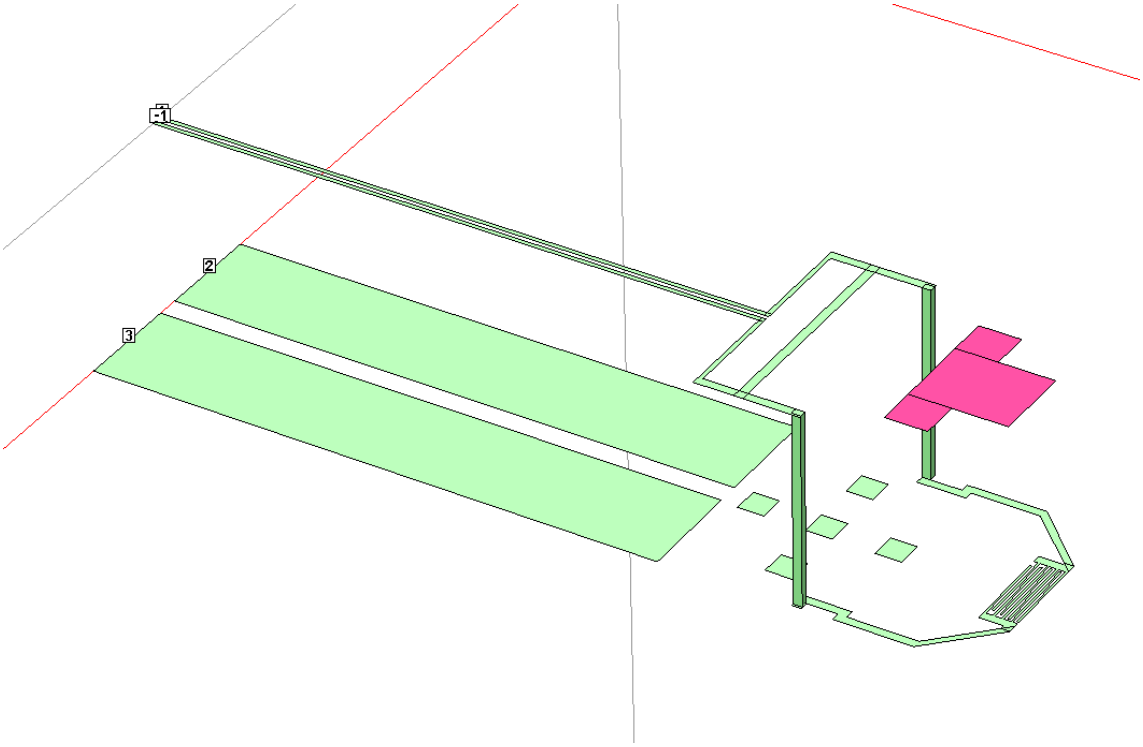


Figure 14. Antenna Simulation in 3D

The antenna is fed from the left side through a differential transmission line. This transmission line is de-embedded from the simulation by port extension. The reference plane of the simulation is shown by the black arrows. The ground planes on both side of the transmission line represent the PCB area of the unit's circuitry. The antenna is an inductively tapped loop with the series capacitance in the main loop realized by a printed interdigital capacitor.

The usage of an interdigital printed capacitor has many advantages:

- Fine-tuning possible
- No need for an extra component
- Reduced value spreading due to the interdigital technique

In this design concept the Si4010 and the whole circuitry is outside of the antenna area. With this structure, outside connection to the circuitry is easier. In theory, the whole circuit could be placed inside the antenna area. Unfortunately, the increase of the useful antenna area due to this would be negligible but the interfacing of the circuitry would be much more difficult.

The unit is working from a CR2032 battery. The battery is placed at the bottom side beneath the printed capacitor (see the round shape battery's pad at the bottom layer in Figure 3.) In this way:

- The interdigital capacitor does not occupy additional space from the antenna area.
- The battery and the metallization around it give some shielding and thus reduce the detuning of the printed capacitor in the vicinity of a hand.

The simulation box size is: 180 mm due to 128 MB memory restrictions of the applied Sonnet level version. With this box size, the boundaries are far enough to avoid the disturbance of the antenna near field and thus the reactive impedance part (i.e., the antenna inductance) estimation is quite accurate. Unfortunately, the distance is not big enough to accurately estimate the far field radiation of the antenna. Due to this, the antenna gain and the radiation resistance is not accurately simulated. With a bigger boundary box, which consumes more memory and requires a higher level Sonnet V11 EM license, accurate far field simulation is possible. Also the structure can have a maximum of 2 metal layers and 6 ports with this Sonnet level. Despite this, the real part of the antenna impedance is estimated relatively well as the ohmic and dielectric loss is usually dominant compared to the radiated loss in case of small loop antennas. During the simulation, the antenna is terminated by an ideal capacitance which models the Si4010 output capacitance at cap bank state 80. Its typical value is ~3.8 pF. The antenna and the PA capacitance together form a parallel resonant circuit and with proper antenna design the resonance occurs at the targeted operation frequency.

Figure 15 shows the used impedance parameters derived by the Si4010 optimum antenna impedance calculator (Si4010_calc_regs_100928.xls). According to this, the optimum values in the parallel RL equivalent of the antenna are: Real_Z=517 Ω, ImagZ=96.43 Ω at 434 MHz. It corresponds to 35.4 nH antenna inductance which is in resonance with the 4010 output capacitance (3.8 pF) at 434 MHz.

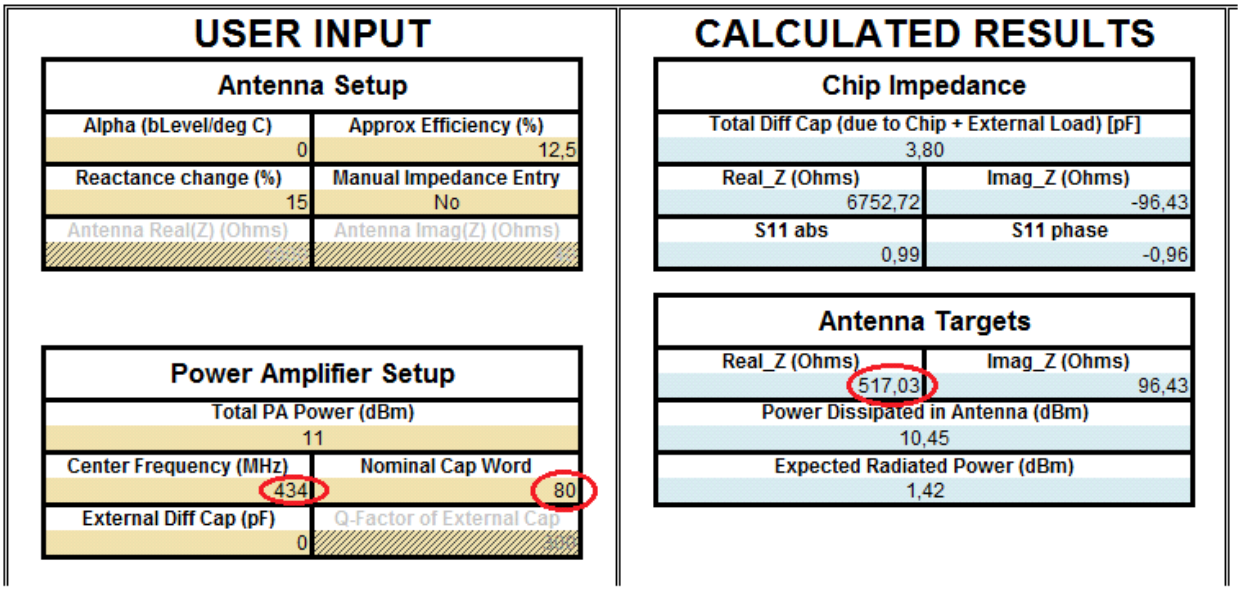


Figure 15. Antenna Targets, Calculated by Si4010 Excel Calculator Sheet

Simulated impedance:

The simulated antenna impedance with 3.8 pF at the input is shown in Figure 16. The resonance is near 434 MHz (the slight detuning will be compensated by the automatic tuning).

The residual impedance at resonance is ~517 Ω.

Note: Accurate tuning of the real impedance part is difficult due to the strong tapping ratio.

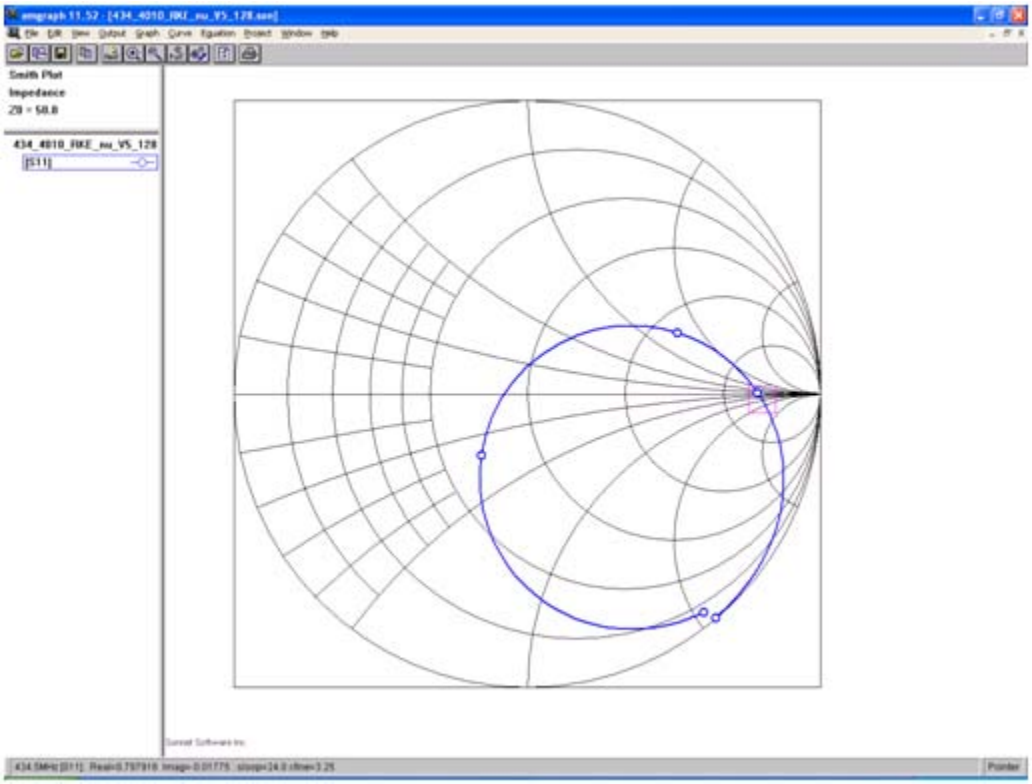


Figure 16. S11 Real/Img Resonance at 434 MHz, Cload=3.8 pF

4. Matching Balun Design for Si4010 with 50 Ω Single-Ended Output

The Si4010 transmitter can be used with single-ended 50 Ω antennas (monopole, spiral, ILA, IFA, etc.) as well if an external matching balun is used between the high impedance differential output of the chip and the 50 Ω single-ended load. The matching balun performs four important tasks with minimal insertion loss:

- Provides the optimum termination impedance (see Section “2. High Impedance Differential Power Amplifier”) to the differential output of the chip if the single-ended port of the balun is terminated by 50 Ω. At high power states the differential output is usually not terminated in the complex conjugate way. (See the "voltage limited" operation mode in Section “2. High Impedance Differential Power Amplifier”. In this case, the S11 parameter will not provide good return loss at the 50 Ω port, but the matching will provide the possible highest power.)
- Makes the balun function, i.e. adds the two differential outputs in-phase, with equal magnitudes.
- Makes suppression on the 2nd harmonic by using a 2nd harmonic trap.

Unfortunately, as the Si4010 outputs are working with the termination (here, the differential port of the balun) with high Q parallel resonance, optimum wideband solution is very difficult or even impossible to design.

If the power requirement is significantly relaxed, a possible wideband solution can be to use a coil-type balun. In this case, however, the termination impedance is far from optimum and the power is lower (i.e, this is a compromise).

In this application note narrowband, nearly optimum matching baluns are described, which use 0402SMD elements with different element values at the different bands.

In the design the losses and parasitic of the SMD elements and the pcb traces are compensated, and due to this it is strongly recommended to use the pcb layout proposed by Silicon Labs.

Also to comply with regulatory standards (ETSI, FCC, etc.), additional 3rd order filtering is necessary at the single-ended side. The proposed balun circuits comprise these filter sections.

4.1. Matching Baluns for Si4010_B1 with SOIC and MSOP Package

This section is useful for readers who do not intend to deeply understand the fundamental operation of the high Q matching balun, but rather are concerned with quickly obtaining a set of component values for a given desired frequency of operation.

The presented baluns shows nearly the optimum impedances listed in Table 1 and Table 2 on page 3 for the Si4010 outputs if the single-ended port is terminated by 50 Ω.

Also in the balun function the magnitude mismatch is lower than 6% (typically 2-3%) and the phase error is lower than 5 degrees (typically 2 degrees). Fortunately, these levels of residual losses have minimal effect (~0.1 dB) on the operation of the matching balun. The main sources of these mismatches are the discrete steps of the available SMD components.

In the design, the losses and parasitic of the SMD elements and the pcb traces are compensated. Due to this it is strongly recommended to use the pcb layout designs proposed by Silicon Labs around the Si4010 outputs, V_{DD}, grounding, etc.

The loss of the matching core is ~0.5 dB typically. The filters introduce 0.3–0.5 dB additional loss at the operation frequency. These loss values are achieved by using high Q wirewound inductor (Coicraft 0402HP series) and capacitor (Murata GRM155 series) types. Usage of lower Q elements (e.g., multilayer inductors) can cause 0.5–1 dB additional loss.

The presented baluns comply with regulatory standards, and for this they comprise the filters at their 50 Ω side.

4.1.1. SOIC Matching Baluns

The schematic of the balun proposed for the SOIC packaged Si4010 is shown in Figure 17. The element values ar given in Table 5.

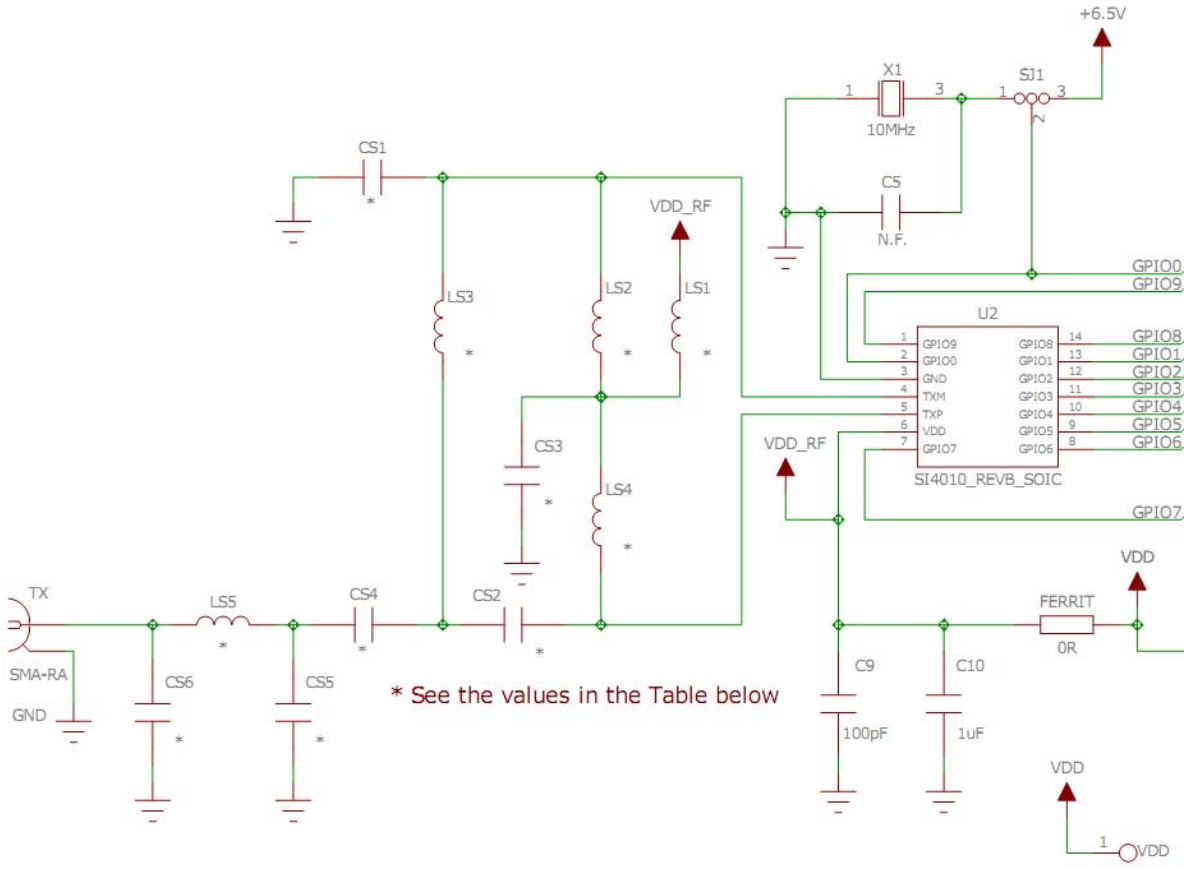


Figure 17. Si4010 SOIC Matching Network Schematic

The top layer of the Silicon Labs testcard is shown in Figure 17. It is recommended to copy and use the RF layout around the chip as it is. The gerbers of the board can be found on the Silicon Labs website.

Table 5. Matching Element Values for SOIC Packaged Si4010

SOIC	LS1	C3	LS2	LS4	CS1	CS2	LS3	LS5	CS5	CS6	CS4
315M	220 nH	4.7 pF	20 nH	20 nH	5.6 pF	3 pF	100 nH	25 nH	8.2 pF	8.2 pF	390 pF
434M	220 nH	2.7 pF	16 nH	16 nH	3.9 pF	2 pF	56 nH	18 nH	6.8 pF	6.8 pF	270 pF
868M	120 nH	3 pF	2.7 nH	2.7 nH	2.7 pF	1.5 pF	24 nH	6.8 nH	5.1 pF	5.1 pF	68 pF
915M	120 nH	3.3 pF	2 nH	2 nH	2.7 pF	1.5 pF	24 nH	6.8 nH	3.9 pF	3.9 pF	56 pF

Unfortunately, around 2.2 GHz, the 50 Ω balun core output (at the C1 capacitor, before the filter) has a very low impedance and thus the filter could not attenuate properly. To avoid this, a 8.5 mm long
50 Ω coplanar transmission line is introduced between the C1 capacitor and the filter. This line transforms the impedance to higher values around 2.2 GHz. In this way, significant reduction of the harmonics around this frequency (5th of the 434 MHz and 3rd of the 868 MHz board) is achieved.

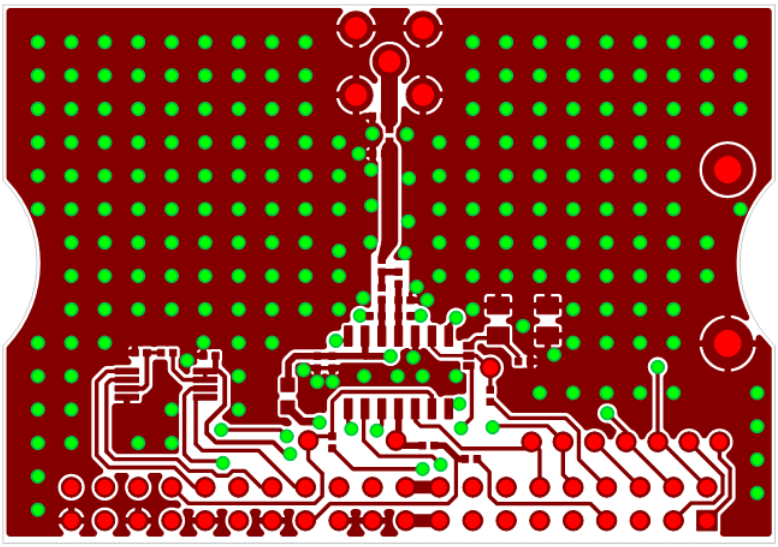


Figure 18. Top Layout of the SI Testcard with SOIC Packaged Si4010

The measured conducted spectrum of the 315, 434, 868, and 915 MHz testcard up to 3.6 GHz is shown in Figures 19, 20, 21, and 22, respectively. The realized matchings have ETSI compliance at 434 and 868 MHz and FCC compliance at 315, 434, and 915 with properly reduced power in this conductive measurement. Assuming 0 dB gain antenna, the compliance will be observed in radiated measurements as well.

The typical power with SOIC package is ~9.5 dBM at low bands and ~8.5 dBM at high bands. Due to the loss of the match and the filter, the power delivered by the 4010 output is at least 1 dB higher. That is the power delivered to a properly designed differential antenna input having the optimum impedance without external tuning elements.

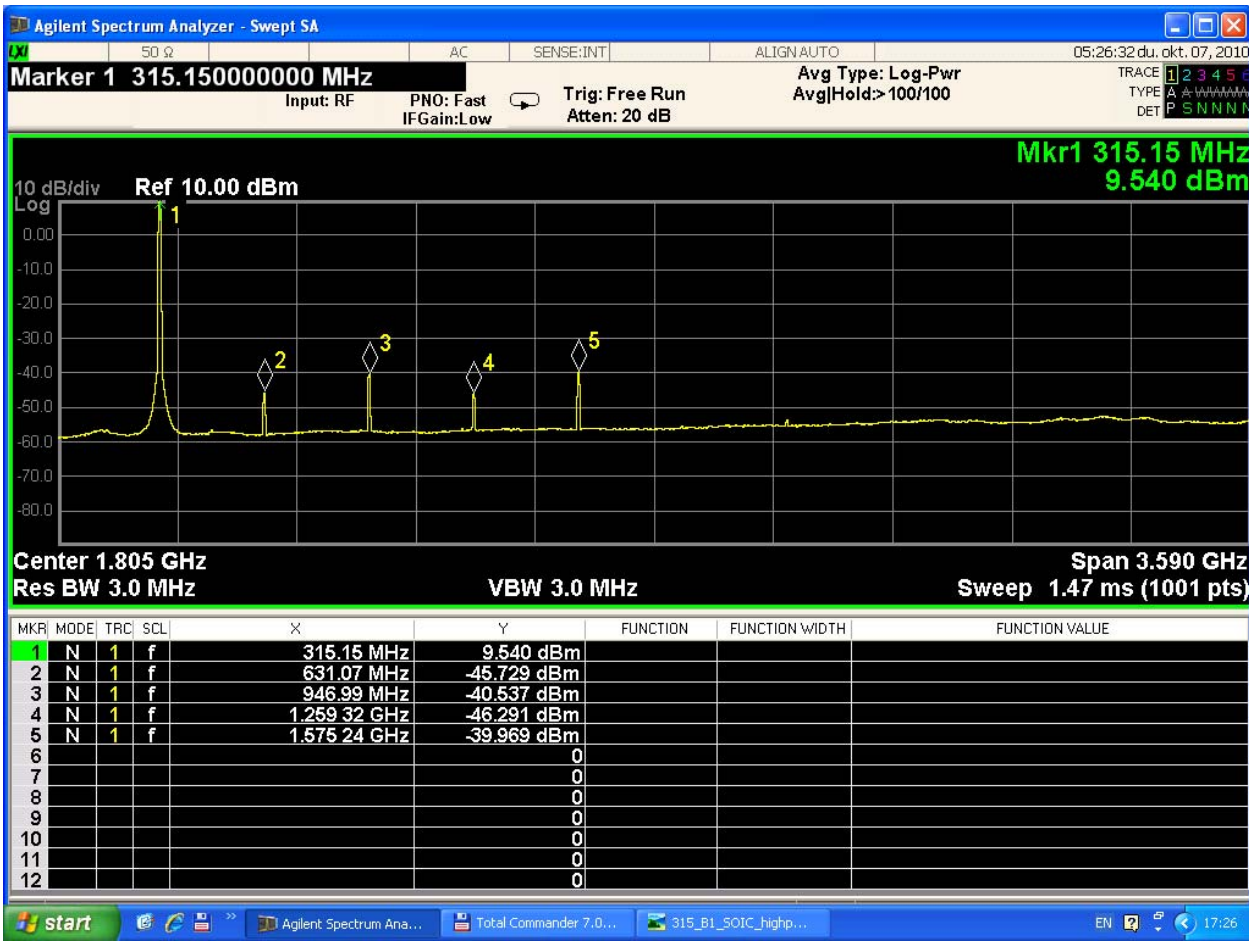


Figure 19. Measured Output Spectrum of the 315MHz SOIC Card Up to 3.6 GHz

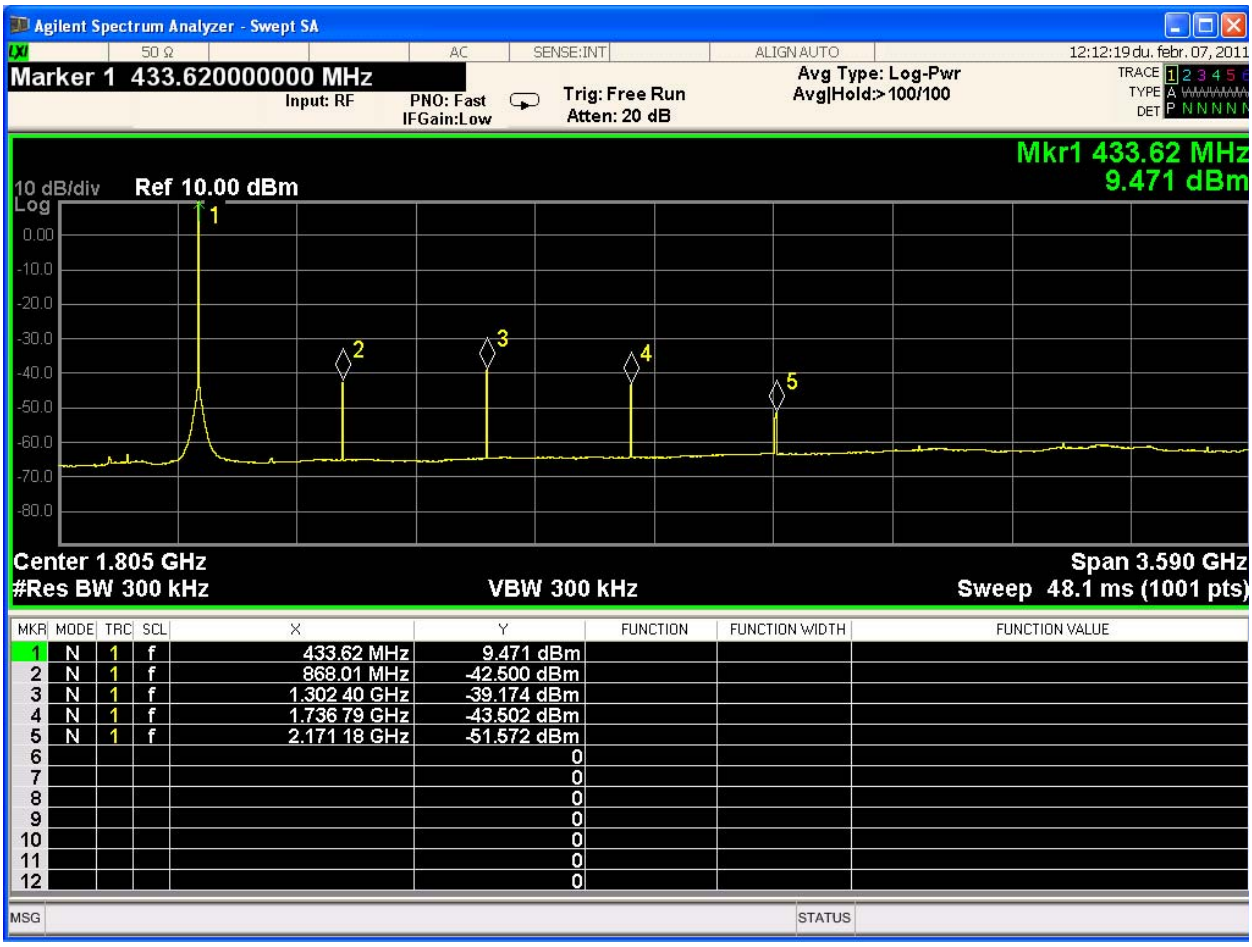


Figure 20. Measured Output Spectrum of the 434 MHz SOIC Card up to 3.6 GHz

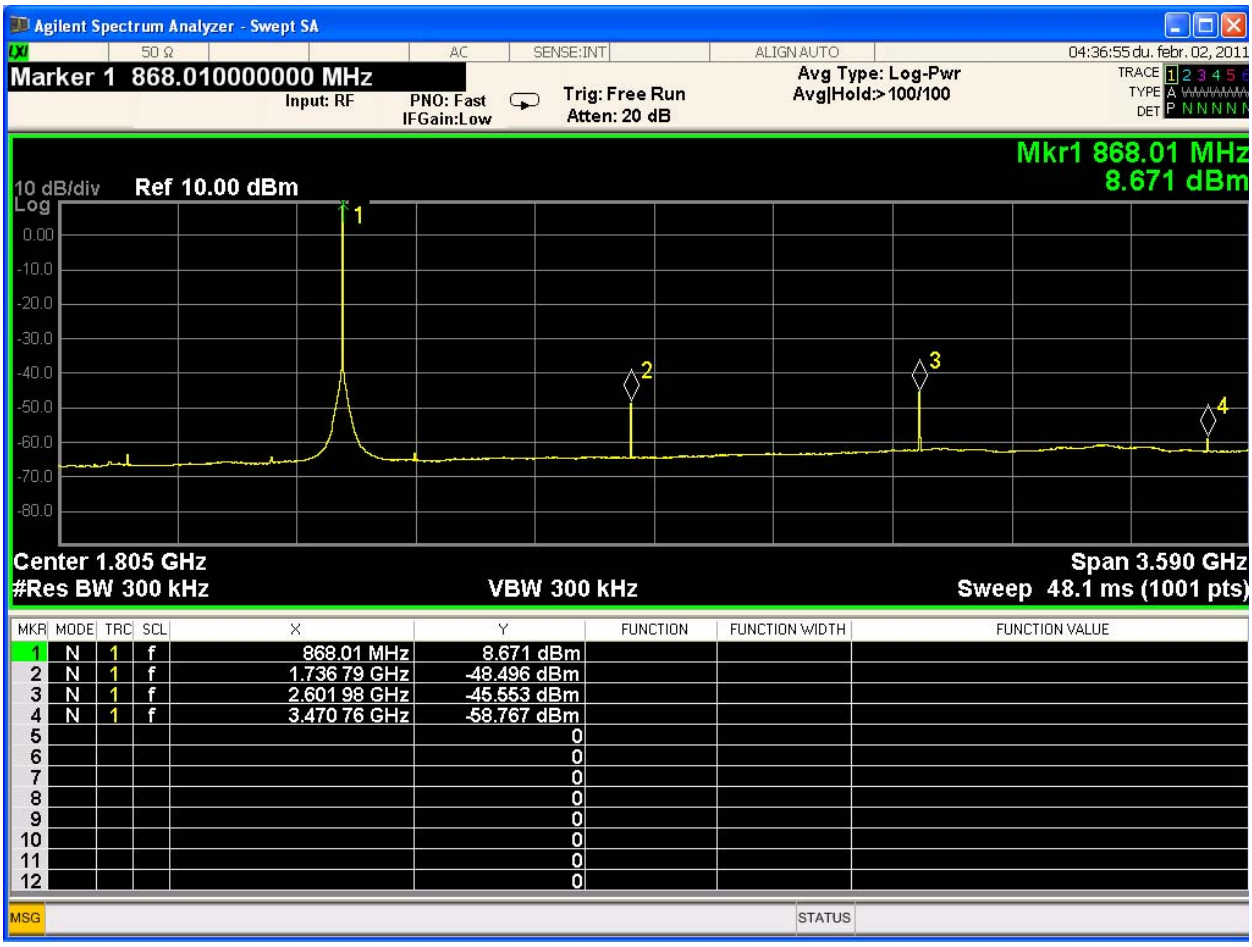


Figure 21. Measured Output Spectrum of the 868 MHz SOIC Card up to 3.6 GHz

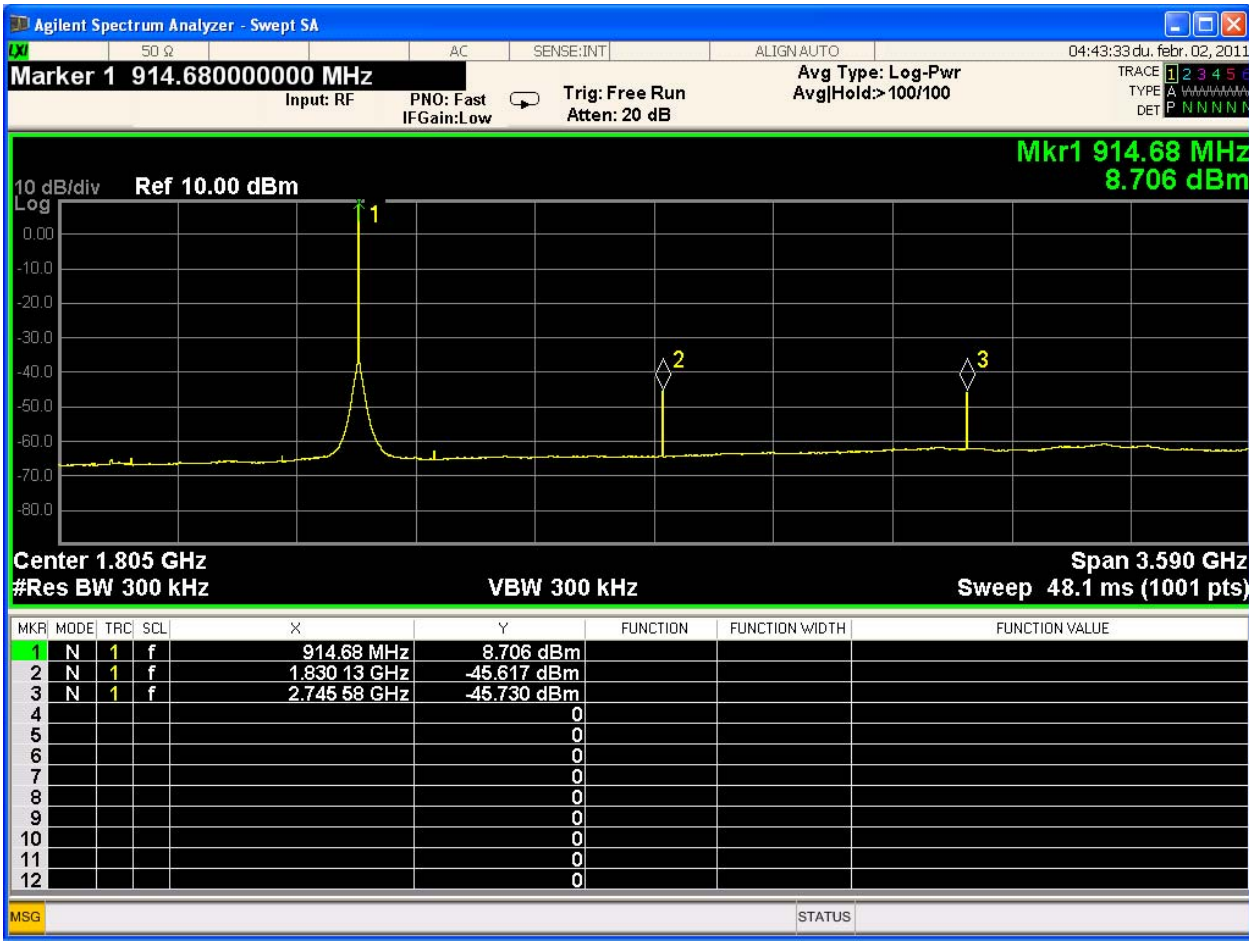


Figure 22. Measured Spectrum of the 915 MHz SOIC Card up to 3.6 GHz

4.1.2. MSOP Matching Baluns

The schematic of the balun with MSOP packaged Si4010 is shown in Figure 23. The element values are given in Table 6.

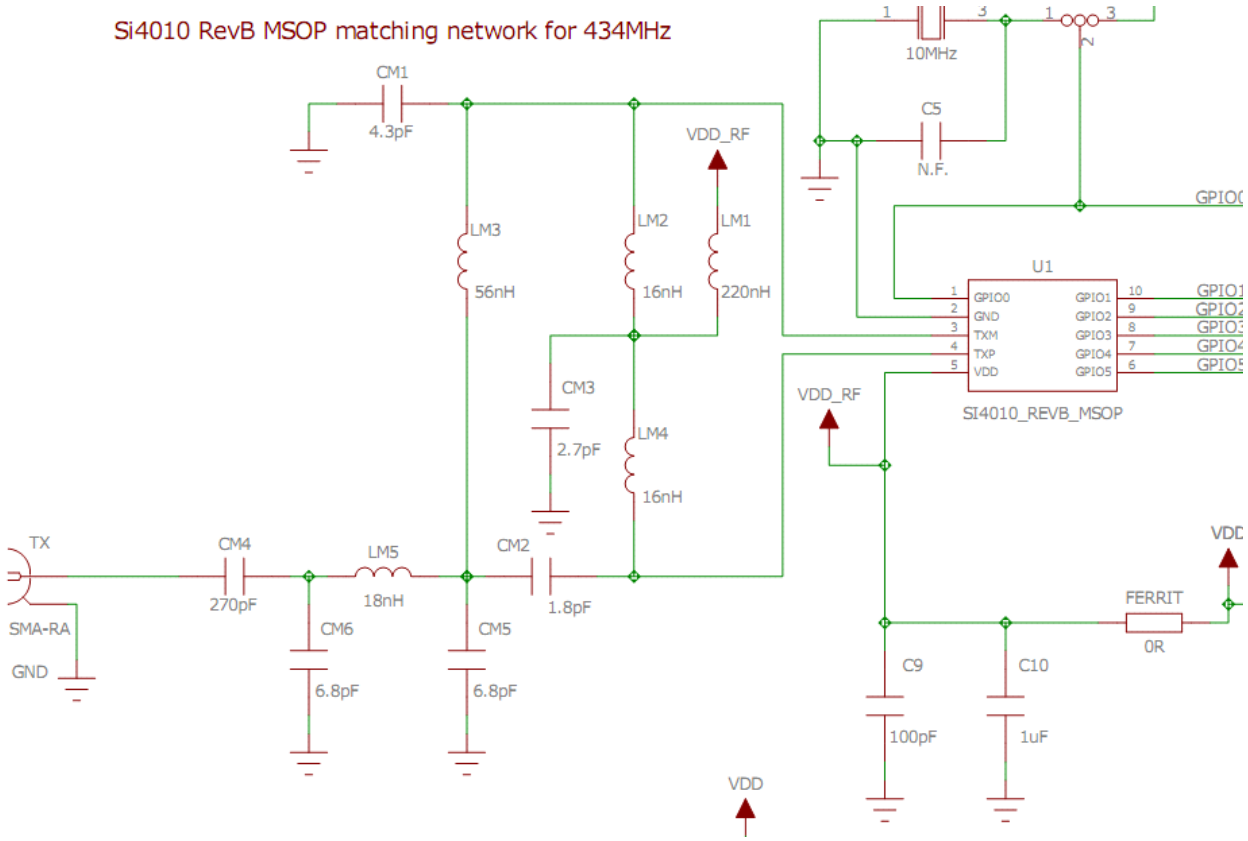


Figure 23. Si4010 MSOP Matching Network Schematic

Table 6. Matching Element Values for MSOP Packaged Si4010

MSOP	LM1	CM3	LM2	LM4	CM1	CM2	LM3	LM5	CM5	CM6	CM4
315M	220 nH	4.7 pF	20 nH	20 nH	5.6 pF	3 pF	120 nH	25 nH	8.2 pF	8.2 pF	390 pF
434M	220 nH	2.7 pF	16 nH	16 nH	4.3 pF	1.8 pF	56 nH	18 nH	6.8 pF	6.8pF	270 pF
868M	120 nH	2.4 pF	3.6 nH	3.6 nH	2.4 pF	1.2 pF	30 nH	6.8 nH	5.1 pF	5.1 pF	68 pF
915M	120 nH	2.4 pF	3.3 nH	2.7 nH	2 pF	1 pF	24 nH	6.2 nH	5.1 pF	5.1 pF	56 pF

The top layer of the Silicon Labs testcard is shown in Figure 24. It is recommended to copy and use the RF layout around the chip as it is. The gerbers of the board can be found on the Silicon Labs website.

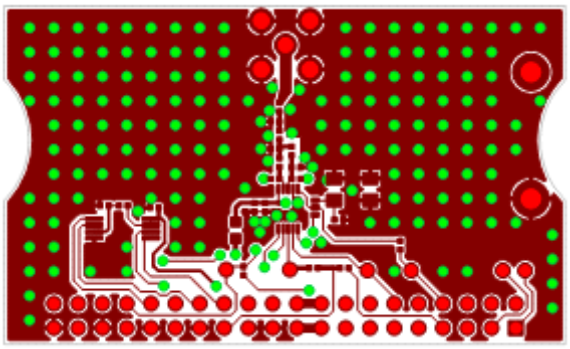


Figure 24. Top Layout of the SI Testcard with MSOP Packaged Si4010

The measured conducted spectrum of the 315, 434, 868, and 915 MHz testcard up to 3.6 GHz is shown in Figures 25, 26, 27, and 28, respectively. The realized matchings have ETSI compliance at 434 and 868 MHz and FCC compliance at 315, 434, and 915 MHz with properly reduced power in this conductive measurement. Assuming 0 dB gain antenna the compliance reserved in radiated measurements as well.

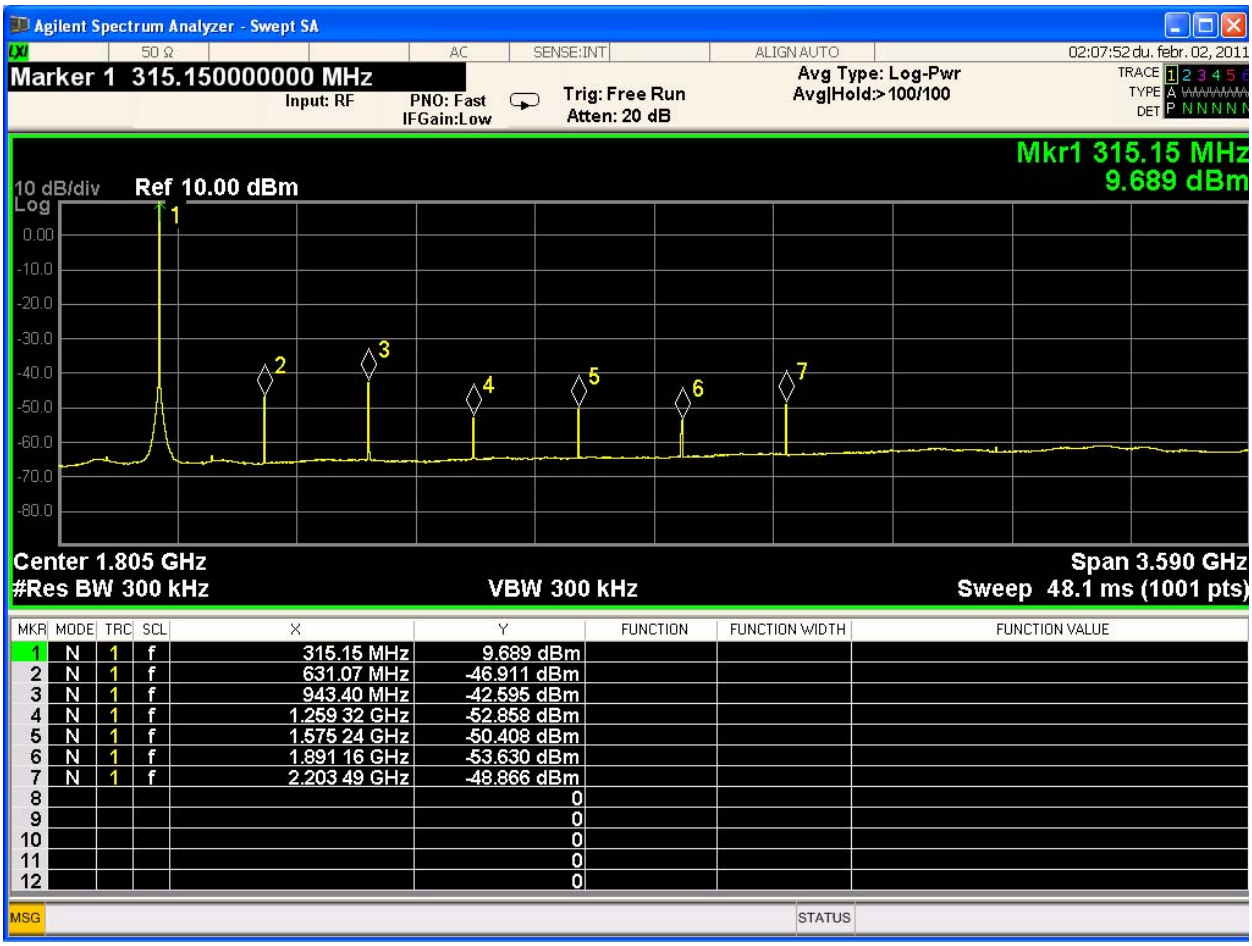
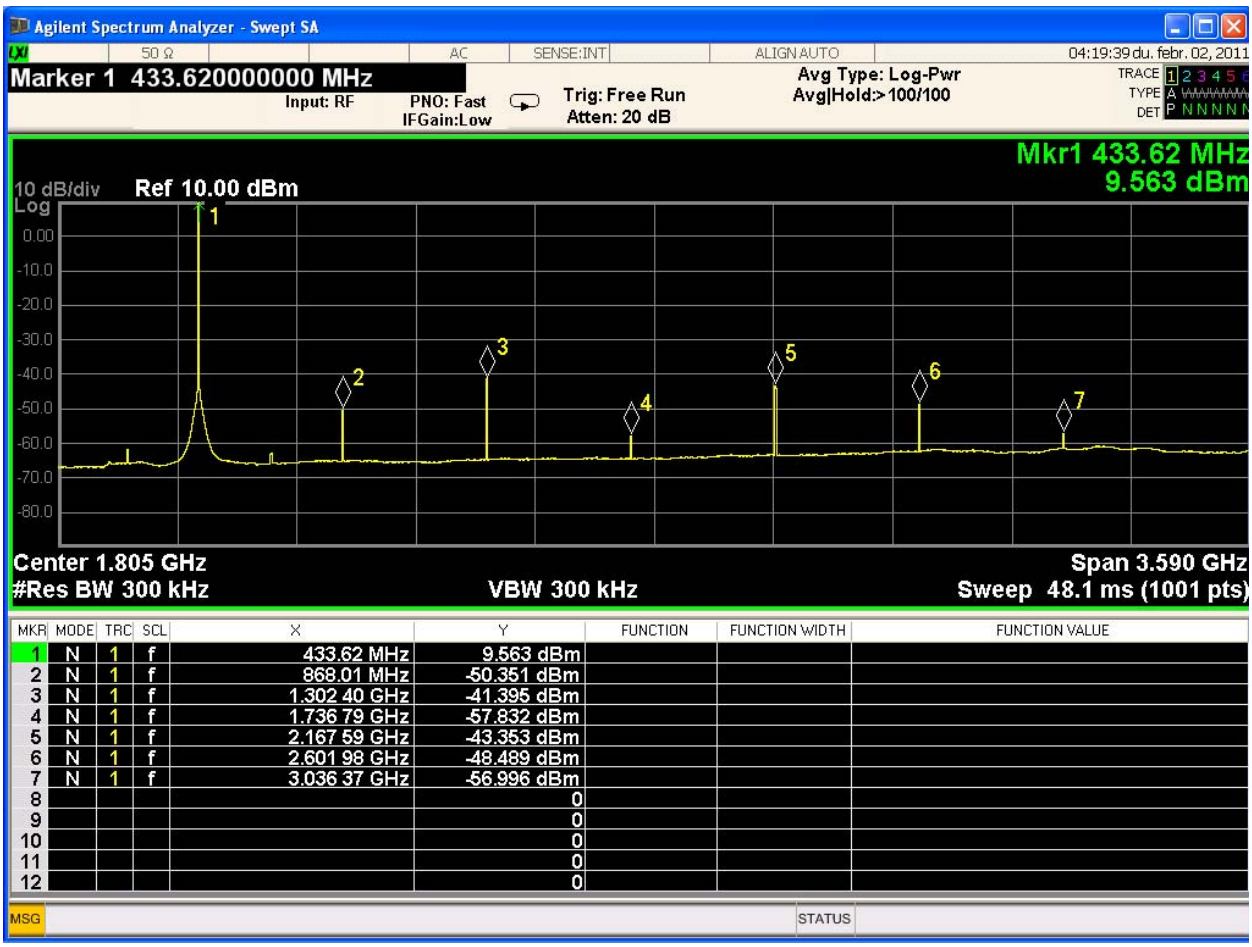


Figure 25. Measured Spectrum of the 315 MHz MSOP Card Up to 3.6 GHz



MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	433.62 MHz	9.563 dBm			
2	N	1	f	868.01 MHz	-50.351 dBm			
3	N	1	f	1.302 40 GHz	-41.395 dBm			
4	N	1	f	1.736 79 GHz	-57.832 dBm			
5	N	1	f	2.167 59 GHz	-43.353 dBm			
6	N	1	f	2.601 98 GHz	-48.489 dBm			
7	N	1	f	3.036 37 GHz	-56.996 dBm			
8					0			
9					0			
10					0			
11					0			
12					0			

Figure 26. Measured Output Spectrum of the 434 MHz MSOP Card Up to 3.6 GHz

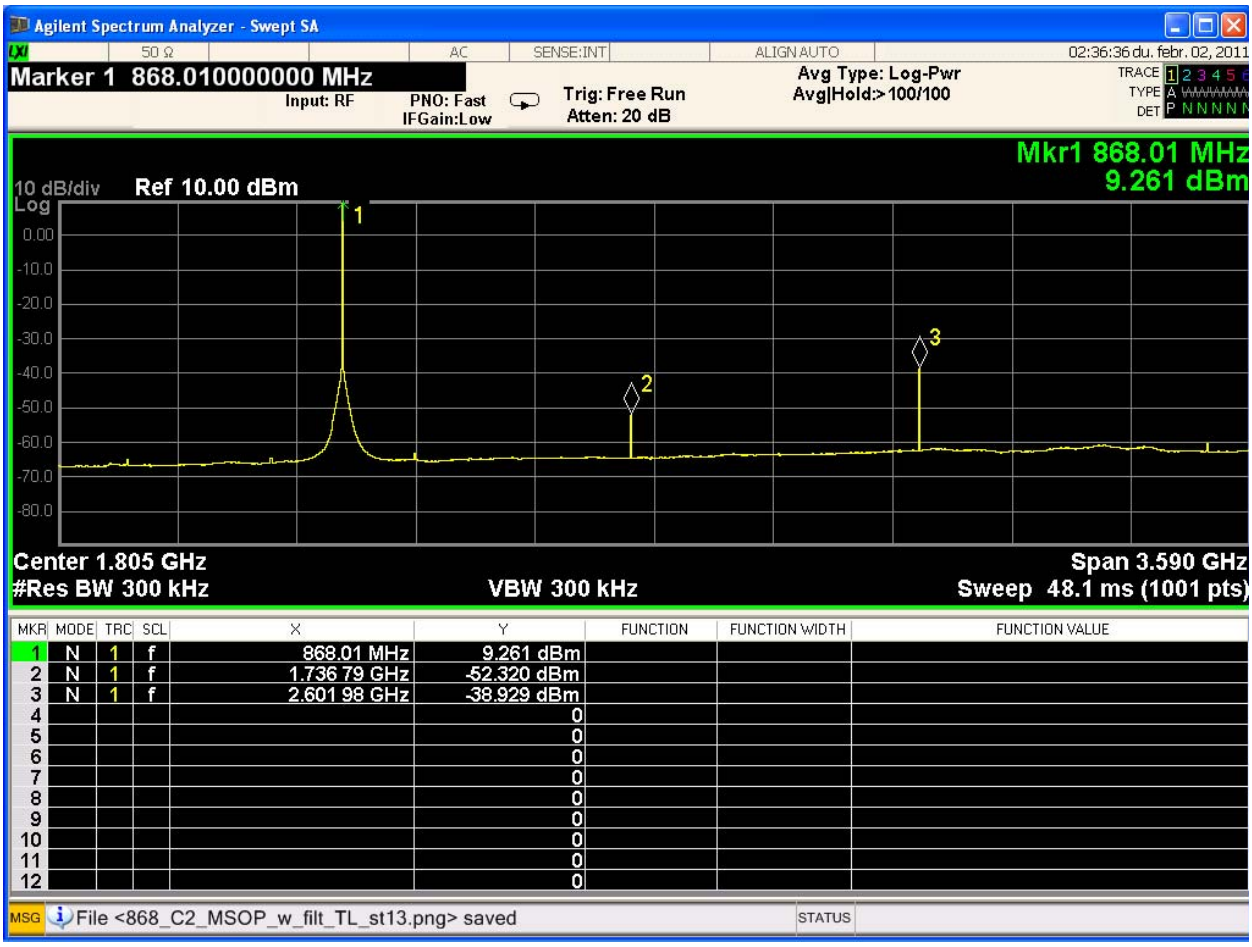


Figure 27. Measured Output Spectrum of the 868 MHz MSOP Card Up to 3.6 GHz

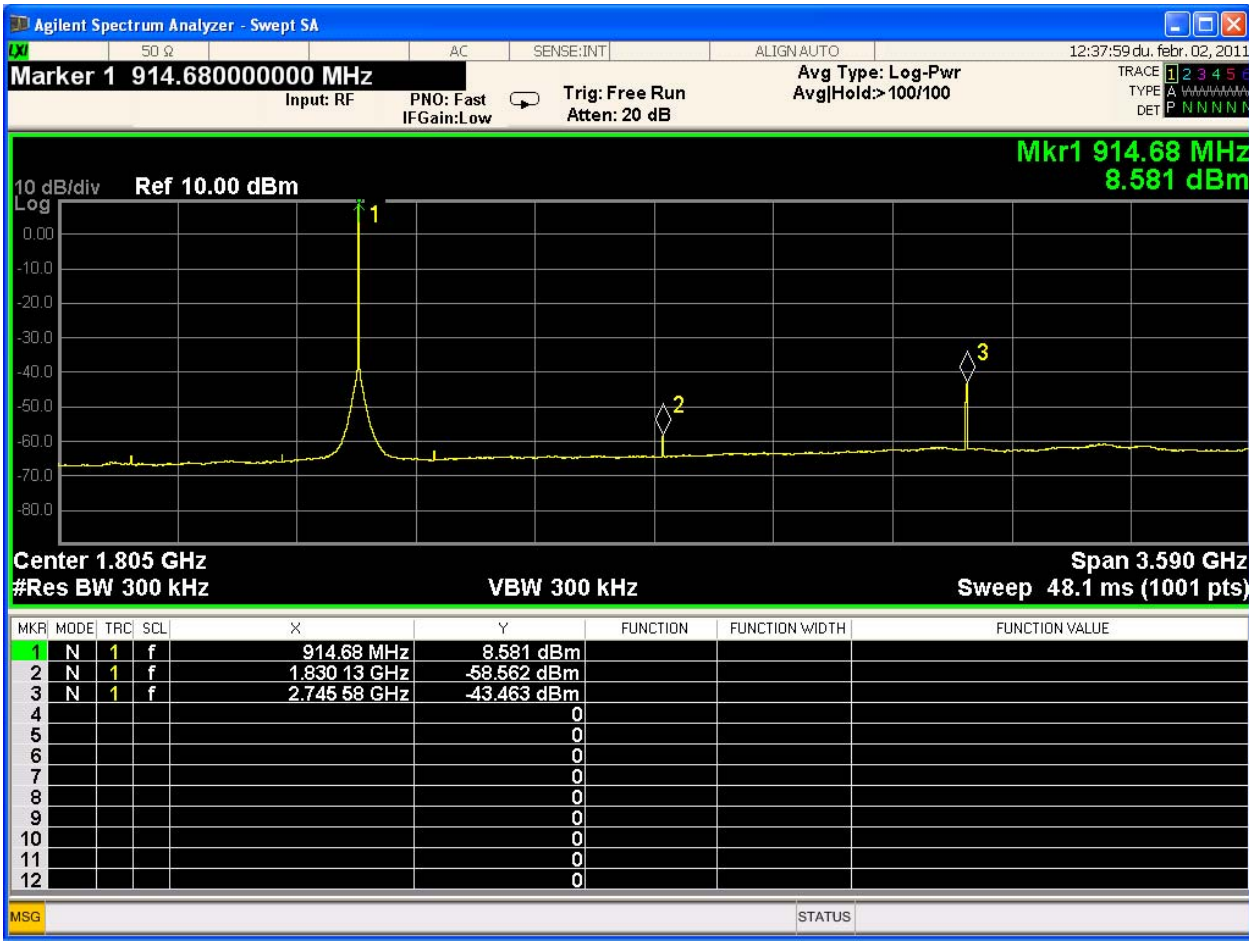


Figure 28. Measured Output Spectrum of the 915 MHz MSOP Card Up to 3.6 GHz

5. Design of High Q Discrete Matching Baluns

This section is useful for readers who intend to understand the fundamental operation of the high Q discrete matching baluns.

The designed baluns shows nearly the optimum impedances listed in Table 1 and Table 2 on page 3 for the Si4010 outputs if the single-ended port is terminated by 50 Ω.

As mentioned previously, the two main tasks the matching balun performs with minimal insertion loss are:

- Shows the optimum termination impedance (see Section “2. High Impedance Differential Power Amplifier”) to the differential output of the chip if the single-ended port of the balun is terminated by 50 Ω.
- Makes the balun function, i.e., adds the two differential outputs in-phase, with equal magnitudes.

Also it has an additional function to trap and remove the 2nd harmonic.

These functions can be satisfied with optimum solution in narrowband only. This section shows the design hints of narrowband discrete baluns.

5.1. Design Procedure

The basic structure which theoretically satisfies the two main matching balun function has four external elements as shown in Figure 29. C_TX in the figure is the same equivalent capacitance which is denoted by C_{TX} in Figure 1 on page 2.

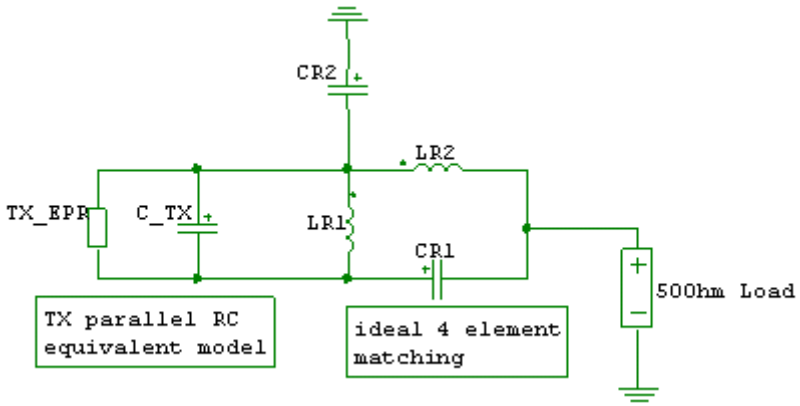


Figure 29. 4-Element Matching Circuit Schematic

In loss free, in the ideal scenario, the element values of the 4 element matching can be derived analytically. A detailed discussion of this analytical solution can be found in Silicon Labs Application Note “AN427: EZRadioPRO Si433x & Si443x RX LNA Matching.” Although that applies to the results for a high impedance Rx matching with parasitic capacitance, the method is applicable to high impedance transmitters as well. The only difference is that in the formulas the parallel equivalent resistance of the optimum termination impedance (R_{AP} in Table 1 and Table 2 in Section “2. High Impedance Differential Power Amplifier”) and the transmitter equivalent capacitance (C_TX in Figure 29, which is also given in the 6th column of Tables 1 and 2) has to be used.

As a result, the following equations are introduced here without proof or further discussion:

$$L_{R2} = \frac{\sqrt{50\Omega \times R_{PA}}}{\omega_{RF}}$$

Equation 3.

$$C_{R1} = \frac{1}{\omega_{RF}^{2} \times L_{R2}}$$

Equation 4.

$$C_{R2} = 2 \times C_{R1}$$

Equation 5.

$$L_{PA} = \frac{1}{\omega_{RF^2} \times C_{TX}}$$

Equation 6.

$$L_M = 2 \times L_{R2}$$

Equation 7.

$$L_{R1} = \frac{L_{PA} \times L_M}{L_{PA} + L_M}$$

Equation 8.

Using these equations as a starting point, the matching design methodology is the following:

1. Calculate the values e.g. for the 434 MHz MSOP case where R_{AP}=508 Ω and the CTX=2.77 pF at internal cap. bank state of 23 (Table 1 in Section “2. High Impedance Differential Power Amplifier”). The ideal matching element values are: LR1=35.9 nH, CR1=2 pF, LR2=69 nH, CR2=3.9 pF.

Note: 1.5 nH was added for the through-hole via inductance and LR1 was reduced accordingly.

2. Split LR1 into two halves to make connection for the Vdd supply choke inductor and the 2nd harmonic trap capacitor. The schematic of the matching with split LR1 (LR11 & LR12) and with choke inductor is shown in Figure 30.

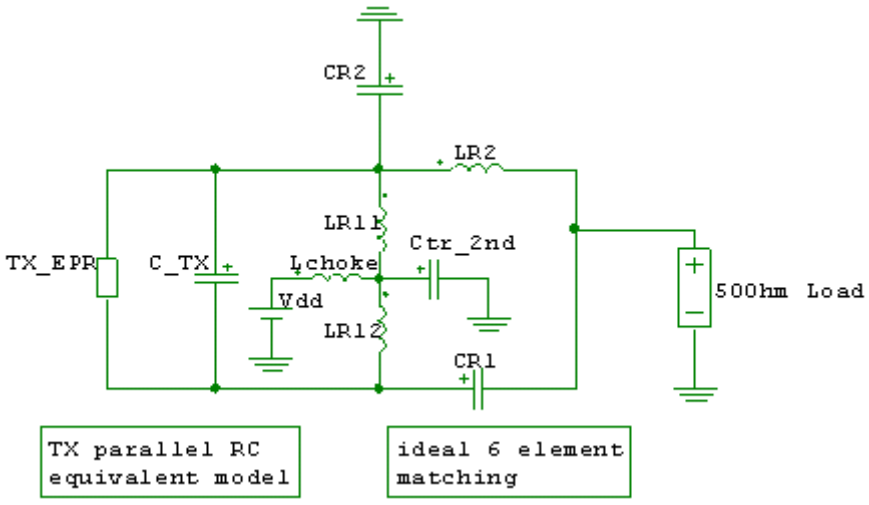


Figure 30. 6-Element Matching Circuit Schematic

The value of LCHOKE should be chosen such that it provides high impedance not only at the fundamental operating frequency but also at the first few harmonic frequencies as well. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 & 434 MHz: approximately 220–270 nH

- 868 & 915 MHz: approximately 120 nH

The value of the 2nd harmonic trap capacitor (Ctr_2nd) is chosen such that it is resonating in series with LR11 and LR12 at the 2nd harmonic frequency. As LR11 and LR12 are parallel connected for the common mode 2nd harmonic, the resulting inductance for the 2nd harmonic is LR11/2=LR12/2=LR1/4. This has to be in resonance with Ctr_2nd at the 2nd harmonic. However, the exact values are strongly influenced by the parasitic and thus it is always tuned at the bench.

3. The parasitics and losses of the SMD components and the pcb are included into a simulation where the above-listed main balun functions can be checked. Going back to the 434 MHz MSOP example, Figures 31 and 32 show the simulated S11 and the balun function (voltage transfer function from the 50 Ω single-ended port to the two differential ports) when the R_{AP} and C_{TX} (Table 1) is used as a differential port termination). As one can see if the differential port of the balun is terminated by the conjugate of the optimum termination impedance (i.e., with the parallel connected RAP and CTX), both its balun function and matching are very good.
4. The balun function is checked when the R_{AP} is replaced by the much higher EPR, i.e., the internal loss of the TX (TX_EPR). That is shown in Figure 33 assuming 20K EPR at cap. bank state 23. The balun function remained good, only the voltage magnitude increased in the same way at both differential nodes. The S11 becomes bad (Figure 34), but this is normal as described in Section “2. High Impedance Differential Power Amplifier”, in "voltage limited" mode when complex conjugate matching is not used for achieving the maximum power.

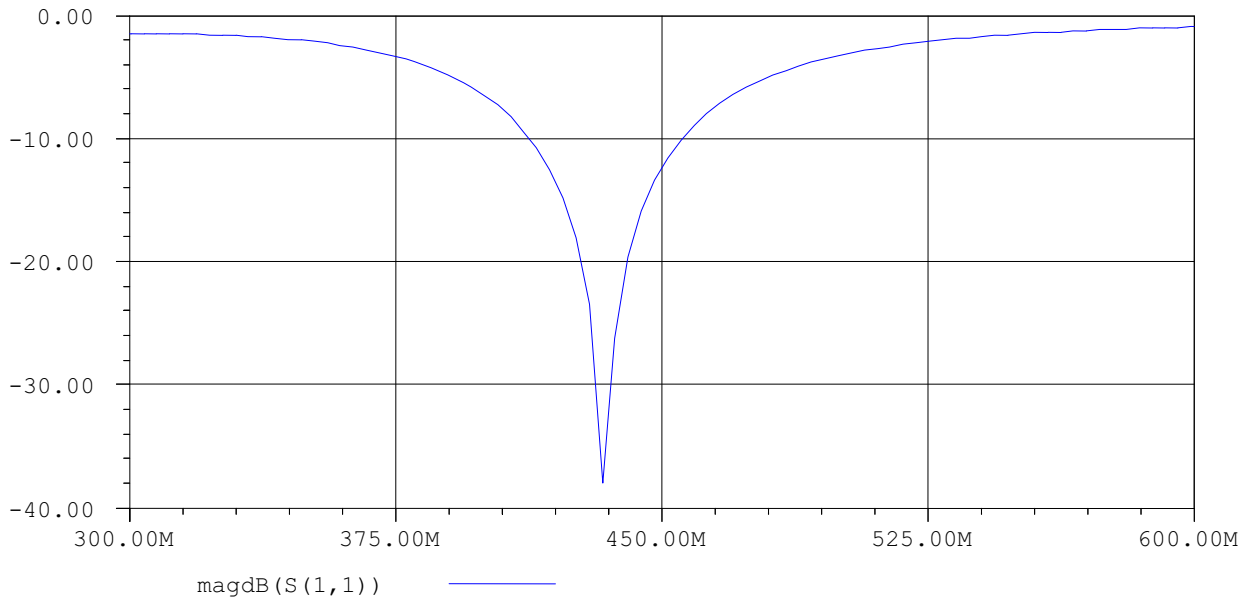


Figure 31. Simulated S11 of the MSOP Example

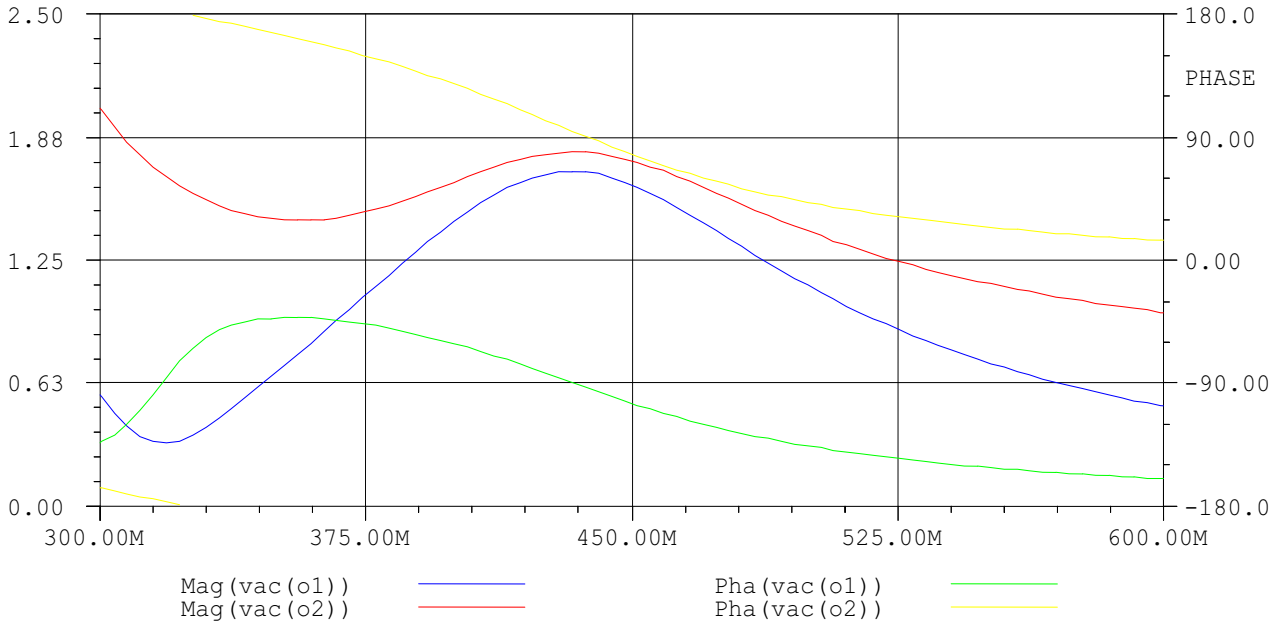


Figure 32. Voltage Transfer Function

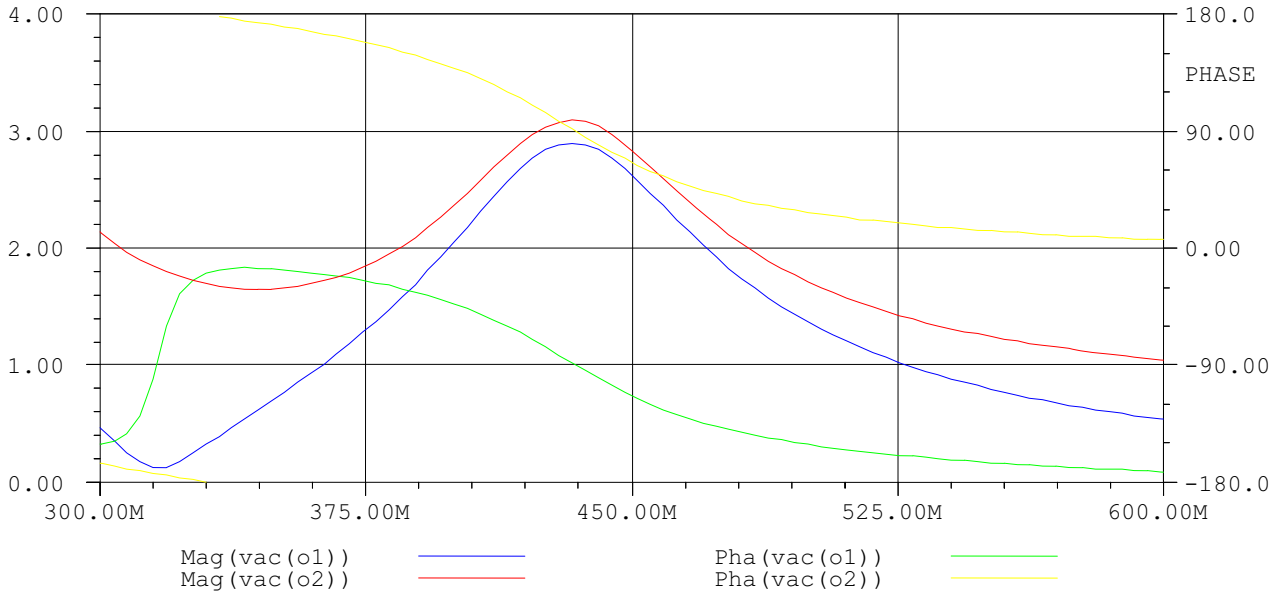


Figure 33. Voltage Transfer Function with Higher EPR

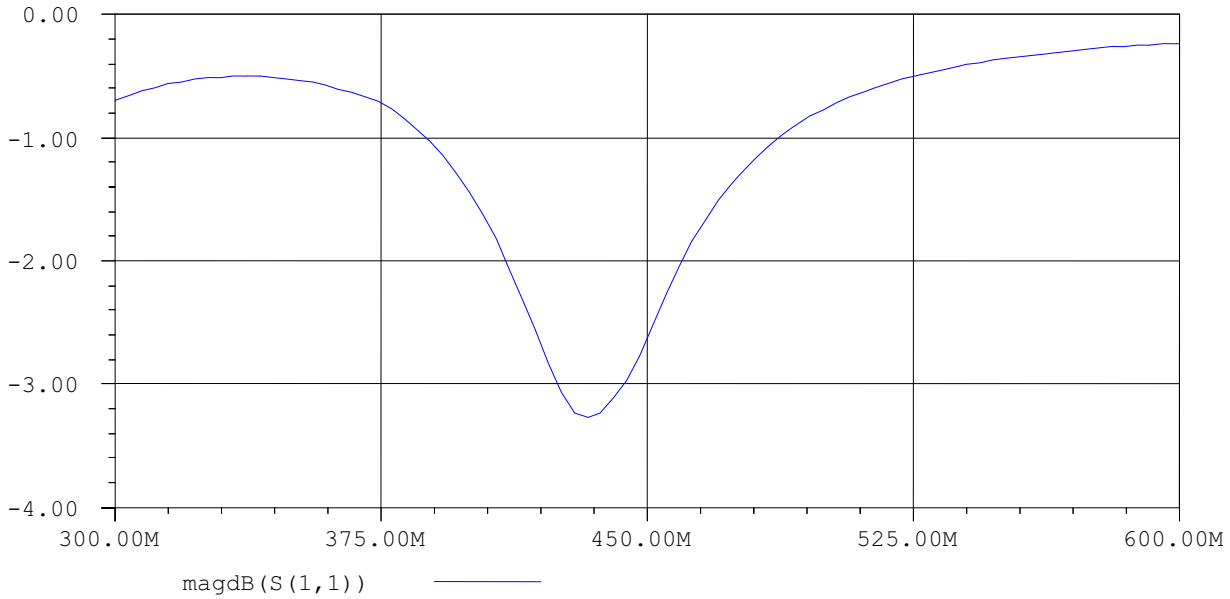


Figure 34. S11 with Higher EPR

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