DLD Lab Final

CSE 2106

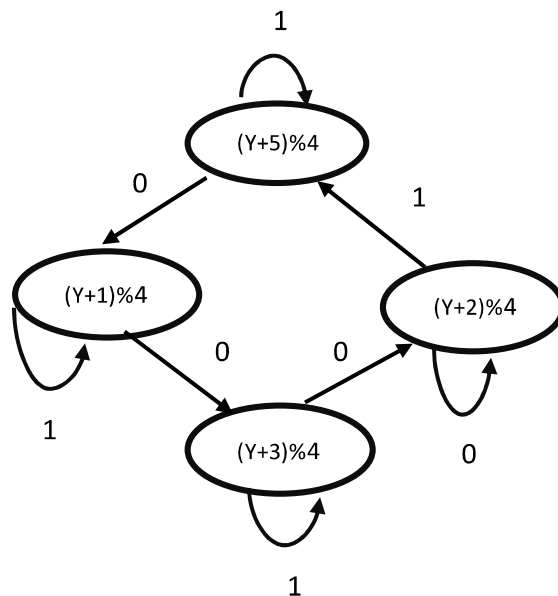Marks: 20   Duration: 1 Hour 15 Minutes

Q1. *[10 Marks]*

Following is a State Diagram. Design the state diagram using **JK** Flip-Flops.

[Here Y = Last digit of your ID]

i.e.: If your ID is 14.02.04.066 then (Y+1) % 4 = 7%4 = 3

Q2. *[5 Marks]*

Design a **4-bit** Johnson Counter. The type of Johnson Counter (Up/Down) and type of Flip-Flop depends on your ID.

- Johnson Up counter using T Flip-Flop if *[Last digit of your ID] % 4 =0*
- Johnson Up counter using D Flip-Flop if *[Last digit of your ID] % 4 =1*
- Johnson Down counter using T Flip-Flop if *[Last digit of your ID] % 4 =2*
- Johnson Down counter using D Flip-Flop if *[Last digit of your ID] % 4 =3*

i.e.: If your ID is 14.02.04.066 then (6%4) = 2 (You need to implement Johnson Down counter using T Flip-Flop)

Q3. *[2.5 + 2.5 = 5 Marks]*

F(A,B,C,D) = M12 . M13 . M15. M(x). M(x+1) .M(x-1). M(x-2)

Implement the aforementioned expression using **DEMUX** and **MUX**.

Show all the necessary steps and draw the circuit diagram.

Here x = [last digit of your ID % 9] + 2

i.e.: If your ID is 14.02.04.066 then (x+1) % 4 = 7%4 = 3

For Question **1 & 2**, you need to Design the following:

- State Diagram
- State Table
- Excitation Table
- K-Map
- Expression
- Circuit