HW 3,

2. (1)

I represents Issue, R represents Read operands. E represents Execution, W represents Write Result

Instruction \ CC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		60	61	62	CC
(1) L.D F6, 34(R2)	I	R	E	W																								4
(1) L.D F2, 45(R3)					I	R	E	W																				4
(10) MUL.D F0, F2, F4						I			R										E	W				...				15
(2) SUB.D F8, F2, F6							I		R		E	W																6
(40) DIV.D F10, F0, F6								I													R					E	W	45
(2) ADD.D F6, F8, F2													I	R		E						W						10

Issue: be stalled until instructions intending to write to the same register are completed (avoid WAW)
Read operands: wait until all operands become available (avoid RAW)
Execution: start after R
Write Result: be delayed until earlier instructions — which intend to read registers this instruction wants to write to — have completed their read operands stage (avoid WAR)

so L.D F6, 34(R2) takes 4 clock cycles,
L.D F2, 45(R3) takes 4 clock cycles,
MUL.D F0, F2, F4 takes 15 clock cycles
SUB.D F8, F2, F6 takes 6 clock cycles
DIV.D F10, F0, F6 takes 45 clock cycles
ADD.D F6, F8, F2 takes 10 clock cycles

(2)

I represents Issue, E represents Execute, W represents Write Result

Instruction \ CC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		52	53	54	CC
(1) L.D F6, 34(R2)	I	E	W																			3
(1) L.D F2, 45(R3)		I	E	W																		3
(10) MUL.D F0, F2, F4			I	E										W				...				12
(2) SUB.D F8, F2, F6				I	E		W															4
(40) DIV.D F10, F0, F6					I									E							W	
(2) ADD.D F6 F8, F2						I	E		W													4

Issue: be issued if all operands and reservation stations are ready or else they are all. Registers are renamed. (avoid WAR and WAW)
Execute: be delayed in this step until all of their operands are available
Write result: start after E

so L.D F6, 34(R2) takes 3 clock cycles,
L.D F2, 45(R3) takes 3 clock cycles,
MUL.D F0, F2, F4 takes 12 clock cycles
SUB.D F8, F2, F6 takes 4 clock cycles
DIV.D F10, F0, F6 takes 50 clock cycles
ADD.D F6, F8, F2 takes 4 clock cycles