第 6 章 时序逻辑电路

Sequential Logic Circuits

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§ 6.1 概述 Introduction

时序电路

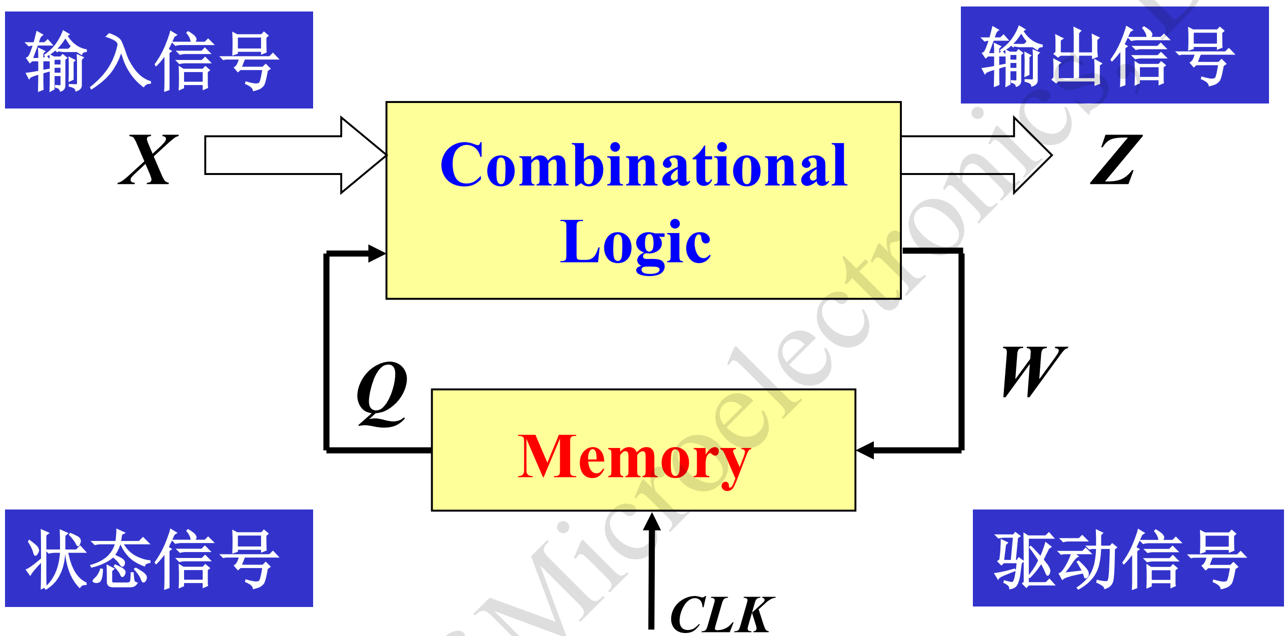
输出 { 输入 / 以前状态 记忆

基本单元: FF (逻辑门 + 反馈线)

逻辑电路 { 同步 所有的触发器在*CLK* 同一边沿触发 / 异步

时序电路结构:

组合电路 + 记忆元件

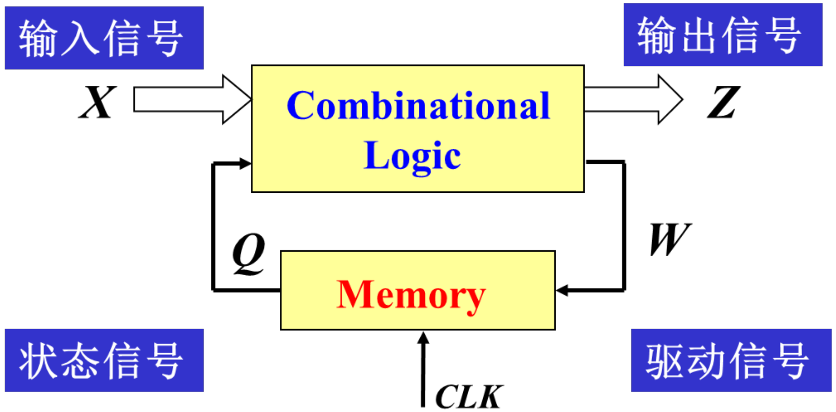


X：外输入

Z：外输出

W: 控制输入 — J, K, D, T

Q: 触发器输出（状态）



外输入 X 控制输入 W

外输出 Z 状态 Q

关系:

- 输出方程 $Z = F(X, Q)$
- 驱动方程 $W = H(X, Q)$
- 特征方程 $Q^{n+1} = G(W, Q^n)$

按照电路中输出变量是否和输入变量直接相关

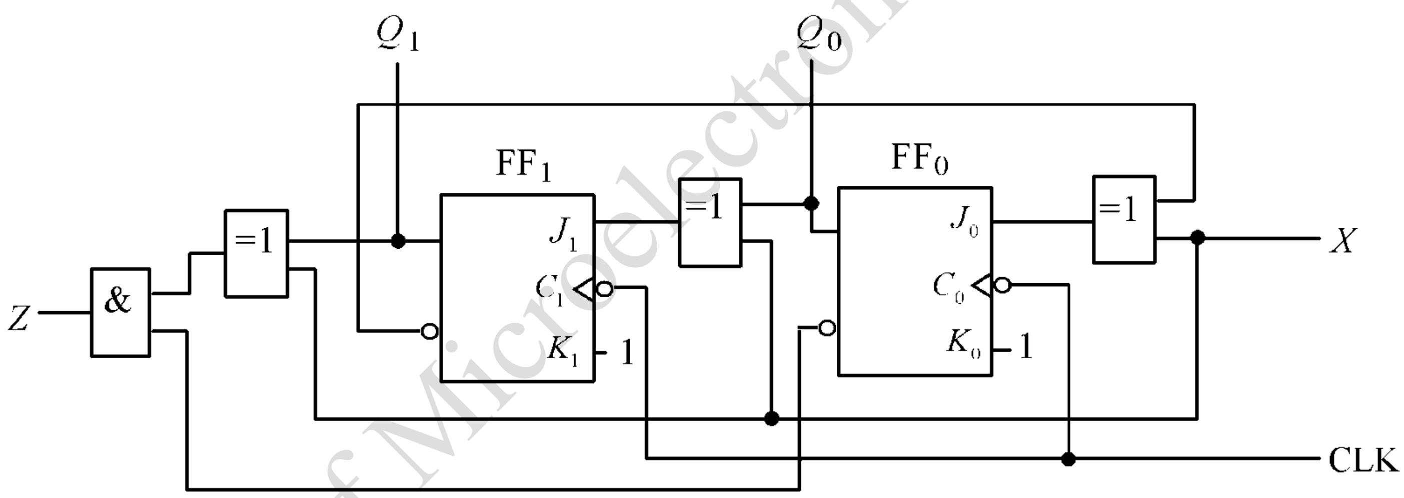
时序电路

- 米里型 (Mealy) 输出 Z $\begin{cases} Q^n \\ X \end{cases}$
- 莫尔型 (Moore) 输出 $Z \sim Q^n$

§6.2 同步时序电路分析
Sequential Logic Circuits Analysis

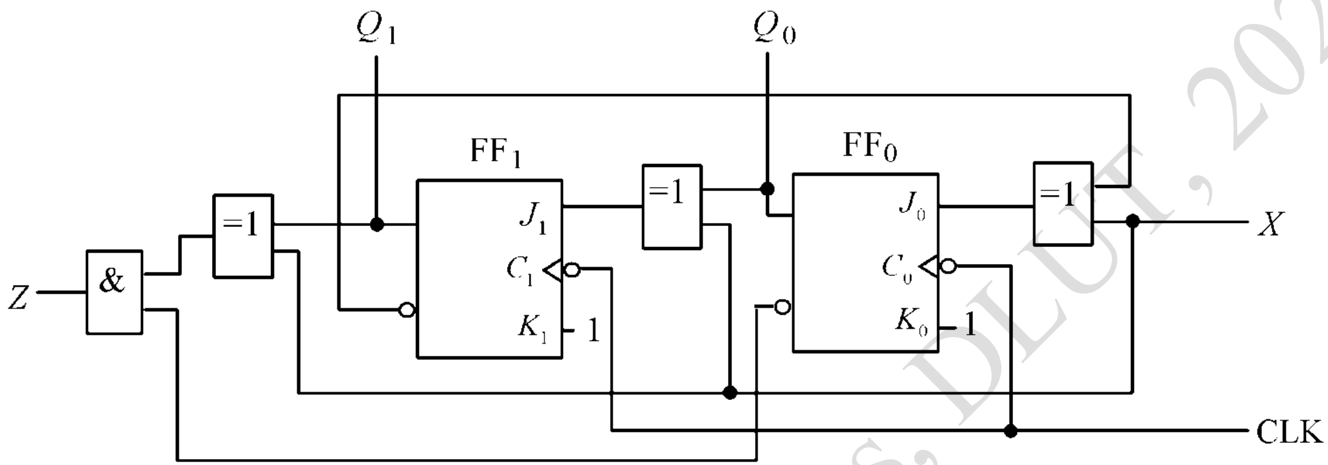
分析: 已知电路, 描述电路原理及功能

例1: 分析下图时序逻辑电路



1) 输入 X 　　控制输入 J_0, K_0, J_1, K_1

输出 Z 　　状态 Q_1 (MSB), Q_0



2) 方程

输出方程 $Z=(X\oplus Q_1^n)\cdot\overline{Q_0^n}$

驱动方程 $\begin{cases} J_0 = X\oplus\overline{Q_1^n} \\ K_0 = 1 \end{cases}$ $\begin{cases} J_1 = X\oplus Q_0^n \\ K_1 = 1 \end{cases}$

特征方程 $\begin{cases} Q_0^{n+1} = J_0\overline{Q_0^n}+\overline{K_0}Q_0^n = (X\oplus\overline{Q_1^n})\cdot\overline{Q_0^n} \\ Q_1^{n+1} = J_1\overline{Q_1^n}+\overline{K_1}Q_1^n = (X\oplus Q_0^n)\cdot\overline{Q_1^n} \end{cases}$

3）状态表和状态图

已知：输入 X，Q^n

求：输出 Z，Q^{n+1}

$$Q_1^{n+1} = (X \oplus Q_0^n)\cdot\overline{Q_1^n}$$

$$Q_0^{n+1} = (X \oplus \overline{Q_1^n})\overline{Q_0^n}$$

$$Z = (X \oplus Q_1^n)\cdot\overline{Q_0^n}$$

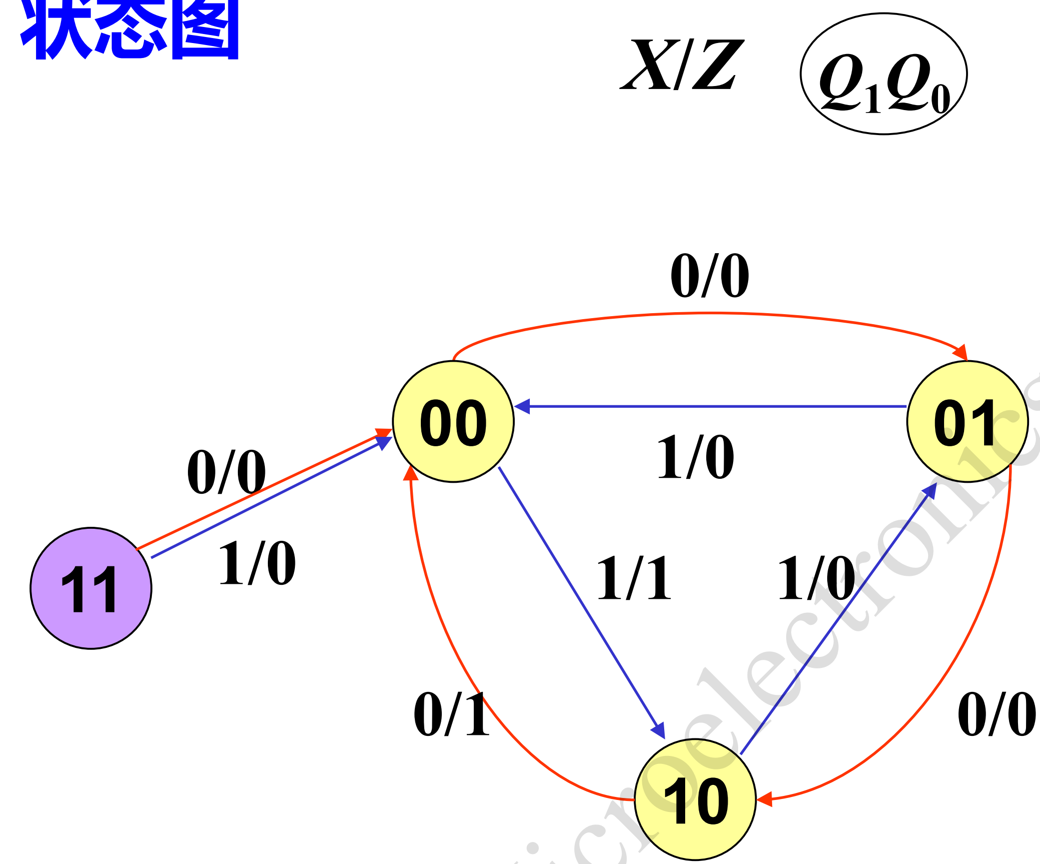
状态表

	X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Z
X=0	0	0	0	0	1	0
	0	0	1	1	0	0
	0	1	0	0	0	1
	0	1	1	0	0	0
X=1	1	0	0	1	0	1
	1	0	1	0	0	0
	1	1	0	0	1	0
	1	1	1	0	0	0

$$X=0\begin{cases} Q_1^{n+1} = Q_0^n\cdot\overline{Q}{}_1^n \\ Q_0^{n+1} = \overline{Q_1^n}\cdot\overline{Q_0^n} = \overline{Q_1^n+Q_0^n} \\ Z = Q_1^n\cdot\overline{Q_0^n} \end{cases}$$

$$X=1\begin{cases} Q_1^{n+1} = \overline{Q_0^n}\cdot\overline{Q_1^n} \\ Q_0^{n+1} = Q_1^n\cdot\overline{Q_0^n} \\ Z = \overline{Q_1^n}\cdot\overline{Q_0^n} \end{cases}$$

状态图



状态表

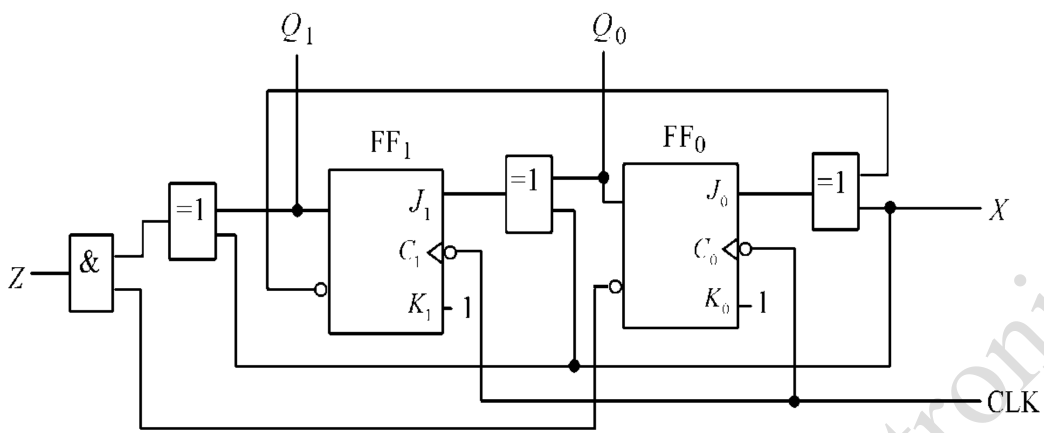
X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Z
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	0	1	0
1	1	1	0	0	0

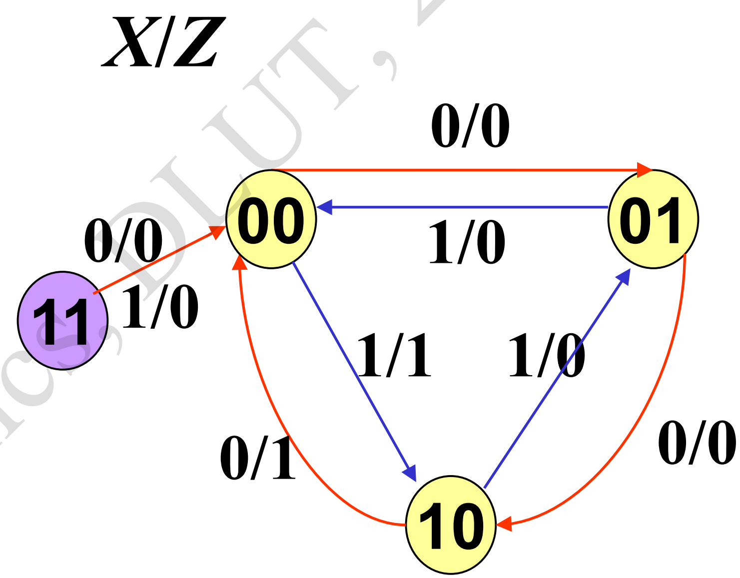
⟶ 对应一个CLK

输出Z是原状态下的输出

每条转换线对应真值表的一行

4) 电路功能



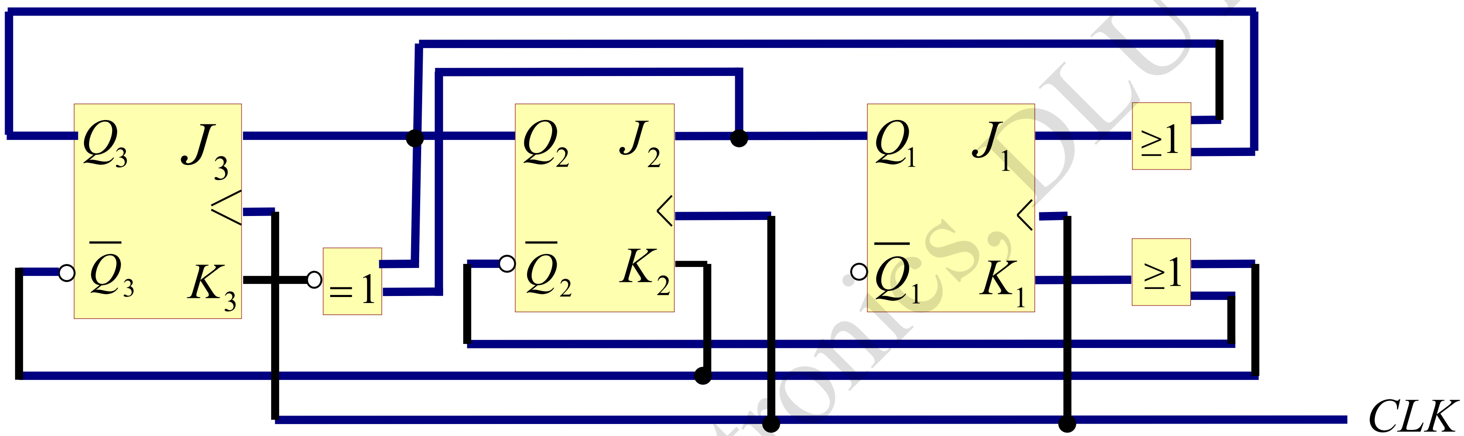


X=0, M-3 加法计数：$Z=1$，进位输出；

X=1, M-3 减法计数：$Z=1$，借位输出。

状态图主循环：模 3 加减双向计数器

例 2. 分析下图时序电路



无外输入，无外输出

$$\begin{cases} J_3 = Q_2^n \\ K_3 = \overline{Q_2^n \oplus Q_1^n} \end{cases} \quad \begin{cases} J_2 = Q_1^n \\ K_2 = \overline{Q}_3^n \end{cases} \quad \begin{cases} J_1 = Q_2^n + Q_3^n \\ K_1 = \overline{Q}_2^n + \overline{Q}_3^n = \overline{Q_2^n Q_3^n} \end{cases}$$

$$Q_3^{n+1} = J_3\overline{Q_3^n} + \overline{K}_3 Q_3^n = Q_2^n\overline{Q_3^n} + (Q_2^n \oplus Q_1^n)Q_3^n$$

$$Q_2^{n+1} = J_2\overline{Q_2^n} + \overline{K}_2 Q_2^n = Q_1^n\overline{Q_2^n} + Q_3^n Q_2^n$$

$$Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K}_1 Q_1^n = (Q_2^n + Q_3^n)\overline{Q_1^n} + Q_2^n Q_3^n Q_1^n$$

Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

$$Q_3^{n+1} \begin{cases} Q_2^n & Q_3^n = 0, \\ Q_2^n \oplus Q_1^n & Q_3^n = 1, \end{cases}$$

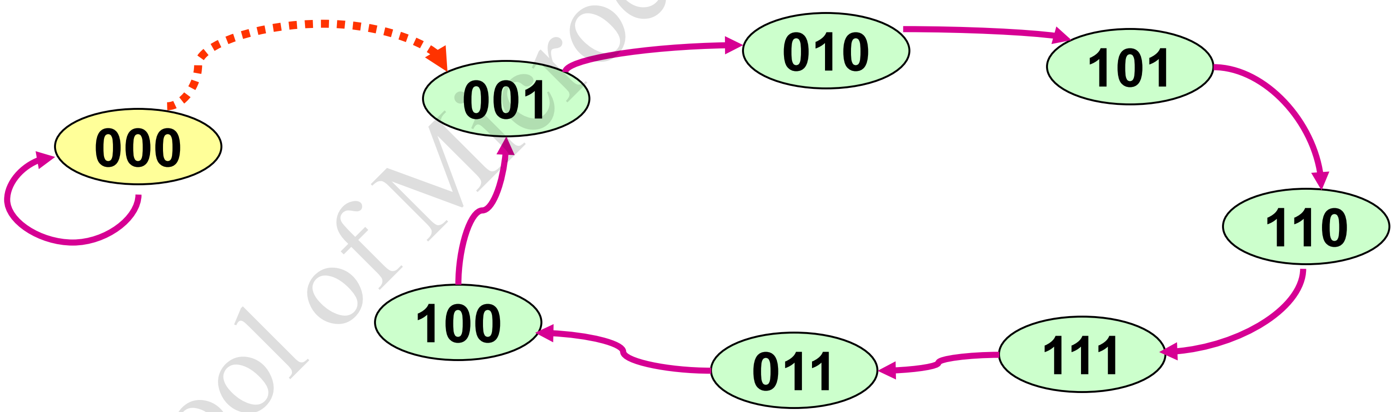
$$Q_2^{n+1} \begin{cases} Q_1^n & Q_2^n = 0, \\ Q_3^n & Q_2^n = 1, \end{cases}$$

$$Q_1^{n+1} \begin{cases} Q_2^n + Q_3^n & Q_1^n = 0, \\ Q_2^n Q_3^n & Q_1^n = 1, \end{cases}$$

Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

000 **孤立状态**

自启动



§6.3 同步时序电路设计

Synchronous Sequential Circuit Design

已知 → 功能或状态图

求 → 电路

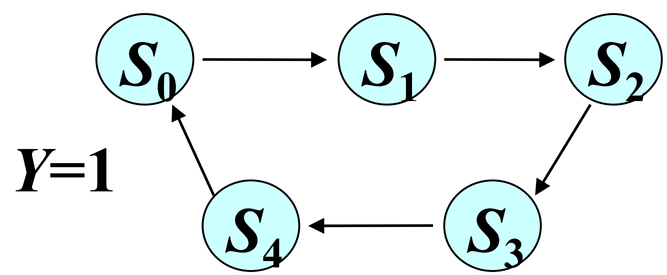
设计要求 →（1）→ 原始状态图 →（2）化简 → 最简状态图 →（3）→ 状态分配 →（4）→ 选触发器，求输出、状态、驱动方程 →（5）→ 画电路图 →（6）→ 检查电路能否自启动

例 1. 设计同步5进制加法计数器

1) 确定状态及状态图

M-5 计数器，5 个状态：S_0, S_1, S_2, S_3, S_4

在计数脉冲CLK作用下，5 个状态周期性变换, 在 S_4 状态下进位输出 $Y=1$



2) 状态化简

M-5, 5 个状态， 不须再化简

3) 状态分配、编码

$2^{n-1} \le$ 状态数 $\le 2^{n}$　　　n：二进制位数　3位

$S_0 \rightarrow 000$

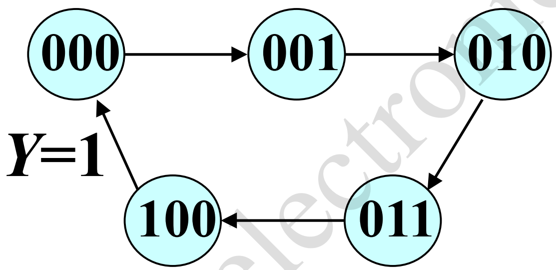
$S_1 \rightarrow 001$

$S_2 \rightarrow 010$

$S_3 \rightarrow 011$

$S_4 \rightarrow 100$

状态图



状态表

$Q_2^n\ Q_1^n\ Q_0^n$	$Q_2^{n+1}\ Q_1^{n+1}\ Q_0^{n+1}$	Y
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1

4) 选择 FF，确定驱动方程、状态方程Q^{n+1}及输出方程

方法 1：先不确定用哪种触发器

由状态表填卡诺图

状态表

Q_2^n Q_1^n Q_0^n	Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}	Y
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1

Q_2^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	0
1	0	1	Φ	Φ

Q_1^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	1	Φ	0
1	1	0	Φ	Φ

Q_0^{n+1}

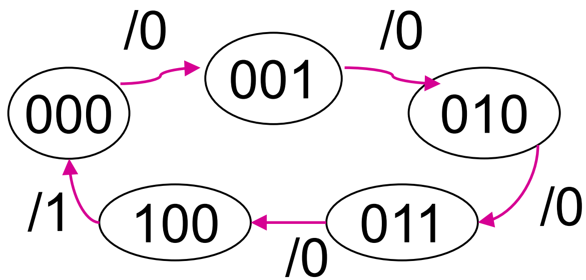
Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	1	1	Φ	0
1	0	0	Φ	Φ

Y

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	1
1	0	0	Φ	Φ

也可直接填卡诺图

直接填卡诺图



5个 有效状态 **3位二进制数** **3 个FF**

$$Q_2^nQ_1^nQ_0^n \xrightarrow{/Z} Q_2^{n+1}Q_1^{n+1}Q_0^{n+1}$$

Y

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	1
1	0	0	Φ	Φ

Q_2^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	0
1	0	1	Φ	Φ

Q_1^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	1	Φ	0
1	1	0	Φ	Φ

Q_0^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	1	1	Φ	0
1	0	0	Φ	Φ

Q_2^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	0
1	0	1	Φ	Φ

Q_1^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	1	Φ	0
1	1	0	Φ	Φ

Q_0^{n+1}

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	1	1	Φ	0
1	0	0	Φ	Φ

$$Q_2^{n+1} = Q_1^nQ_0^n = D_2$$

$$D_2 = Q_1^nQ_0^n$$

$$Q_1^{n+1} = Q_0^n\bar{Q}_1^n + \bar{Q}_0^nQ_1^n = Q_0^n \oplus Q_1^n = T_1 \oplus Q_1^n$$

$$T_1 = Q_0^n$$

$$Q_0^{n+1} = \bar{Q}_2^n\bar{Q}_0^n = D_0$$

或

$$\begin{cases} J_0 = \bar{Q}_2^n \\ K_0 = 1 \end{cases}$$

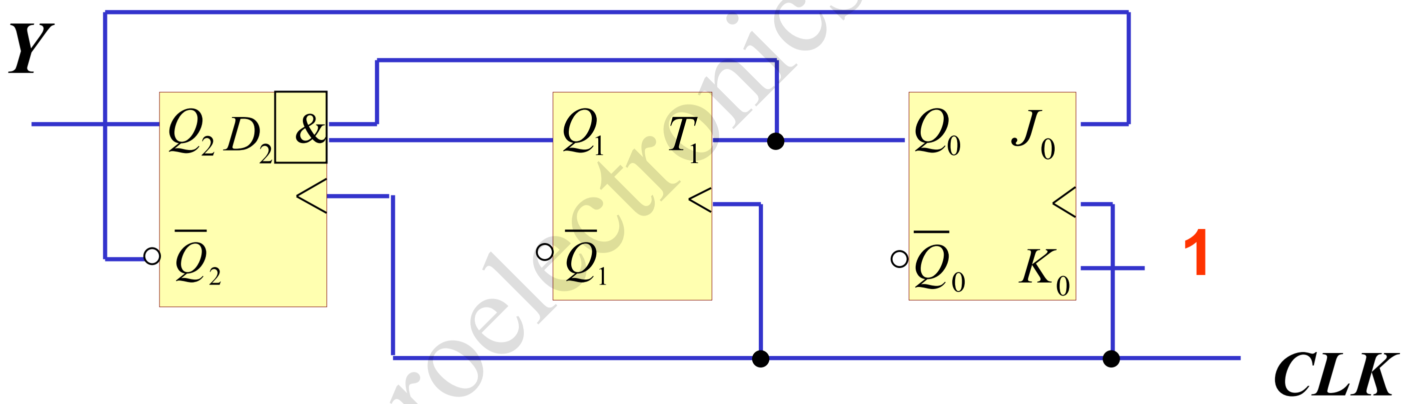
Y

Q_0^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	Φ	1
1	0	0	Φ	Φ

$$Y = Q_2^n$$

$D_2 = Q_1^n Q_0^n$　　$T_1 = Q_0^n$　　$\begin{cases} J_0 = \overline{Q_2}^n \\ K_0 = 1 \end{cases}$　　$Y = Q_2^n$

5）电路



与门可以省略

6)检查是否可以自启动

$$Q_2^{n+1} = Q_1^n Q_0^n$$

$$Q_1^{n+1} = Q_0^n \overline{Q}_1^n + \overline{Q}_0^n Q_1^n$$

$$= Q_0^n \oplus Q_1^n$$

$$Q_0^{n+1} = \overline{Q}_2^n \overline{Q}_0^n$$

状态表

$Q_2^n\ Q_1^n\ Q_0^n$	$Q_2^{n+1}\ Q_1^{n+1}\ Q_0^{n+1}$	Y
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1
1 0 1	0 1 0	1
1 1 0	0 1 0	1
1 1 1	1 0 0	1

方法 2: 确定用哪种触发器

4) 选择 FF　　选 JK-FFs

5) 状态方程Q^{n+1}及控制输入– J, K

状态表

$Q_2^n Q_1^n Q_0^n$	$Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Y
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1

JK-FF 激励表

$Q^n \rightarrow Q^{n+1}$	$J\ K$
0 0	0 ×
0 1	1 ×
1 0	× 1
1 1	× 0

Q_2^n	$\Rightarrow$ Q_2^{n+1}	J_2
0	0	0
0	0	0
0	0	0
0	1	1
1	0	X
X	X	X
X	X	X
X	X	X

得到 2#-FF 控制输入 J_2 驱动卡诺图

J_2 Q_2^n \ $Q_1^n Q_0^n$	00	01	11	10
0	0	0	1	0
1	×	×	×	×

状态图

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

JK-FF 激励表

$Q^n \rightarrow Q^{n+1}$		J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Q_1^n	$\Rightarrow$ Q_1^{n+1}	K_1
0	0	X
0	1	X
1	1	0
1	0	1
0	0	X
X	X	X
X	X	X
X	X	X

得到 1#-FF 控制输入 K_1 驱动卡诺图

K_1 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	×	×	1	0
1	×	×	×	×

得到各个触发器控制输入驱动卡诺图及控制输入

J_2 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	0	0	1	0
1	×	×	×	×

$$J_2 = Q_1^n Q_0^n$$

J_1 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	0	1	×	×
1	0	×	×	×

$$J_1 = Q_0^n$$

J_0 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	1	×	×	1
1	0	×	×	×

$$J_0 = \overline{Q_2^n}$$

K_2 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	X	X	X	X
1	1	X	X	X

$$K_2 = 1$$

K_1 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	×	×	1	0
1	×	×	×	×

$$K_1 = Q_0^n$$

K_0 Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	×	1	1	×
1	×	×	×	×

$$K_0 = 1$$

输出卡诺图

Y Q_2^n \ $Q_1^nQ_0^n$	00	01	11	10
0	0	0	0	0
1	1	×	×	×

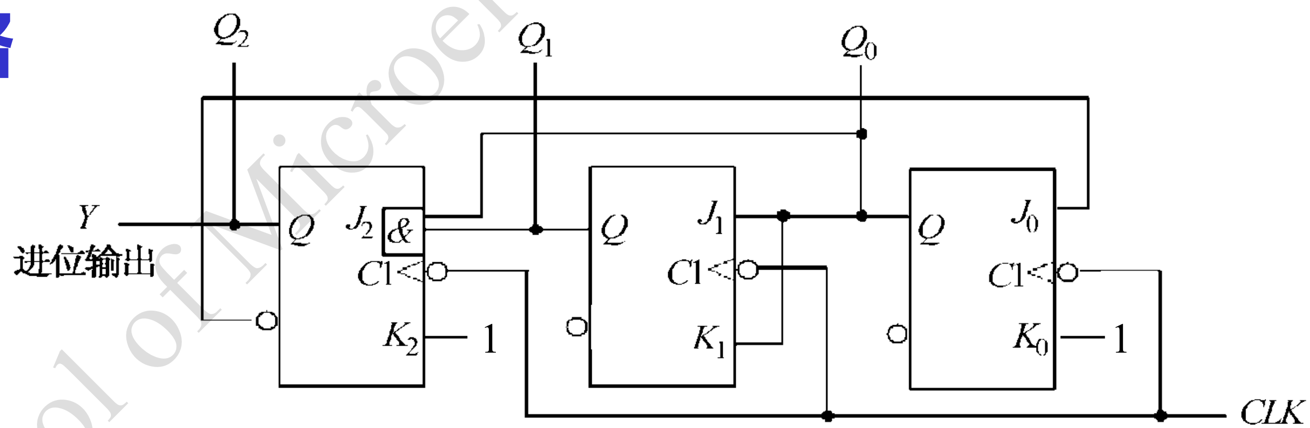
状态表

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

$$Y = Q_2^n$$

$$\begin{cases} J_2 = Q_1^n Q_0^n \\ K_2 = 1 \end{cases} \quad \begin{cases} J_1 = Q_0^n \\ K_1 = Q_0^n \end{cases} \quad \begin{cases} J_0 = \overline{Q_2^n} \\ K_0 = 1 \end{cases}$$

6) 电路



7)检查是否可以自启动

例 2. 设计一个串行数据检测器。该检测器有一个输入端X。电路的功能是对输入信号进行检测。当连续输入三个1（以及三个以上1）时，该电路输出$Y = 1$，否则输出$Y = 0$。

1）根据设计要求，设定状态

S_0—初始状态或没有收到1时的状态；

S_1—收到一个1后的状态；

S_2—连续收到两个1后的状态；

S_3—连续收到三个1（以及三个以上1）后的状态。

X=1，收到一个“1”

2）画出状态转换图

S_0—初始状态或没有收到1时的状态；

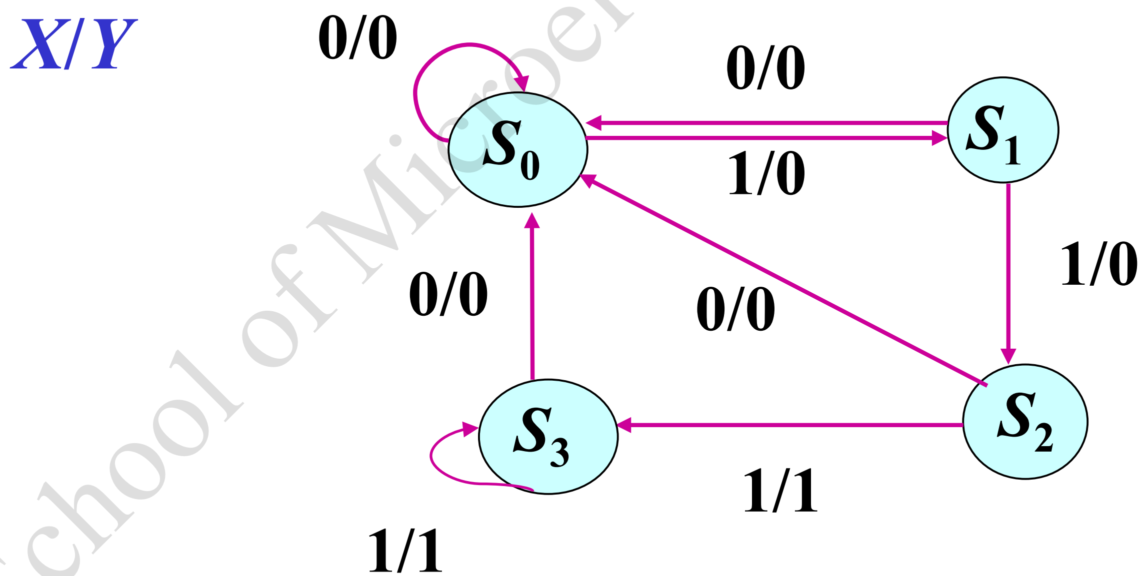
S_1—收到一个1后的状态；

S_2—连续收到两个1后的状态；

S_3—连续收到三个1（以及三个以上1）后的状态。

X=1, 收到一个 “1”

输入三个1（以及三个以上1）时，输出$Y=1$



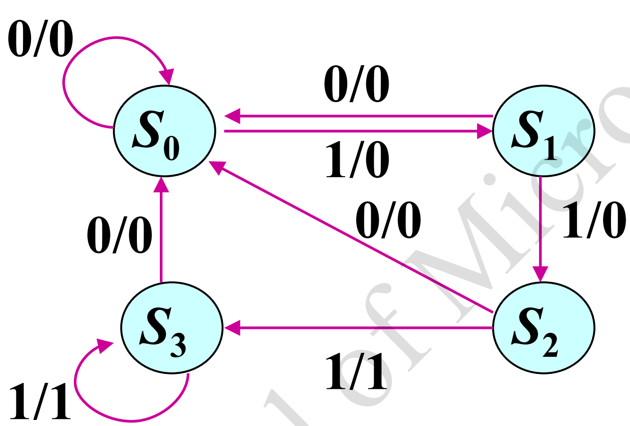
3）状态化简

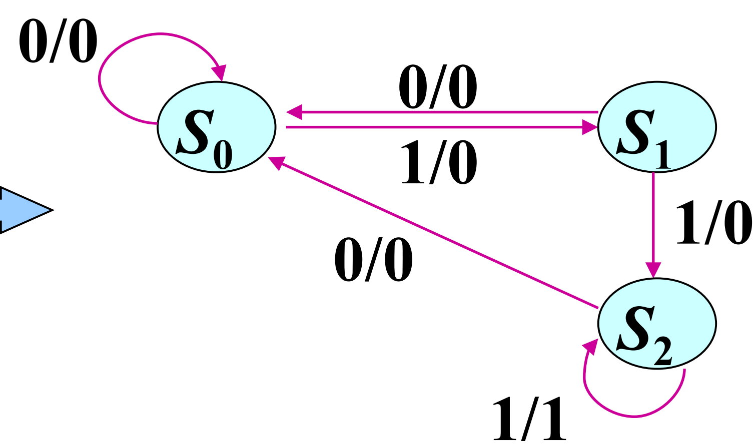
状态化简：合并等效状态

等效状态：

在相同的输入条件下，输出相同、次态也相同的状态

S_2 和 S_3 是等效状态，将 S_2 和 S_3 合并为 S_2





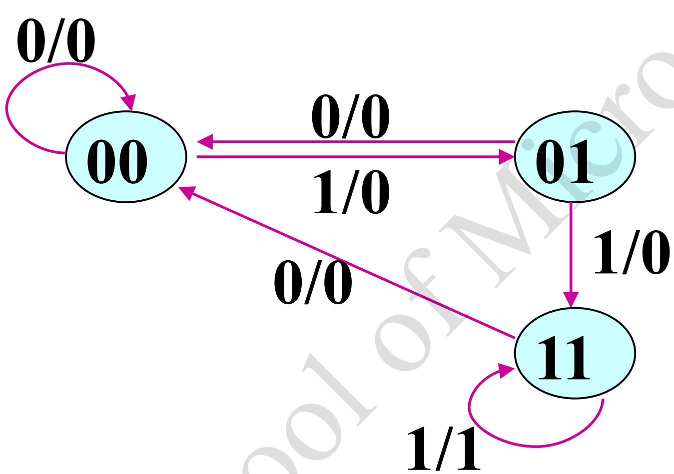
3）状态分配、编码

Set $S_0 = 00$

$S_1 = 01$ 　编码可以不连续

$S_2 = 11$

编码后的状态图



状态表

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	Φ	Φ	Φ
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	Φ	Φ	Φ
1	1	1	1	1	1

4) 选触发器及控制输入

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	Φ	Φ	Φ
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	Φ	Φ	Φ
1	1	1	1	1	1

Q_1^{n+1}

Q_0^n \ XQ_1^n	00	01	11	10
0	0	Φ	Φ	0
1	0	0	1	1

$$Q_1^{n+1} = XQ_0^n = D_1 \qquad D_1 = XQ_0^n$$

Q_0^{n+1}

Q_0^n \ XQ_1^n	00	01	11	10
0	0	Φ	Φ	1
1	0	0	1	1

$$Q_0^{n+1} = X = D_0 \qquad D_0 = X$$

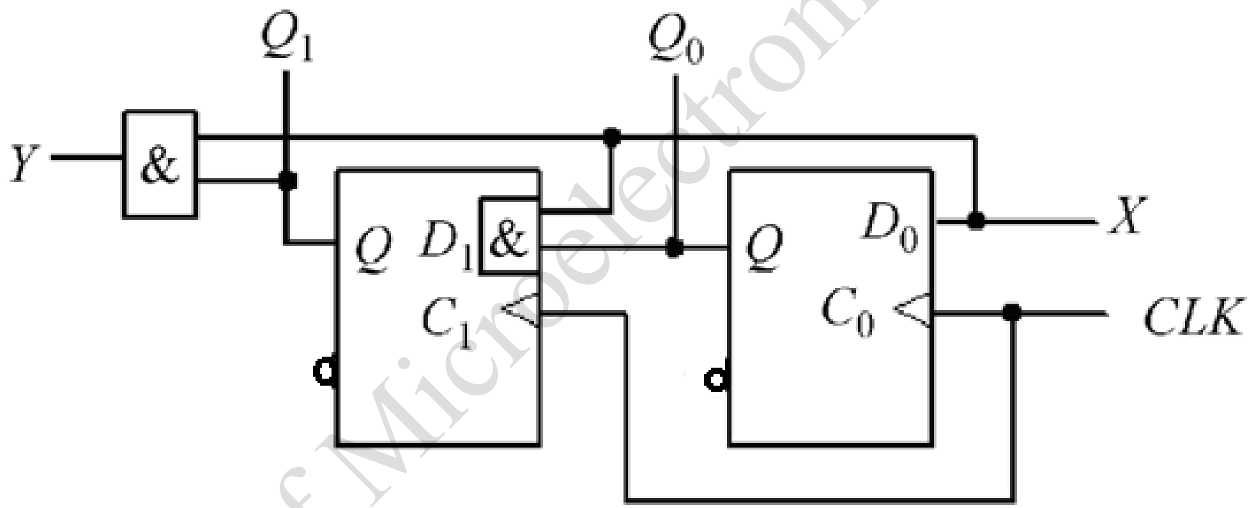
Y

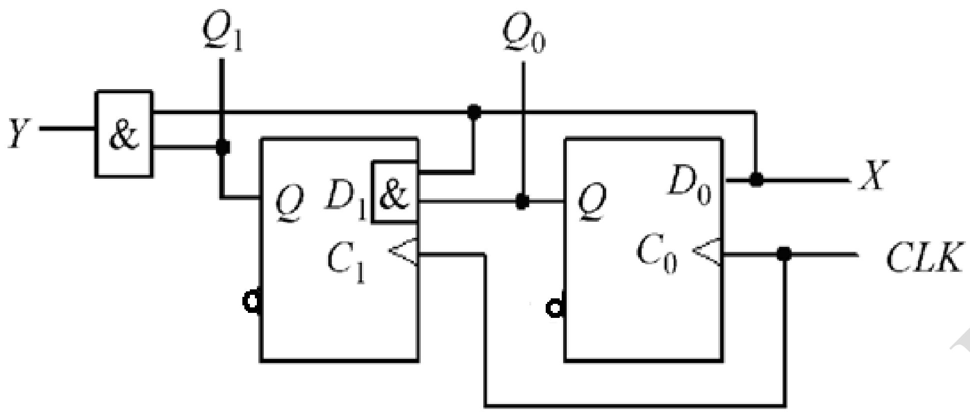
Q_0^n \ XQ_1^n	00	01	11	10
0	0	Φ	Φ	0
1	0	0	1	0

$$Y = XQ_1^n$$

5) 电路

2 D-FFs $D_1 = XQ_0^n$ $D_0 = X$ $Y = XQ_1^n$





$$Q_1^{n+1} = XQ_0^n$$

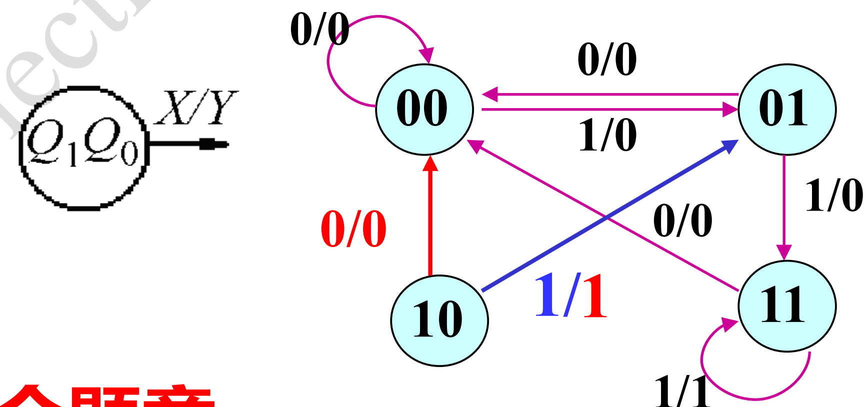
$$Q_0^{n+1} = X$$

$$Y = XQ_1^n$$

6）自启动

从电路的状态图分析

可以自启动



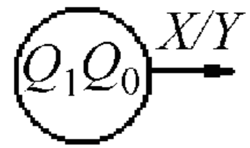
但其功能错误，

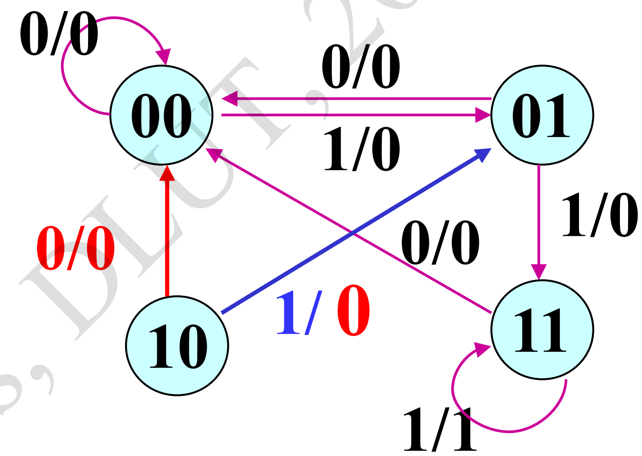
输出应设置为0，才符合题意

检测 连续输入三个及以上个1时，电路输出$Y=1$**。**

自启动

让X=1，10对应的输出为0





状态表

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	1	1	1

Y (Q_0^n \ XQ_1^n)	00	01	11	10
0	0	0	0	0
1	0	0	1	0

$$Y = XQ_1^nQ_0^n$$

既实现自启动，也符号题意。

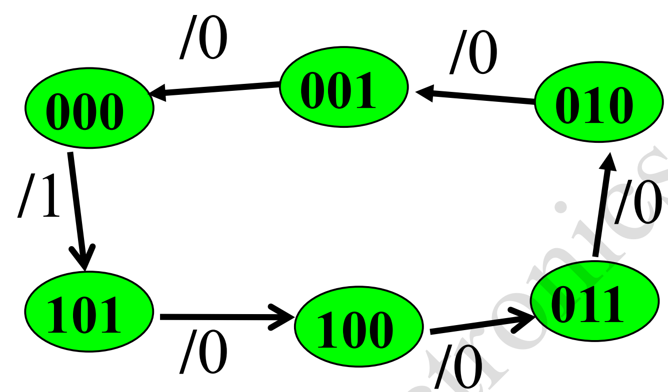
可以在最初设计时考虑自启动（K-map随意项的填写）

例 3. 设计 M-6 减法计数器

6 个状态 **直接用3位数编码** $Q_3Q_2Q_1$

借位输出 *Z*

/ Z



Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	0

Q_3^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	1

Q_2^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	1	Φ	0

Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	1
1	0	0	Φ	0

Q_3^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	1

Q_2^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	1	Φ	0

Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	1
1	0	0	Φ	0

$$Q_3^{n+1} = \overline{Q_3}\,\overline{Q_2}\,\overline{Q_1} + Q_3Q_1$$

$$D_3 = \overline{Q_3}\,\overline{Q_2}\,\overline{Q_1} + Q_3Q_1$$

$$Q_2^{n+1} = Q_2Q_1 + Q_3\overline{Q_1}$$

$$D_2 = Q_2Q_1 + Q_3\overline{Q_1}$$

$$Q_1^{n+1} = \overline{Q_1}$$

$$D_1 = \overline{Q_1}$$

Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	0

$$Z = \overline{Q_3}\,\overline{Q_2}\,\overline{Q_1}$$

自启动及电路图略