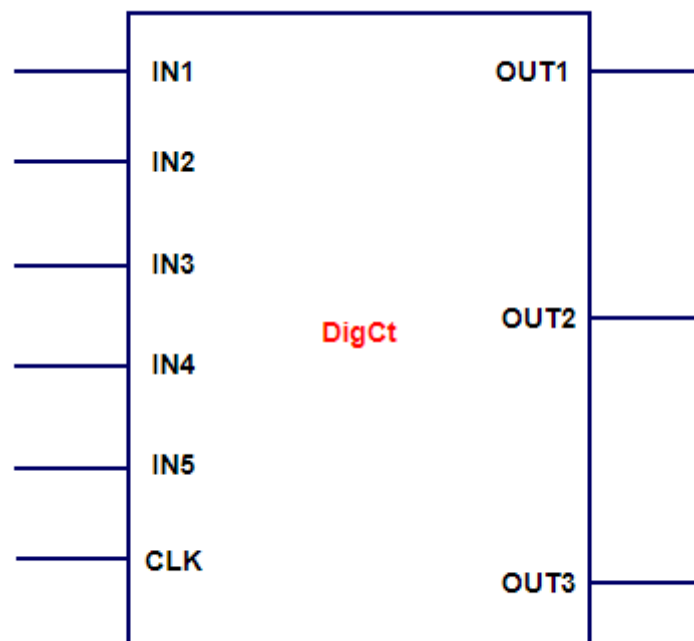


# Assignment 1

## introduction: -

The target of this assignment is to start building digital circuit using Verilog language that contain both combinational logic and sequential logic using **always block**.

## Block Interface

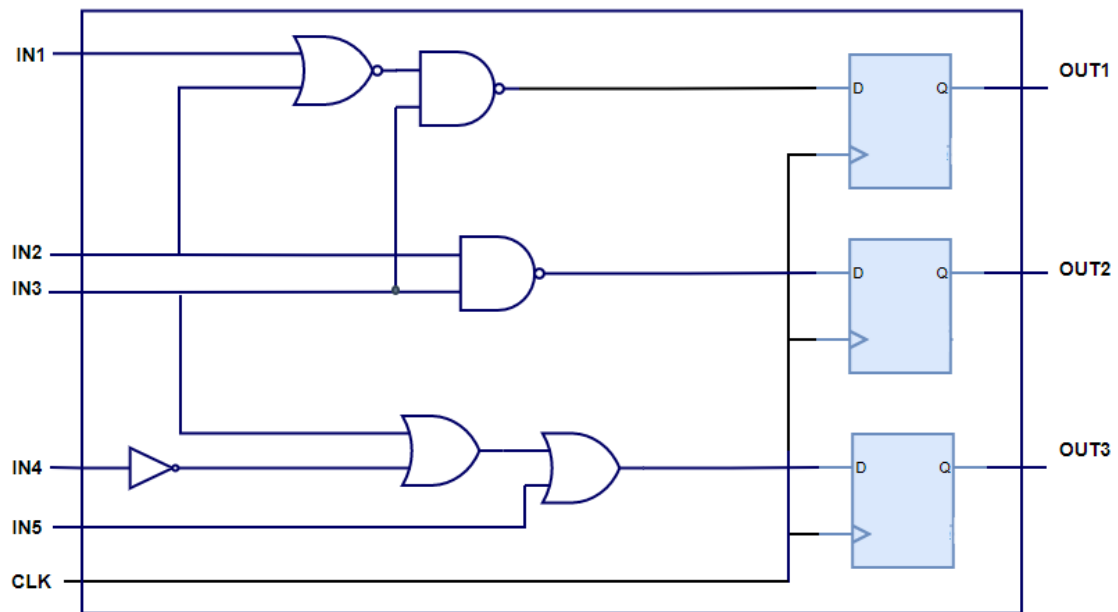


Block(Module) Name: DigCt

Inputs: IN1, IN2, IN3, IN4, IN5, CLK (all inputs of 1-bit width)

Outputs: OUT1, OUT2, OUT3 (output of 1-bit width)

## Circuit Implementation: -



## Requirements: -

- Design the above circuit using Verilog language.