Information Technology Institute

Digital Design and Computer Architecture

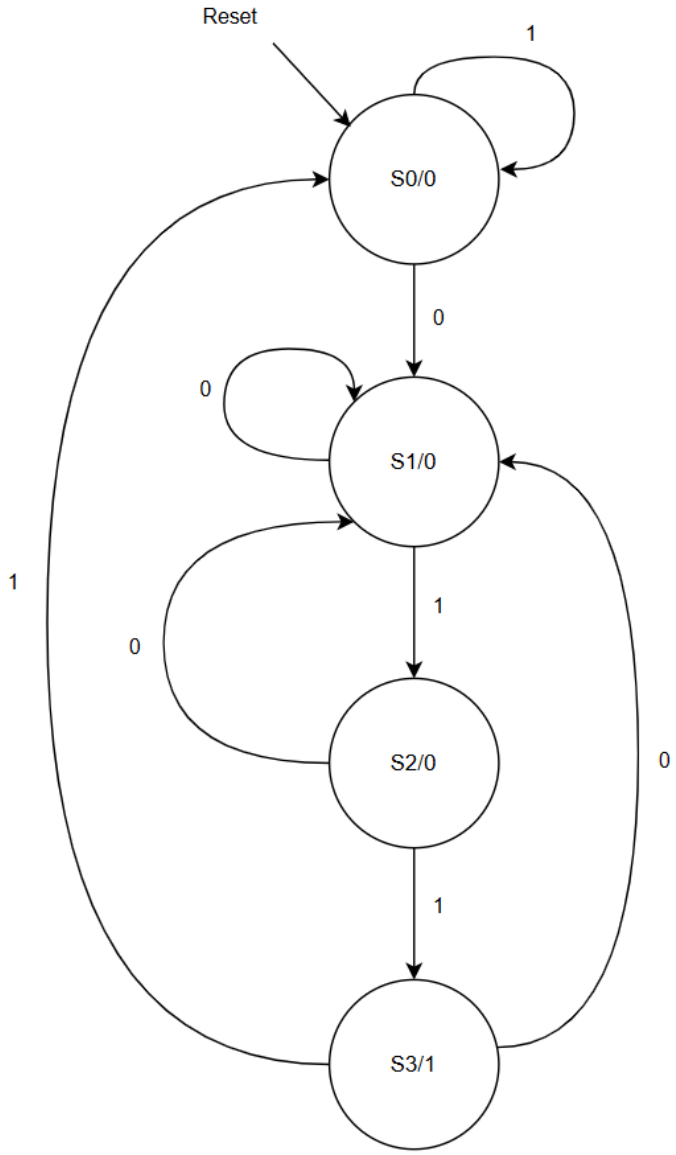
Lab 1: FSM

Submitted by: Ali Yehia Abdelmonem

Sequence Detector of 011 using Moore and Mealy

1. Moore FSM Design

1.1 State Transition Diagram for Moore FSM



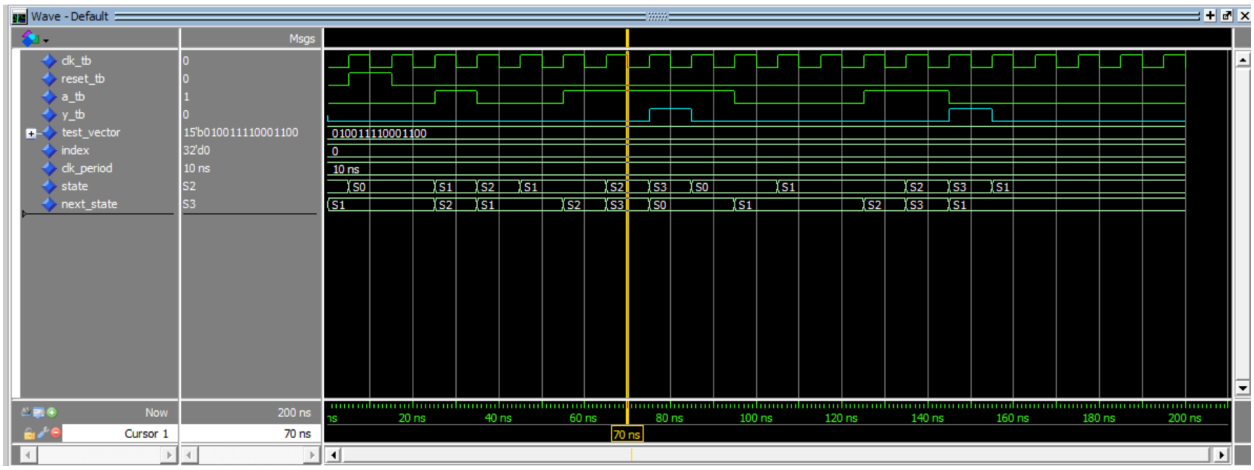
1.2 Moore FSM VHDL Code

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity patternMoore is
    port(
        clk   : in  STD_LOGIC;
        reset : in  STD_LOGIC;
        a     : in  STD_LOGIC;
        y     : out STD_LOGIC
    );
end;

architecture synth of patternMoore is
    type state_type is (S0, S1, S2, S3);
    signal state, next_state : state_type;
begin
    -- State register
    process(clk, reset)
    begin
        if reset = '1' then
            state <= S0;
        elsif rising_edge(clk) then
            state <= next_state;
        end if;
    end process;

    -- Next state logic
    process(state, a)
    begin
        case state is
            when S0 =>
                if a = '1' then
                    next_state <= S0;
                else
                    next_state <= S1;
                end if;
            when S1 =>
                if a = '1' then
                    next_state <= S2;
                else
                    next_state <= S1;
                end if;
            when S2 =>
                if a = '1' then
                    next_state <= S3;
                else
                    next_state <= S1;
                end if;
            when S3 =>
                if a = '1' then
                    next_state <= S0;
                else
                    next_state <= S1;
                end if;
            when others =>
                next_state <= S0;
        end case;
    end process;

    -- Output logic
    y <= '1' when state = S3 else '0';
end;
```

1.3 Moore FSM Testbench Code

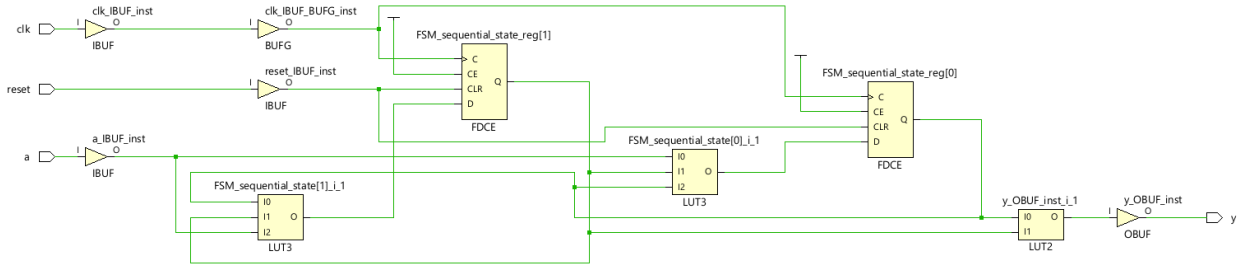
```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity patternMoore_tb is
end entity;

architecture simulation of patternMoore_tb is
    constant clk_period : time := 10 ns;
    signal clk_tb : std_logic := '0';
    signal reset_tb : std_logic := '0';
    signal a_tb : std_logic := '0';
    signal y_tb : std_logic;
    signal test_vector : std_logic_vector(14 downto 0) := "010011110001100";
    signal index : integer := 0;

begin

    -- Clock generation process
    clock_gen : process
    begin
        clk_tb <= '0';
        wait for clk_period / 2;
        clk_tb <= '1';
        wait for clk_period / 2;
    end process;

    -- Instantiate the Moore FSM component
    moore_fsm_inst : entity work.patternMoore
    port map (
        clk   => clk_tb,
        reset => reset_tb,
        a     => a_tb,
        y     => y_tb
    );

    -- Stimulus process to apply inputs and reset
    stimulus_proc : process
    begin
        -- Apply reset pulse
        wait until rising_edge(clk_tb);
        reset_tb <= '1';
        wait until rising_edge(clk_tb);
        reset_tb <= '0';

        -- Apply input vector pattern to the FSM
        for index in test_vector'range loop
            a_tb <= test_vector(index);
            wait until rising_edge(clk_tb);
        end loop;

        -- End of test
        wait;
    end process;

    monitor_output : process(y_tb)
    begin
        if y_tb = '1' then
            report "Output Y is set to 1 at time " & time'image(now);
        end if;
    end process;

end architecture;
```

1.4 Simulation Results




```
VSIM(paused)> run
# ** Note: Output Y is set to 1 at time 75 ns
#    Time: 75 ns  Iteration: 3  Instance: /patternmoore_tb
# ** Note: Output Y is set to 1 at time 145 ns
#    Time: 145 ns  Iteration: 3  Instance: /patternmoore_tb

VSIM(paused)>
```

1.5 Synthesis Results for Default Encoding (binary)



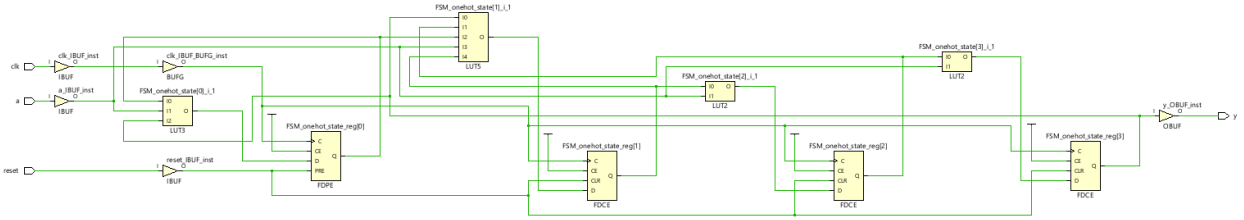
1.6 Log File Output

```
INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'patternMoore'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                      s0 |                               00 |                               00
                      s1 |                               01 |                               01
                      s2 |                               10 |                               10
                      s3 |                               11 |                               11
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'sequential' in module 'patternMoore'
```

Figure 1-1: Default State Encoding in Vivado.

```
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     1|
|3     |LUT3 |     2|
|4     |FDCE |     2|
|5     |IBUF |     3|
|6     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    10|
+------+---------+-------+------+
---------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:07 ; elapsed = 00:00:22 . Memory (MB): peak = 1590.285 ; gain = 904.551
---------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:07 ; elapsed = 00:00:22 . Memory (MB): peak = 1590.285 ; gain = 904.551
Synthesis Optimization Complete : Time (s): cpu = 00:00:07 ; elapsed = 00:00:22 . Memory (MB): peak = 1590.285 ; gain = 904.551
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1620.469 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1722.086 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete | Checksum: 1bc50985
INFO: [Common 17-83] Releasing license: Synthesis
16 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:40 . Memory (MB): peak = 1722.086 ; gain = 1076.621
Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1722.086 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Users/aliye/OneDrive/Desktop/ITI/01-Technical/12-Computer Architecture/My Labs/Lab1 FSM/Moore_FSM/Moore_FSM.runs/synth_1/patternMoore.dcp' has been generated.
INFO: [Vivado 12-24828] Executing command : report_utilization -file patternMoore_utilization_synth.rpt -pb patternMoore_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Tue Dec 17 20:55:32 2024...
```

1.7 Changing FSM Encoding Style from auto (binary) to one-hot



1.8 New Log File for one-hot State Encoding

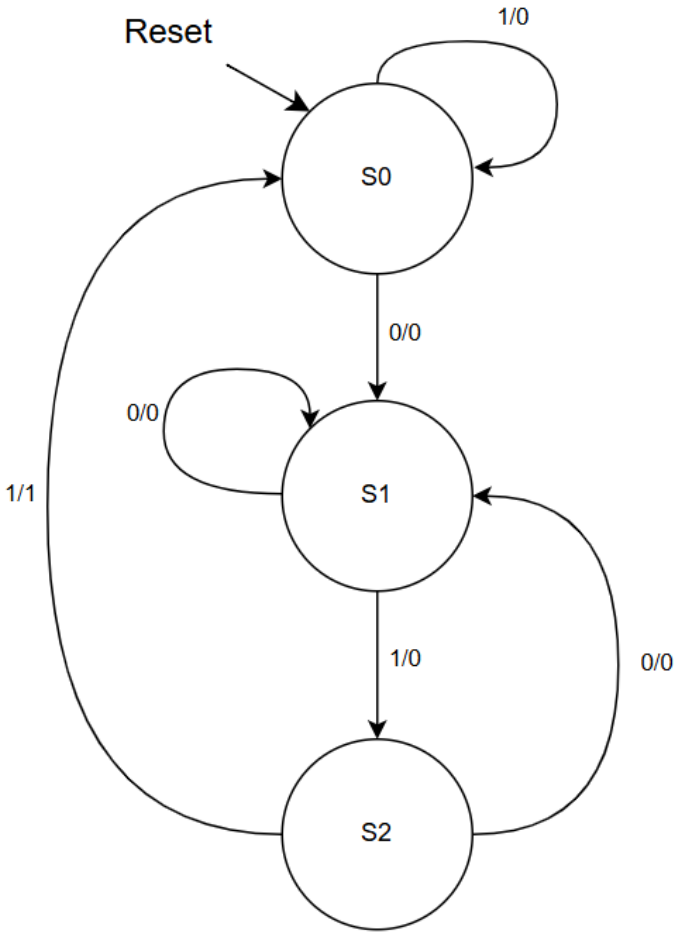
```
INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'patternMoore'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                      s0 |                             0001 |                               00
                      s1 |                             0010 |                               01
                      s2 |                             0100 |                               10
                      s3 |                             1000 |                               11
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'one-hot' in module 'patternMoore'
```

Figure 1-2: Changing to one-hot State Encoding in Vivado.

```
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     2|
|3     |LUT3 |     1|
|4     |LUT5 |     1|
|5     |FDCE |     3|
|6     |FDPE |     1|
|7     |IBUF |     3|
|8     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    13|
+------+---------+-------+------+
---------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1590.395 ; gain = 894.062
---------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1590.395 ; gain = 894.062
Synthesis Optimization Complete : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1590.395 ; gain = 894.062
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1618.750 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1723.699 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete | Checksum: 907705e7
INFO: [Common 17-83] Releasing license: Synthesis
20 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:12 ; elapsed = 00:00:35 . Memory (MB): peak = 1723.699 ; gain = 1073.812
Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1723.699 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Users/aliye/OneDrive/Desktop/ITI/01-Technical/12-Computer Architecture/My Labs/Lab1 FSM/Moore_FSM/Moore_FSM.runs/synth_1/patternMoore.dcp' has been generated.
INFO: [Vivado 12-24828] Executing command : report_utilization -file patternMoore_utilization_synth.rpt -pb patternMoore_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Tue Dec 17 21:14:59 2024...
```

2. Mealy FSM Design

2.1 State Transition Diagram for Mealy FSM



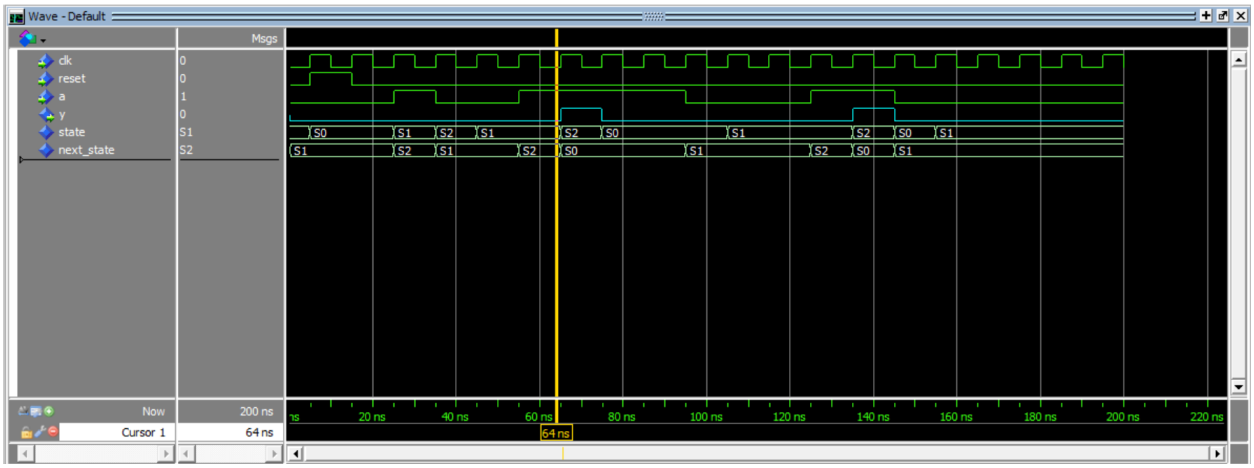
2.2 Mealy FSM VHDL Code

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity patternMealy is
    port(
        clk   : in  STD_LOGIC;
        reset : in  STD_LOGIC;
        a     : in  STD_LOGIC;
        y     : out STD_LOGIC
    );
end;

architecture synth of patternMealy is
    type state_type is (S0, S1, S2);
    signal state, next_state : state_type;
begin
    -- State register
    process(clk, reset)
    begin
        if reset = '1' then
            state <= S0;
        elsif rising_edge(clk) then
            state <= next_state;
        end if;
    end process;

    -- Next state logic
    process(state, a)
    begin
        case state is
            when S0 =>
                if a = '1' then
                    next_state <= S0;
                else
                    next_state <= S1;
                end if;
            when S1 =>
                if a = '1' then
                    next_state <= S2;
                else
                    next_state <= S1;
                end if;
            when S2 =>
                if a = '1' then
                    next_state <= S0;
                else
                    next_state <= S1;
                end if;
            when others =>
                next_state <= S0;
        end case;
    end process;

    -- Output logic
    y <= '1' when (a = '1' and state = S2) else '0';

end;
```

2.3 Mealy FSM Testbench Code

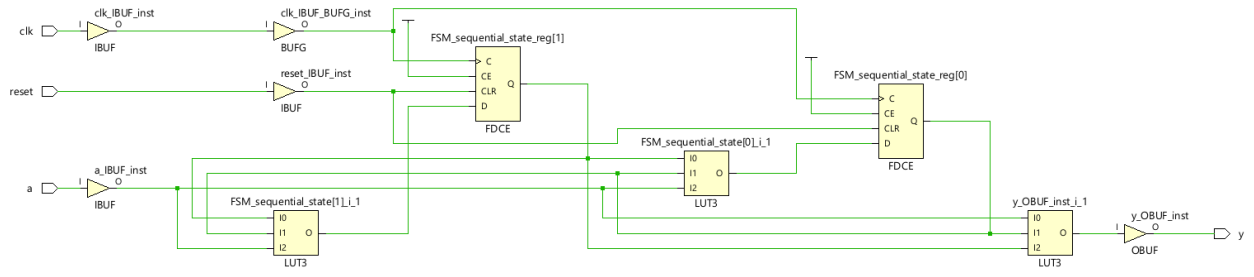
```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity patternMealy_tb is
end entity;

architecture simulation of patternMealy_tb is
    constant clk_period : time := 10 ns;
    signal clk_tb : std_logic := '0';
    signal reset_tb : std_logic := '0';
    signal a_tb : std_logic := '0';
    signal y_tb : std_logic;
    signal test_vector : std_logic_vector(14 downto 0) := "010011110001100";
    signal index : integer := 0;

begin

    -- Clock generation process
    clock_gen : process
    begin
        clk_tb <= '0';
        wait for clk_period / 2;
        clk_tb <= '1';
        wait for clk_period / 2;
    end process;

    -- Instantiate the Mealy FSM component
    mealy_fsm_inst : entity work.patternMealy
    port map (
        clk   => clk_tb,
        reset => reset_tb,
        a     => a_tb,
        y     => y_tb
    );

    -- Stimulus process to apply inputs and reset
    stimulus_proc : process
    begin
        -- Apply reset pulse
        wait until rising_edge(clk_tb);
        reset_tb <= '1';
        wait until rising_edge(clk_tb);
        reset_tb <= '0';

        -- Apply input vector pattern to the FSM
        for index in test_vector'range loop
            a_tb <= test_vector(index);
            wait until rising_edge(clk_tb);
        end loop;

        -- End of test
        wait;
    end process;

    monitor_output : process(y_tb)
    begin
        if y_tb = '1' then
            report "Output Y is set to 1 at time " & time'image(now);
        end if;
    end process;

end architecture;
```

2.4 Simulation Results




```
VSIM(paused)> run
# ** Note: Output Y is set to 1 at time 65 ns
#    Time: 65 ns  Iteration: 3  Instance: /patternmealy_tb
# ** Note: Output Y is set to 1 at time 135 ns
#    Time: 135 ns  Iteration: 3  Instance: /patternmealy_tb

VSIM(paused)>
```

2.5 Synthesis Results for Default Encoding (binary)



2.6 Log File Output

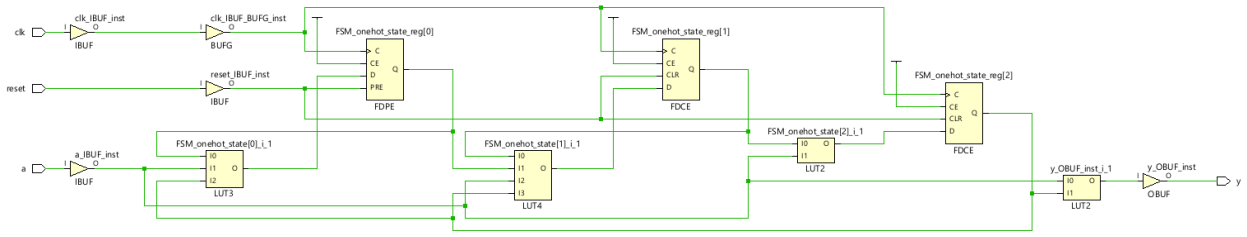
```
INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'patternMealy'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                      s0 |                               00 |                               00
                      s1 |                               01 |                               01
                      s2 |                               10 |                               10
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'sequential' in module 'patternMealy'
```

Figure 2-1: Default State Encoding in Vivado

```
Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT3 |     3|
|3     |FDCE |     2|
|4     |IBUF |     3|
|5     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    10|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1588.797 ; gain = 903.578
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1588.797 ; gain = 903.578
Synthesis Optimization Complete : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1588.797 ; gain = 903.578
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1618.406 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1721.582 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete | Checksum: eda505c9
INFO: [Common 17-83] Releasing license: Synthesis
15 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:23 ; elapsed = 00:00:34 . Memory (MB): peak = 1721.582 ; gain = 1077.387
Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1721.582 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Users/aliye/OneDrive/Desktop/ITI/01-Technical/12-Computer Architecture/My Labs/Lab1 FSM/Mealy_FSM/Mealy_FSM.runs/synth_1/patternMealy.dcp' has been generated.
INFO: [Vivado 12-24828] Executing command : report_utilization -file patternMealy_utilization_synth.rpt -pb patternMealy_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Tue Dec 17 21:34:43 2024...
```

.

2.7 Changing FSM Encoding Style to one-hot



2.8 New Log File for one-hot State Encoding

```
INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'patternMealy'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                      s0 |                              001 |                              00
                      s1 |                              010 |                              01
                      s2 |                              100 |                              10
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'one-hot' in module 'patternMealy'
```

Figure 2-2: Changing to one-hot State Encoding in Vivado.

```
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     2|
|3     |LUT3 |     1|
|4     |LUT4 |     1|
|5     |FDCE |     2|
|6     |FDPE |     1|
|7     |IBUF |     3|
|8     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    12|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1594.227 ; gain = 898.000
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1594.227 ; gain = 898.000
Synthesis Optimization Complete : Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 1594.227 ; gain = 898.000
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1624.109 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1726.914 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete | Checksum: e4e622e6
INFO: [Common 17-83] Releasing license: Synthesis
19 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:25 ; elapsed = 00:00:34 . Memory (MB): peak = 1726.914 ; gain = 1077.008
Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1726.914 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Users/aliye/OneDrive/Desktop/ITI/01-Technical/12-Computer Architecture/My Labs/Lab1 FSM/Mealy_FSM/Mealy_FSM.runs/synth_1/patternMealy.dcp' has been generated.
INFO: [Vivado 12-24828] Executing command : report_utilization -file patternMealy_utilization_synth.rpt -pb patternMealy_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Tue Dec 17 21:43:27 2024...
```

3. Differences between Moore and Mealy FSMs

The primary differences between Moore and Mealy FSMs are observed in their state requirements and output dependencies. A Mealy FSM generally requires one fewer state than a Moore FSM to represent the same behavior. Additionally, in a Moore FSM, the output depends solely on the current state, whereas in a Mealy FSM, the output depends on both the current state and the input. These differences are illustrated in the following two figures.

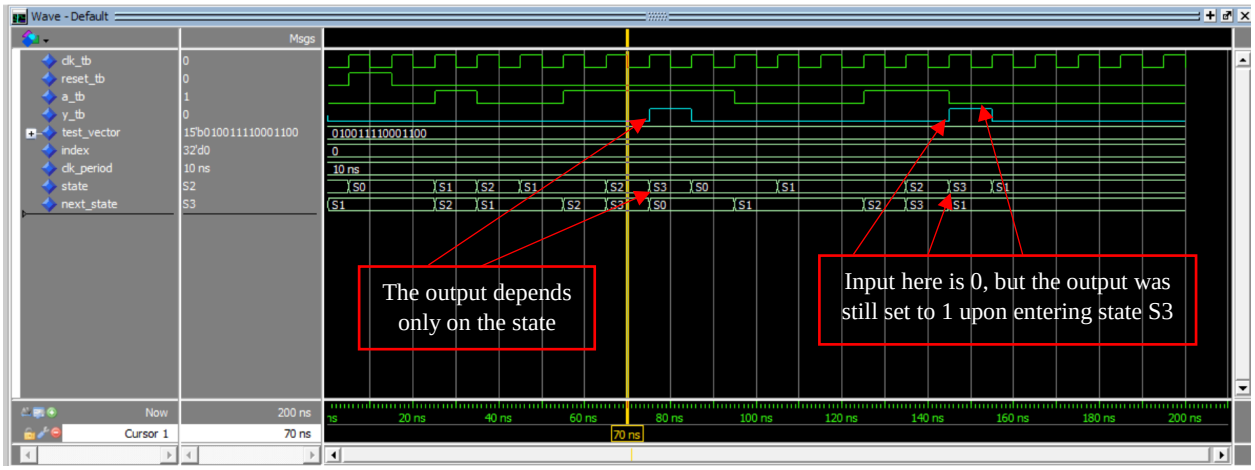


Figure 3-1: Moore FSM Waveform.

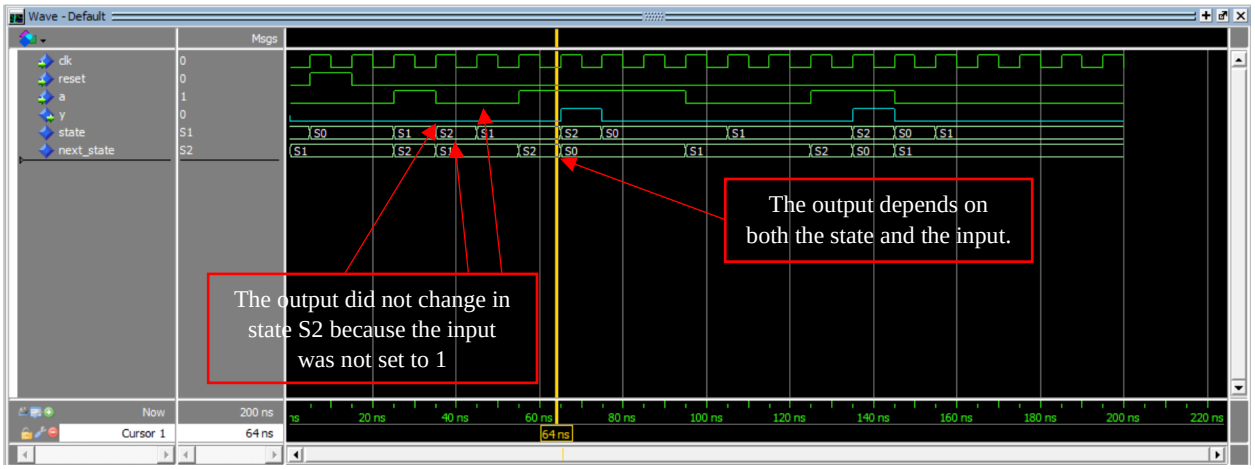


Figure 3-2: Mealy FSM Waveform.