Information Technology Institute

Digital Circuits
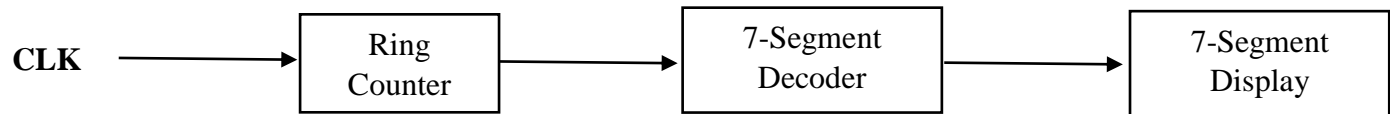
Lab 1

Submitted by:

Ali Yehia Abdelmonem

Design Report

1. Overview of Design

CLK ──────→ | Ring Counter | ──────→ | 7-Segment Decoder | ──────→ | 7-Segment Display |

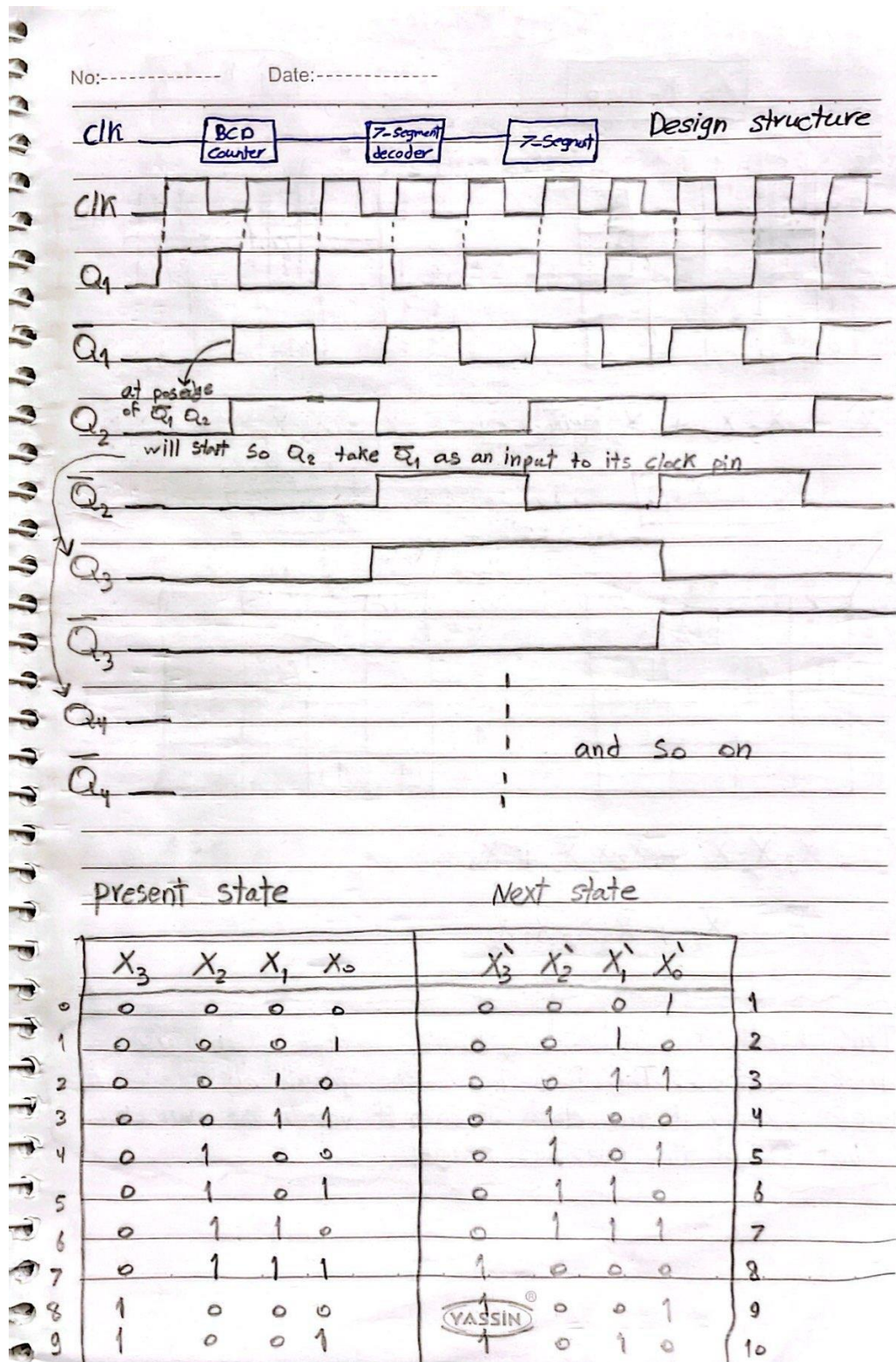## 2. Components Used

1. D-Flip Flops
2. AND, OR and NOT Gates
3. Input Logic
4. Clock Source
5. 7- Segment Display

3. Step-by-step Description of the Design Process

No:-------------   Date:-------------

Design structure

clk ──→ | BCD Counter | ──→ | 7-Segment decoder | ──→ | 7-Segut |

clk

Q_1

$\overline{Q_1}$

at posedge of Q_1 Q_2 will start So Q_2 take $\overline{Q_1}$ as an input to its clock pin

$\overline{Q_2}$

Q_3

$\overline{Q_3}$

Q_4

$\overline{Q_4}$

and so on

Present state   Next state

	X_3	X_2	X_1	X_0	X_3'	X_2'	X_1'	X_0'	
0	0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	0	1	0	2
2	0	0	1	0	0	0	1	1	3
3	0	0	1	1	0	1	0	0	4
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	1	0	6
6	0	1	1	0	0	1	1	1	7
7	0	1	1	1	1	0	0	0	8
8	1	0	0	0	0	0	0	1	9
9	1	0	0	1	1	0	1	0	10

Ring Counter

X_0' K-map

X_3X_2 \ X_1X_0	00	01	11	10
00	1			1
01	1			1
11				
10	1			

X_1' K-map

X_3X_2 \ X_1X_0	00	01	11	10
00		1		1
01		1		1
11				
10		1		

$$X_0' = \overline{X_3}\,\overline{X_0} + \overline{X_2}\,\overline{X_1}\,\overline{X_0}$$

$$X_1' = \overline{X_3}\,\overline{X_1}\,X_0 + \overline{X_3}\,X_1\,\overline{X_0} + \overline{X_2}\,\overline{X_1}\,X_0$$

X_2' K-map

X_3X_2 \ X_1X_0	00	01	11	10
00			1	
01	1	1		1
10				
11				

X_3' K-map

X_3X_2 \ X_1X_0	00	01	11	10
00				
01			1	
11				
10	1	1		

$$X_2' = \overline{X_3}\,X_2\,\overline{X_1} + \overline{X_3}\,X_2\,\overline{X_0} + \overline{X_3}\,\overline{X_2}\,X_1\,X_0$$

$$X_3' = \overline{X_3}\,\overline{X_2}\,\overline{X_1} + \overline{X_3}\,X_2\,X_1\,X_0$$

This method is harder, more complex and uses more gates. Therefore from the graph all needed are flip flops only if the clock of each FF wasn't the main clk but $\overline{Q}$ of the previous stage.

3

7-segment decoder

Similarly From K-map

(a) segment For example "①" 4 corners grouped together

AB\CD	00	01	11	10
00	①		1	①
01		1	1	1
11	1		1	1
10	①	1		①

$$a = A\bar{B}\bar{C} + \bar{A}BD + A\bar{D} + \bar{A}C + BC + \bar{B}\bar{D}$$

$$b = \bar{A}\bar{C}\bar{D} + \bar{A}CD + A\bar{C}D + \bar{B}\bar{C} \cdot + \bar{B}\bar{D}$$

$$c = \bar{A}\bar{C} + \bar{A}D + \bar{C}D + \bar{A}B + A\bar{B}$$

$$d = \bar{A}\bar{B}\bar{D} + \bar{B}CD + B\bar{C}D + BC\bar{D} + A\bar{C}$$

$$e = AC + AB + C\bar{D} + \bar{B}\bar{D}$$

$$F = \bar{A}B\bar{C} + \bar{C}\bar{D} + B\bar{D} + A\bar{B} + AC$$

$$g = \bar{A}B\bar{C} + A\bar{B} + AD + \bar{B}C + C\bar{D}$$

4. Screenshots of the Simulation

Figure 1: Start of simulation.

Figure 2: Simulation part 1.
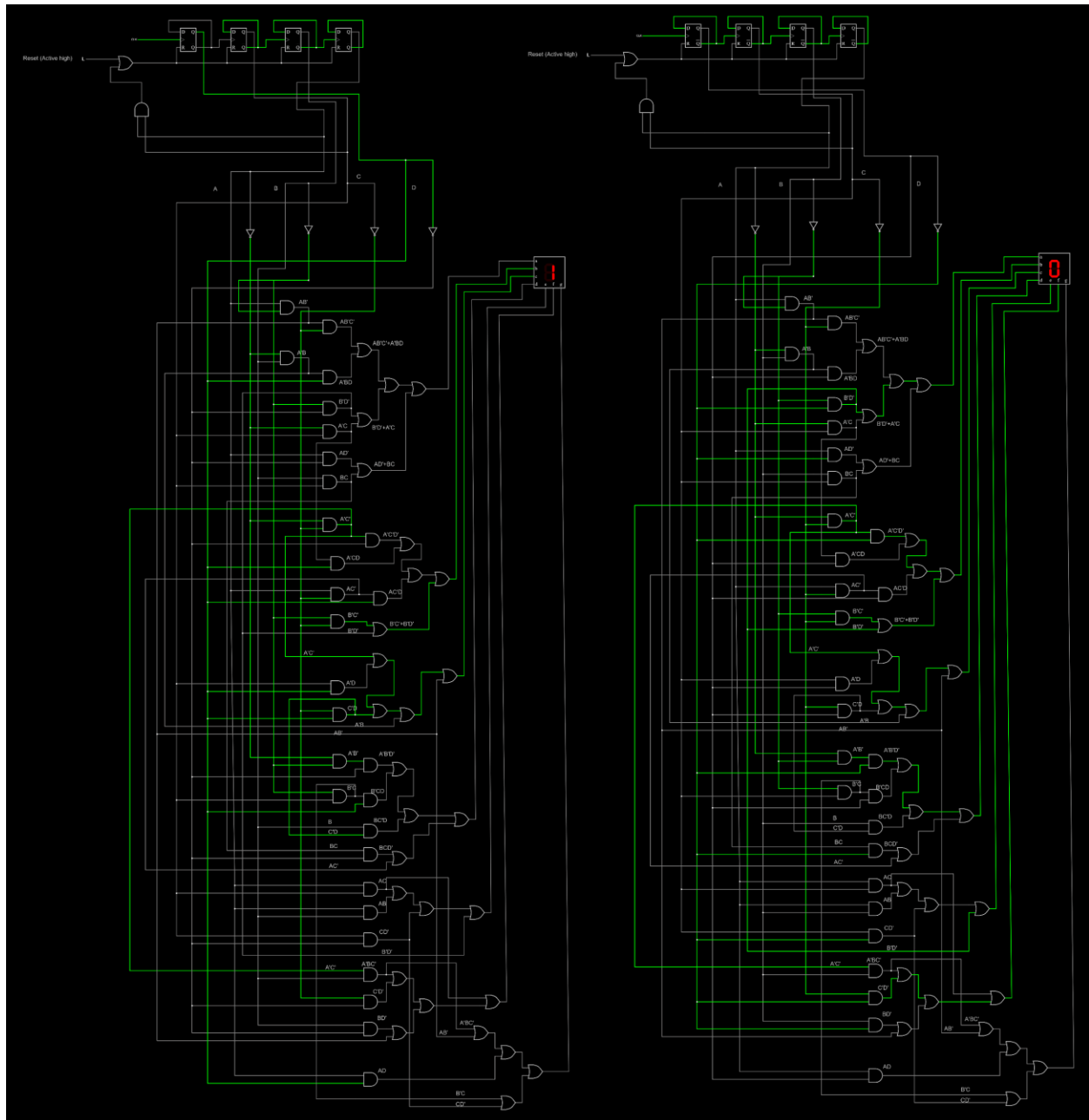
Figure 3: Simulation part 2.

Figure 4: Simulation part 3.

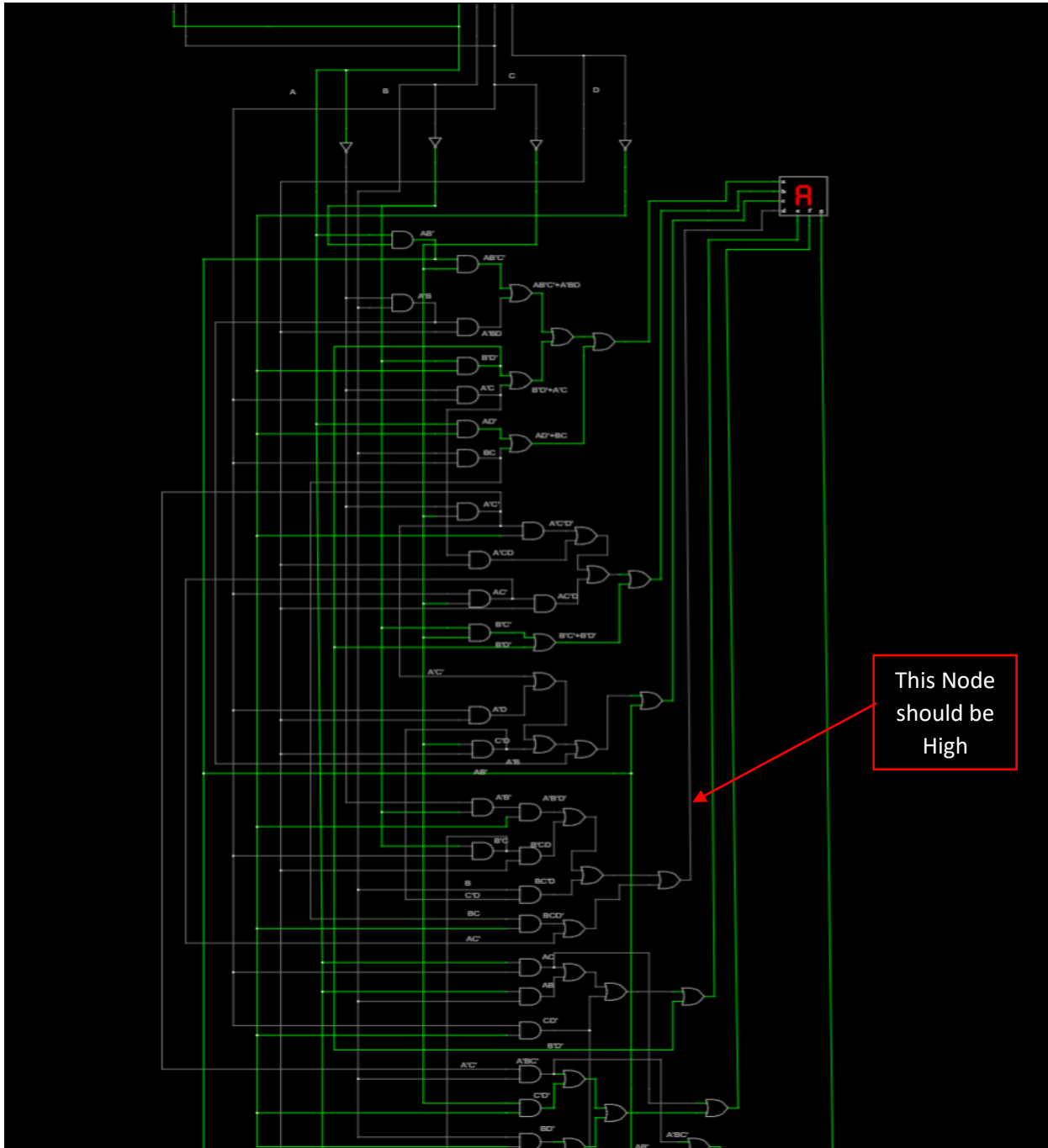# 5. Issues Faced

Number 8 is not displayed correctly

Figure 5: Number 8 not displayed correctly.

According to A B C D truth table:

At number 8 I should have A=1, B=0, C=0, D=0 which is AB'C'D'

And (d) segment equation is:

d = A'B'D' + B'CD + BC'D + BCD' + AC'

Therefore, the argument that must be high to satisfy the high condition for d segment for number 8 will be AC' which is part of AB'C'D' and by checking its node I found out that:
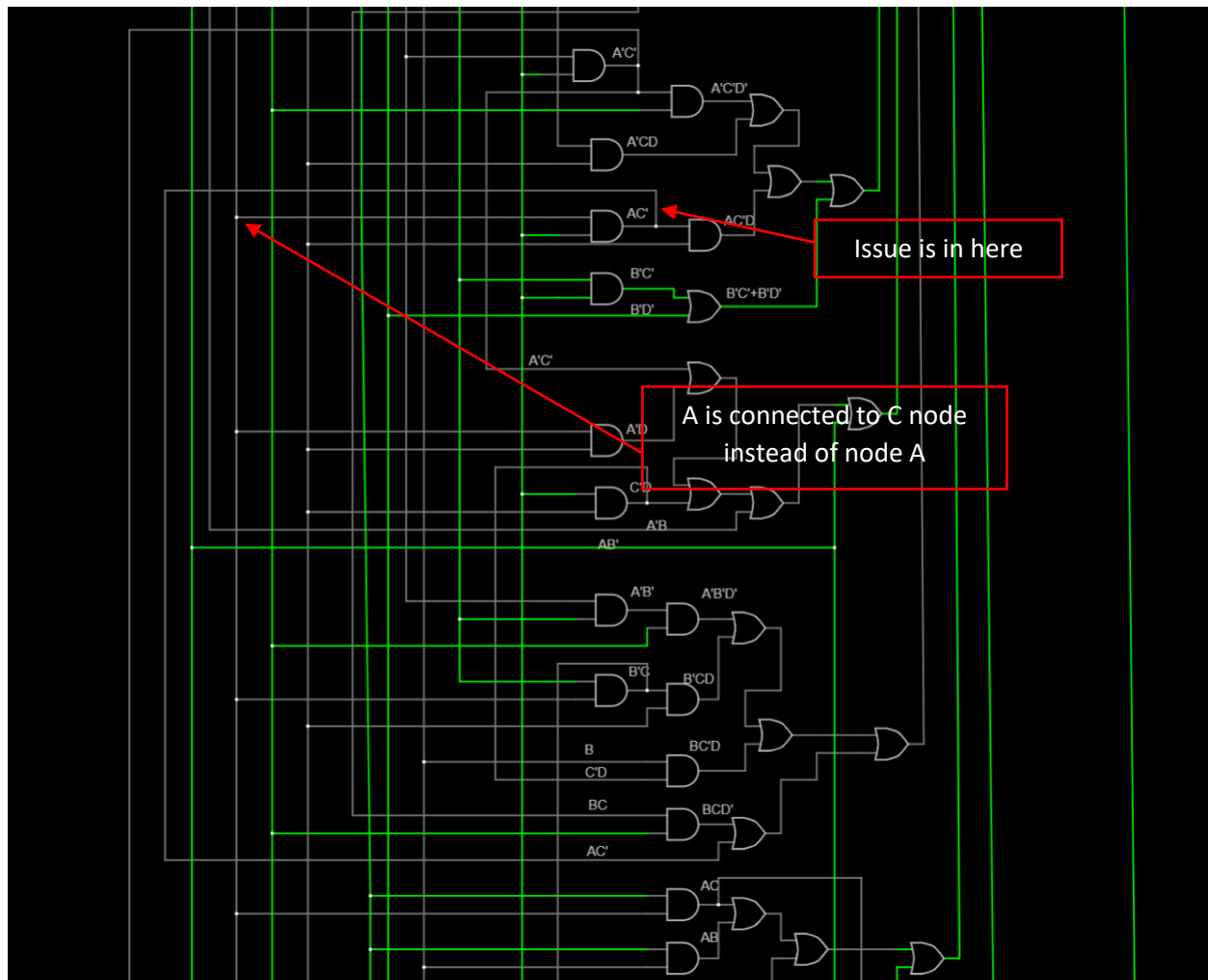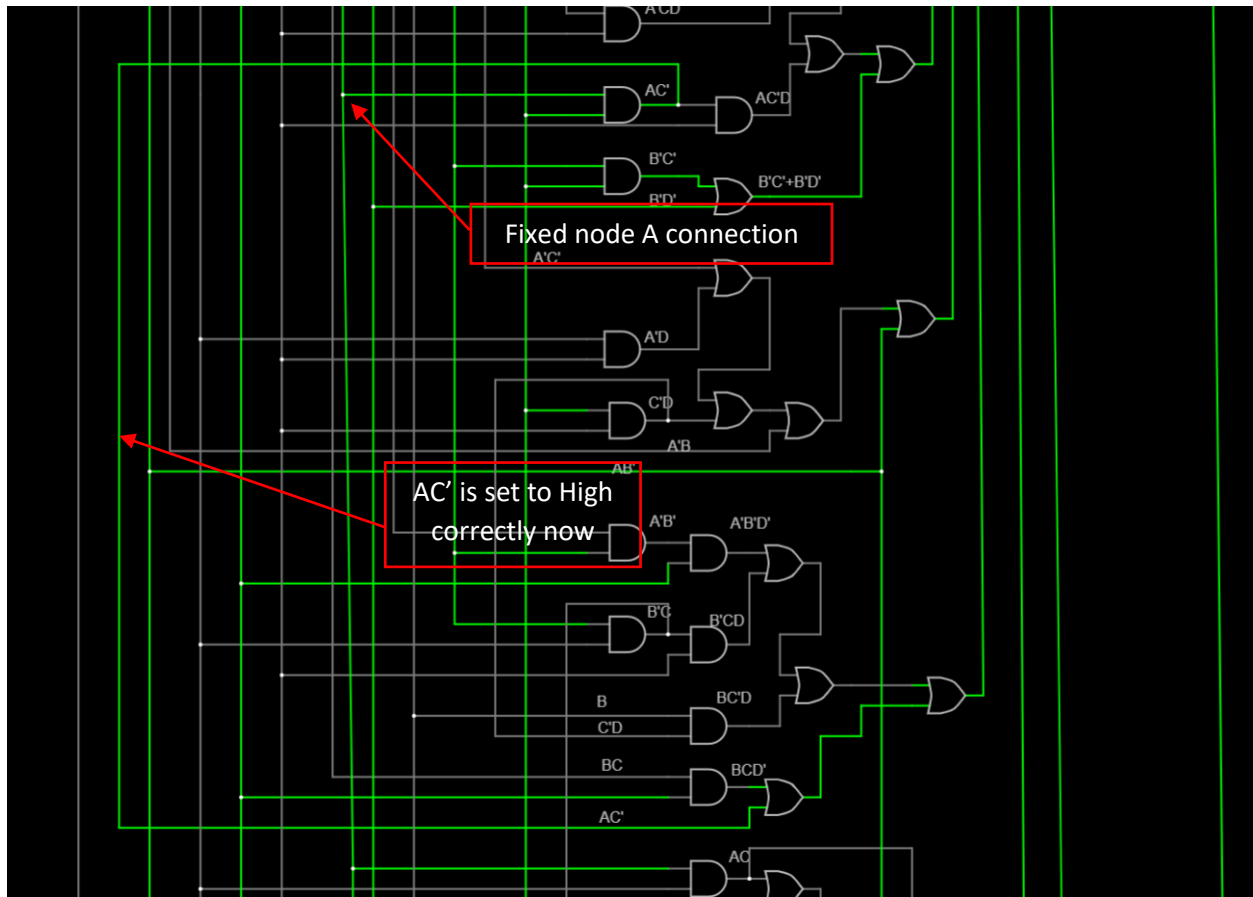

Figure 6: Analyzing and spotting the issue.
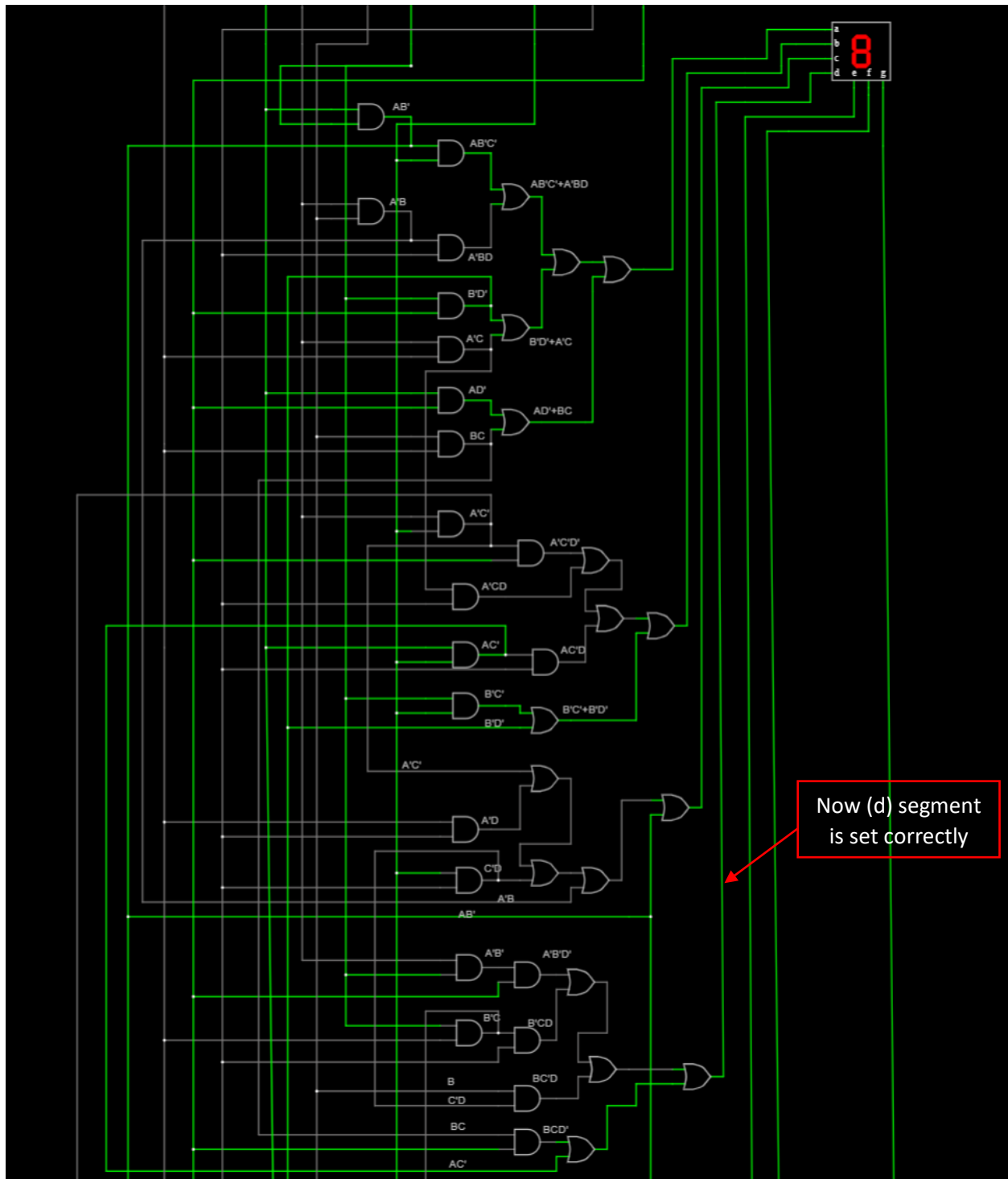
Figure 7: Corrected connection.

Figure 8: Issue fixed.