Information Technology Institute

Track: Digital IC Design

Digital Circuits

Implementation of APB Interface (Master/Slave) Using Combinational and Sequential Logic Circuits

Submitted by:

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1. Introduction

The **Advanced Peripheral Bus (APB)** is a simplified interface used for connecting peripherals to a system in embedded systems, particularly in SoCs (System-on-Chip). It is designed for low-bandwidth, low-latency communication, making it ideal for simpler, slower peripherals such as timers, UARTs, and GPIOs. The APB protocol consists of basic handshaking signals and provides simple, single-cycle access to devices.

The APB bus uses the following primary signals:

- **PADDR**: Address bus.
- **PWDATA**: Write data bus.
- **PRDATA**: Read data bus.
- **PSEL**: Select signal, used to identify which peripheral is being accessed.
- **PWRITE**: Write control signal (indicates write operation).
- **PENABLE**: Enables the transfer cycle.
- **PREADY**: Slave ready signal, indicating the completion of the operation.

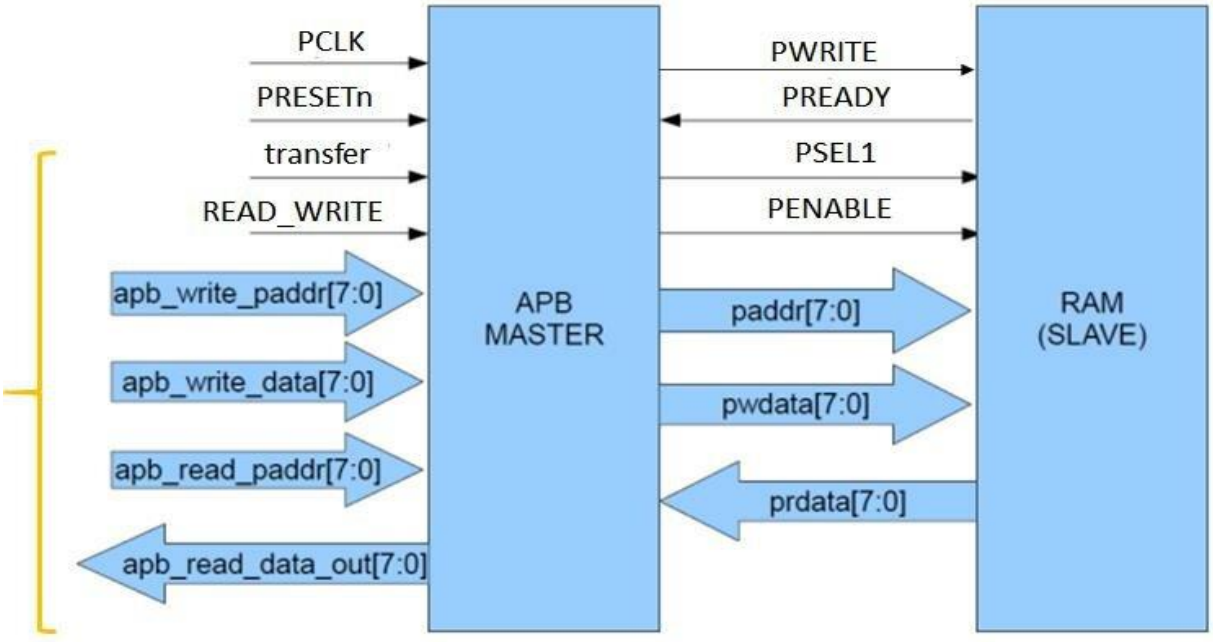

Figure 1:APB Interface.

2. Master Interface

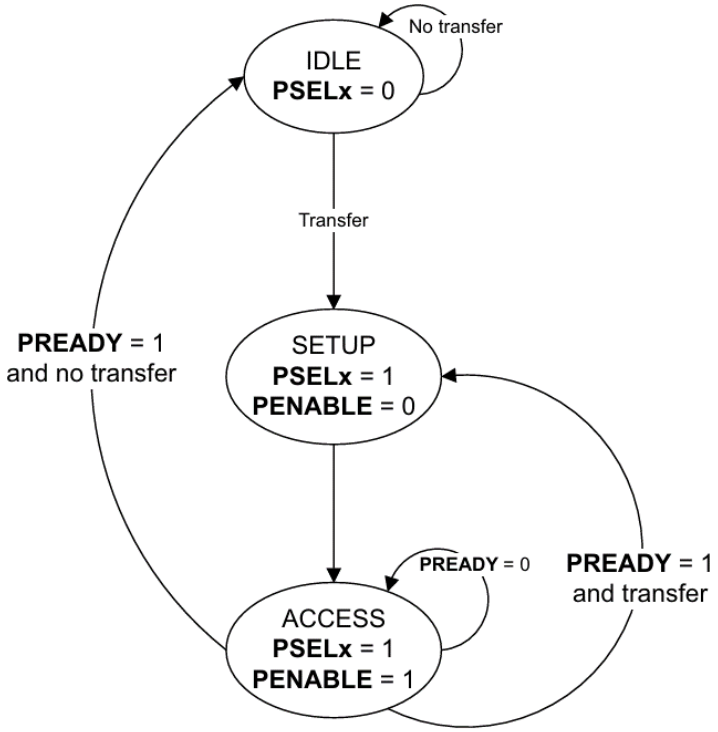

Figure 2: APB Master FSM.

Abstract FSM Truth Table for Master:

Inputs			Current State			Next State		
TRANSFER	PREADY	PRESETn	IDLE	SETUP	ACCESS	IDLE	SETUP	ACCESS
x	x	0	x	x	x	1	0	0
1	x	1	1	0	0	0	1	0
x	x	1	0	1	0	0	0	1
x	0	1	0	0	1	0	0	1
1	1	1	0	0	1	0	1	0
0	1	1	0	0	1	1	0	0

Current State			Output	
IDLE	SETUP	ACCESS	PSELx	PENABLE
1	0	0	0	0
0	1	0	1	0
0	0	1	1	1

1. Full Truth Table for Master Interface:

Term	PRESETn	Trans	Pready	CS_1	CS_0	=>	NS_1	NS_0	PSELx	PENABLE
0	0	0	0	0	0		0	0	0	0
1	0	0	0	0	1		0	0	1	0
2	0	0	0	1	0		0	0	1	1
3	0	0	0	1	1		0	0	0	0
4	0	0	1	0	0		0	0	0	0
5	0	0	1	0	1		0	0	1	0
6	0	0	1	1	0		0	0	1	1
7	0	0	1	1	1		0	0	0	0
8	0	1	0	0	0		0	0	0	0
9	0	1	0	0	1		0	0	1	0
10	0	1	0	1	0		0	0	1	1
11	0	1	0	1	1		0	0	0	0
12	0	1	1	0	0		0	0	0	0
13	0	1	1	0	1		0	0	1	0
14	0	1	1	1	0		0	0	1	1
15	0	1	1	1	1		0	0	0	0
16	1	0	0	0	0		0	0	0	0
17	1	0	0	0	1		1	0	1	0
18	1	0	0	1	0		1	0	1	1
19	1	0	0	1	1		0	0	0	0
20	1	0	1	0	0		0	0	0	0
21	1	0	1	0	1		1	0	1	0
22	1	0	1	1	0		0	0	1	1
23	1	0	1	1	1		0	0	0	0
24	1	1	0	0	0		0	1	0	0
25	1	1	0	0	1		1	0	1	0
26	1	1	0	1	0		1	0	1	1
27	1	1	0	1	1		0	0	0	0
28	1	1	1	0	0		0	0	0	0
29	1	1	1	0	1		1	0	1	0
30	1	1	1	1	0		0	1	1	1
31	1	1	1	1	1		0	0	0	0

2. Boolean Equation for Master Interface:

```
Minimized:
NS_1 = PRESETn CS_1' CS_0 + PRESETn Pready' CS_1 CS_0';
NS_0 = PRESETn Trans Pready CS_1 CS_0' + PRESETn Trans Pready' CS_1' CS_0';
PSELx = CS_1' CS_0 + CS_1 CS_0';
PENABLE = CS_1 CS_0';
```

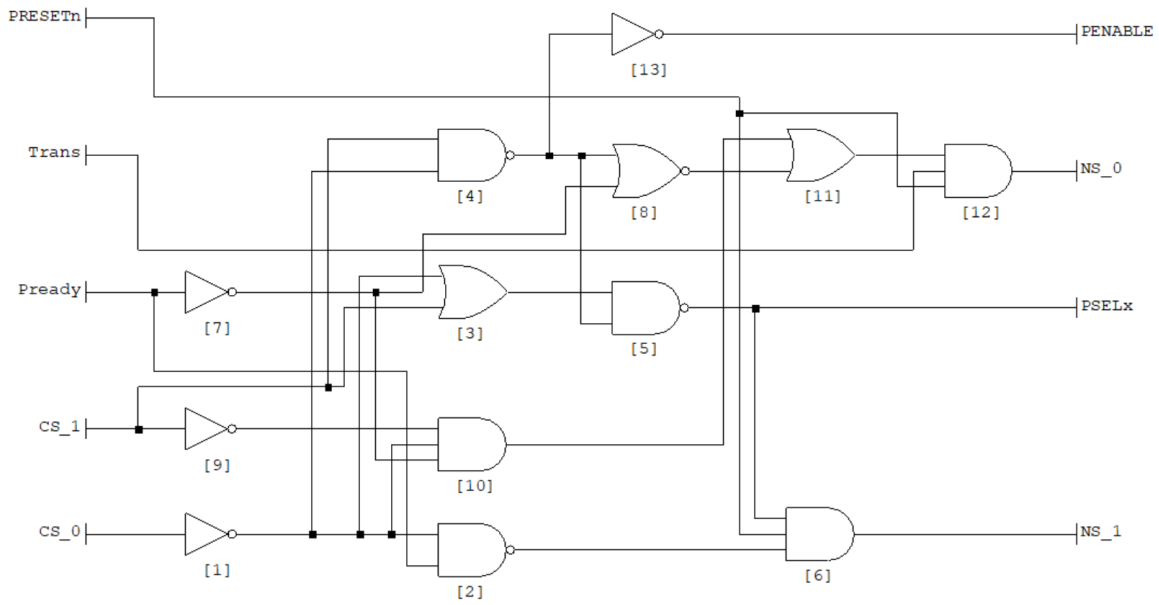

Figure 3: Mapped Gates of Master FSM.

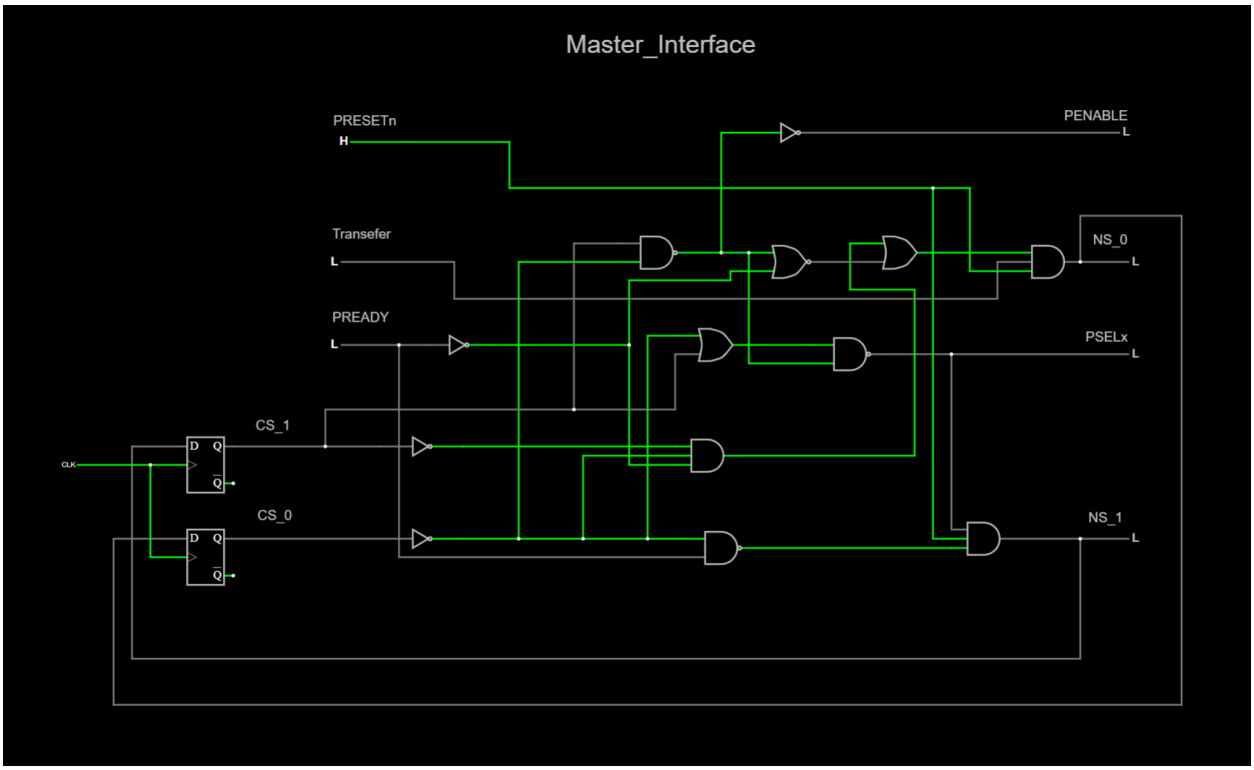

Figure 4: Falstad Design of Master Interface.

3. Slave Interface

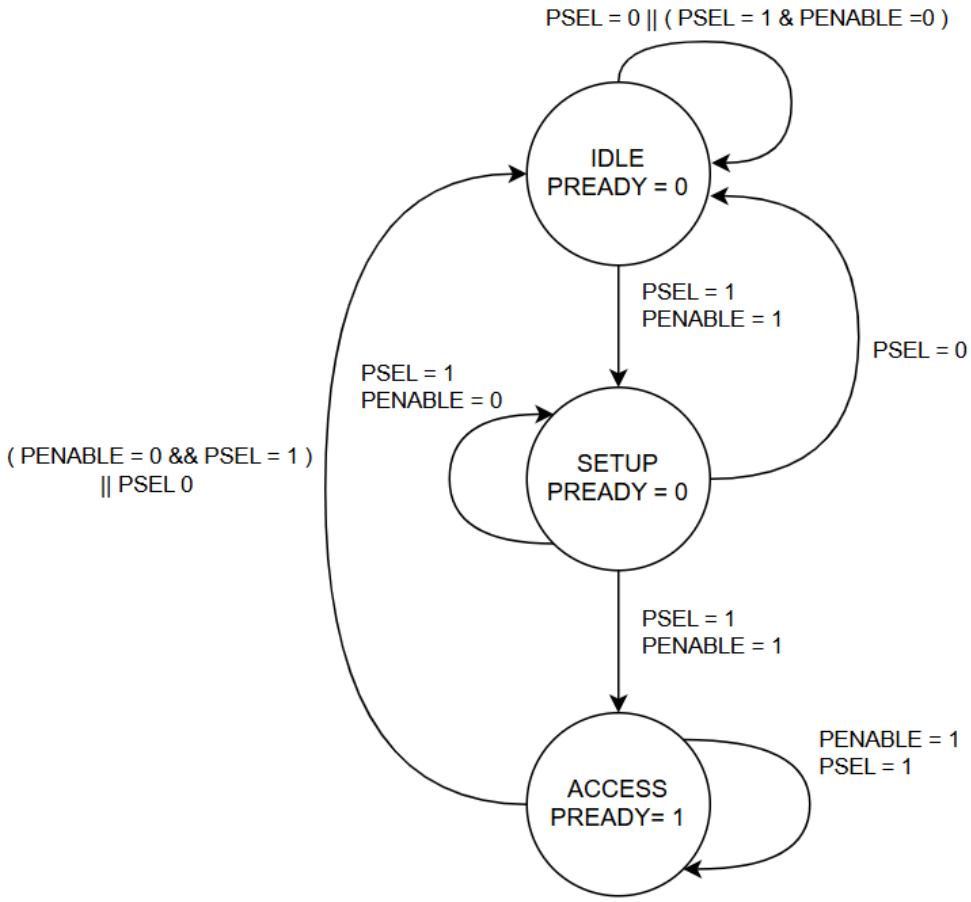

Figure 5: APB Slave FSM.

1. Full Truth Table for Slave Interface:

Term	PENABLE	PSEL	CS_1	CS_0	=>	NS_1	NS_0	PREADY
0	0	0	0	0		0	0	0
1	0	0	0	1		0	0	0
2	0	0	1	0		0	0	1
3	0	0	1	1		0	0	0
4	0	1	0	0		0	0	0
5	0	1	0	1		0	1	0
6	0	1	1	0		0	0	1
7	0	1	1	1		0	0	0
8	1	0	0	0		0	0	0
9	1	0	0	1		0	0	0
10	1	0	1	0		0	0	1
11	1	0	1	1		0	0	0
12	1	1	0	0		0	1	0
13	1	1	0	1		1	0	0
14	1	1	1	0		1	0	1
15	1	1	1	1		0	0	0

2. Boolean Equation for Slave Interface:

```
Minimized:
NS_1 = PENABLE PSEL CS_1' CS_0 + PENABLE PSEL CS_1 CS_0';
NS_0 = PENABLE' PSEL CS_1' CS_0 + PENABLE PSEL CS_1' CS_0';
PREADY = CS_1 CS_0';
```

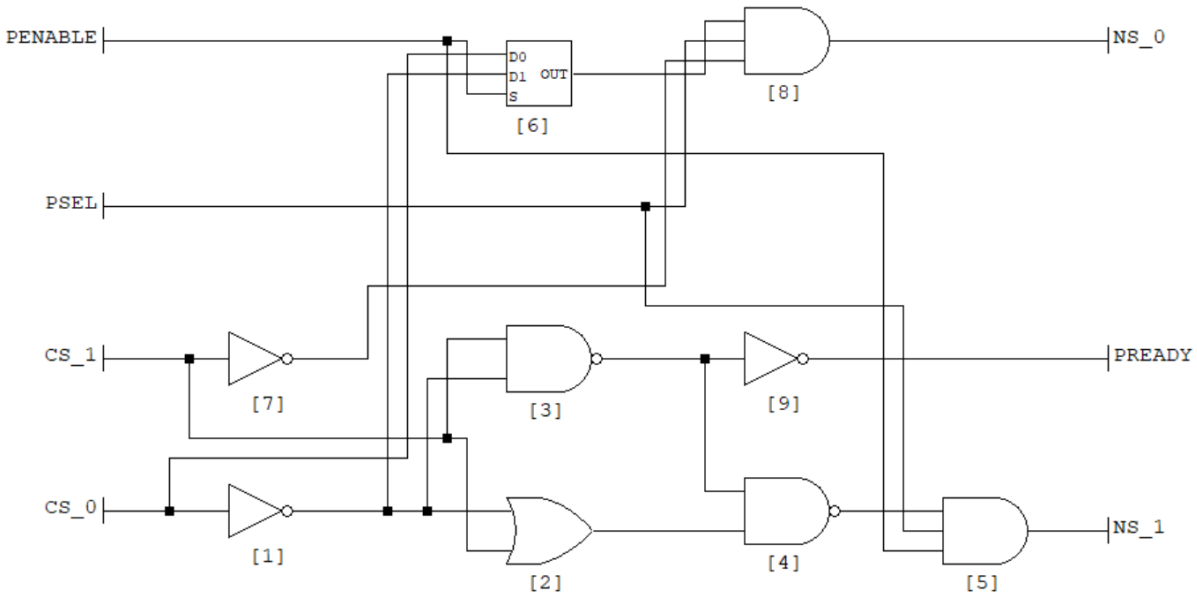

Figure 6: Mapped Gates of Master FSM.

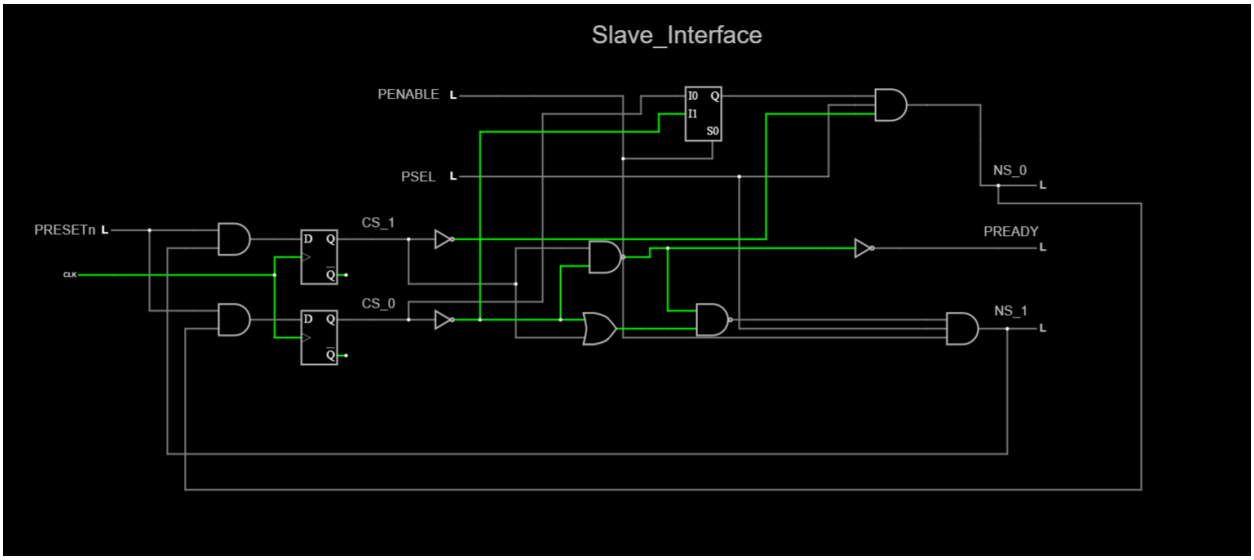

Figure 7: Falstad Design of Slave Interface.

4. APB Protocol

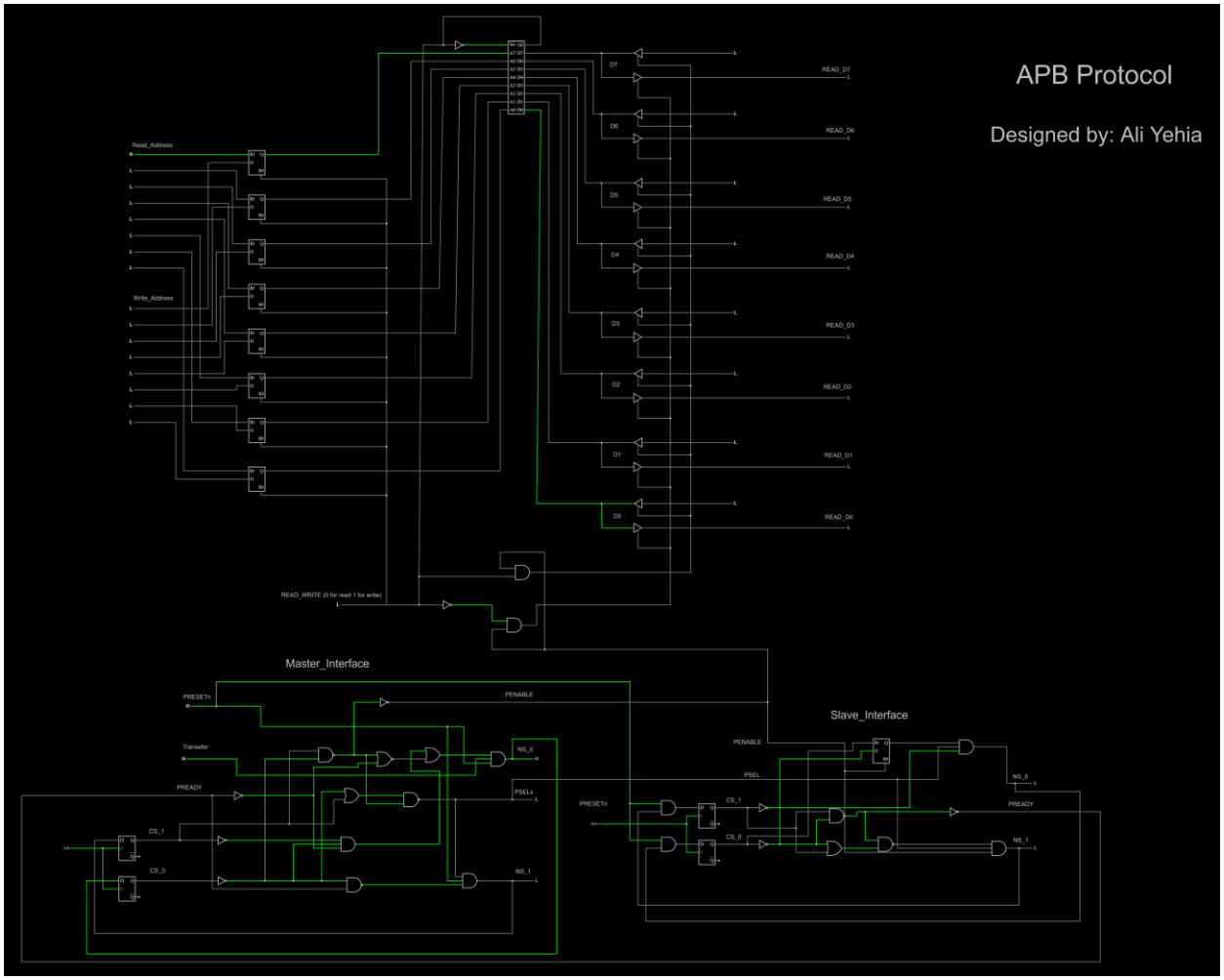

Figure 8: Falstad Design of APB Protocol.

5. State Transitions for Master and Slave:

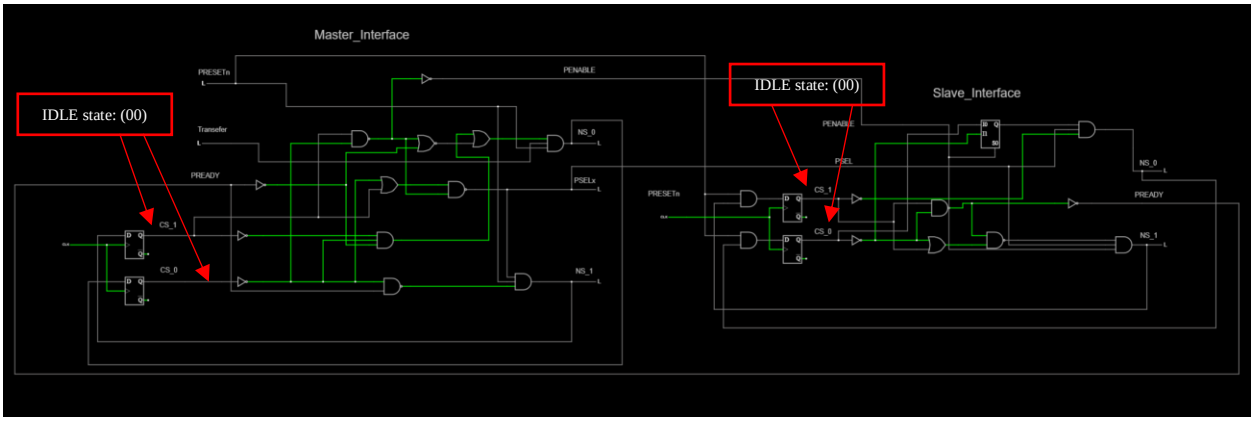

Figure 9: IDLE State for Master and Slave.

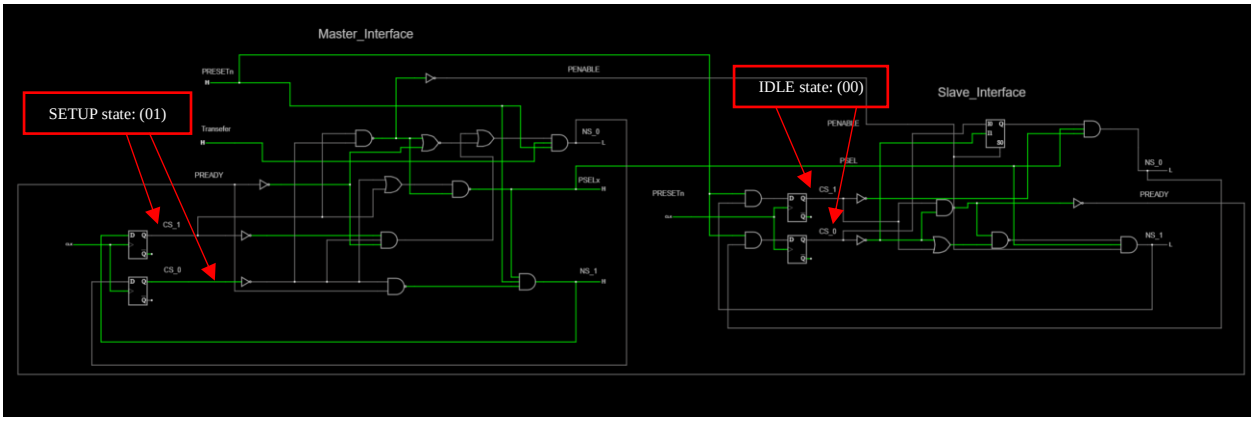

Figure 10: SETUP State for Master.

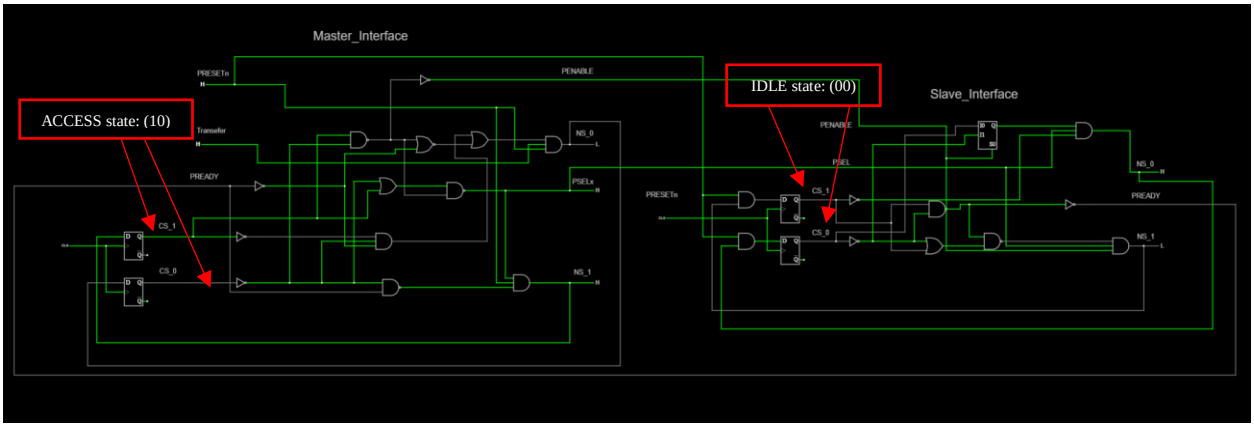

Figure 11: ACCESS State for Master.

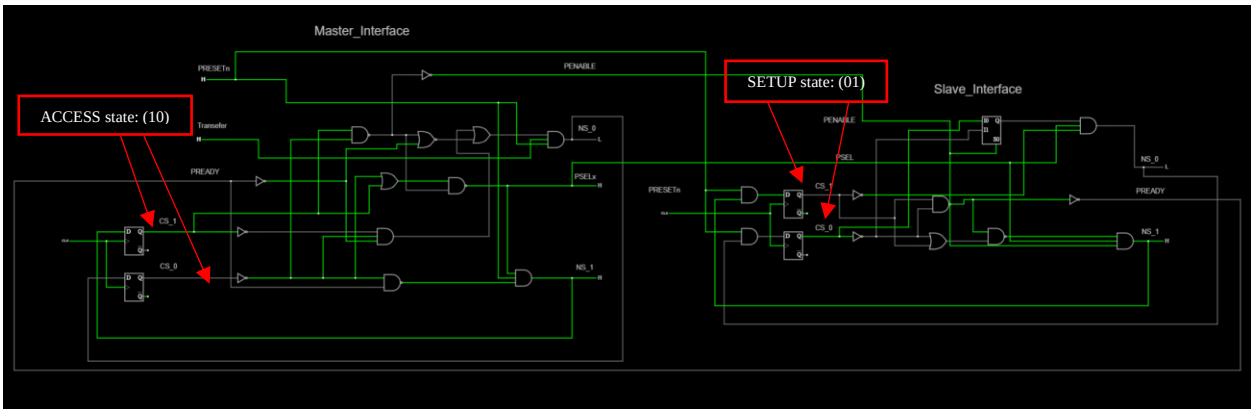

Figure 12: SETUP State for Slave.

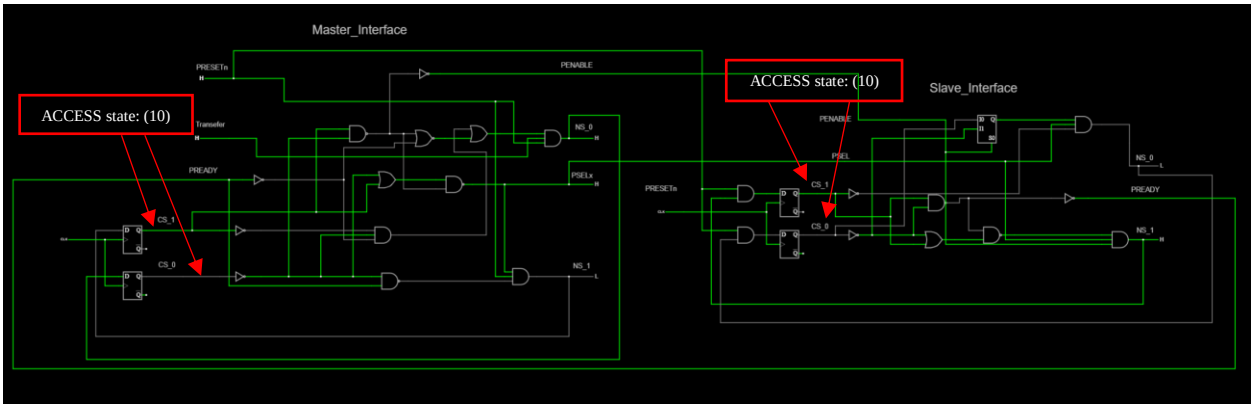

Figure 13: ACCESS State for Slave.

As Long as TRANSEFER Signal is high the Operation continues:

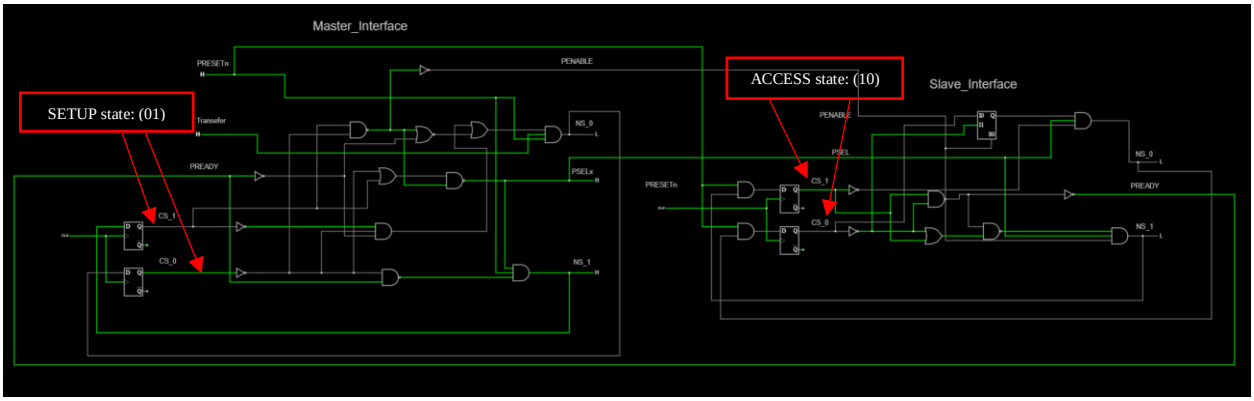

Figure 14: SETUP State for Master and Still ACCESS for Slave.

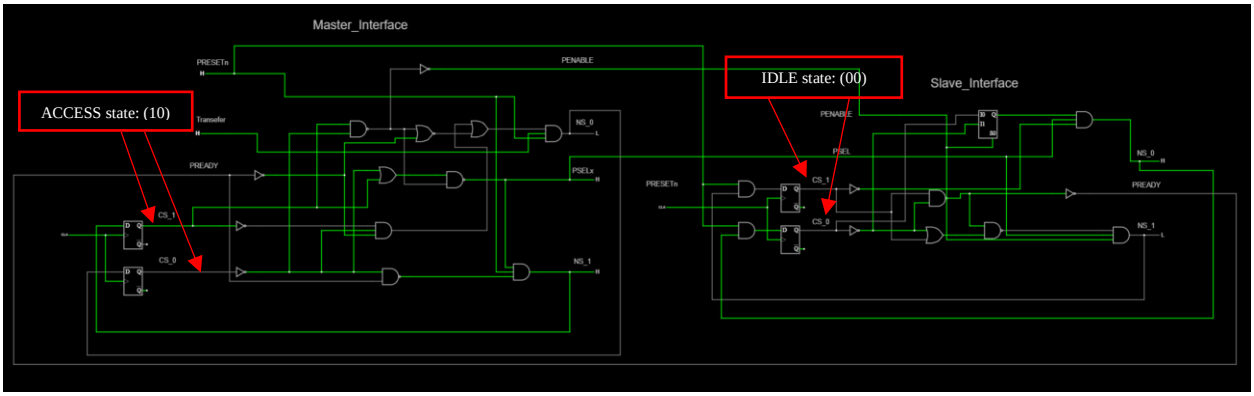

Figure 15: ACCESS State for Master and IDLE State for Slave.

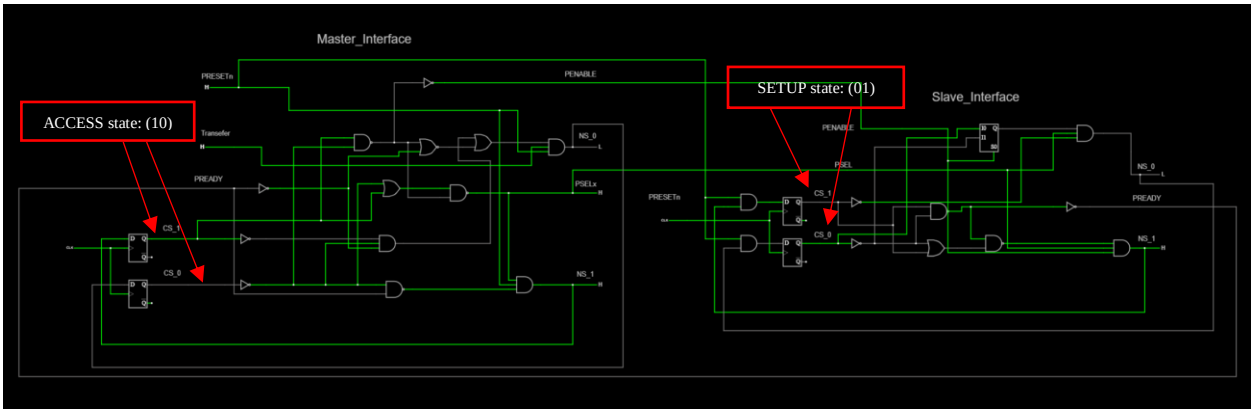

Figure 16: ACCESS State for Master and SETUP State for Slave.

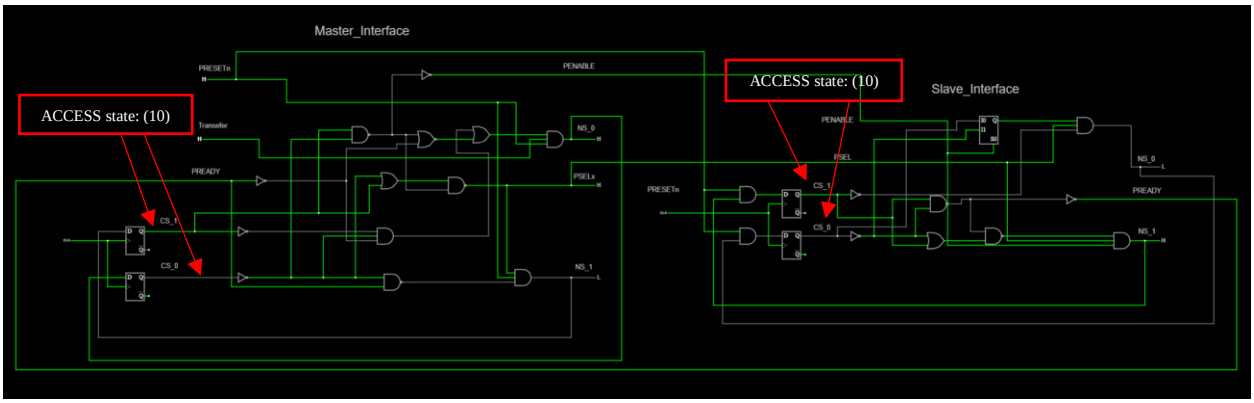

Figure 17: Again, Both Master and Slave in ACCESS State.

6. Write and Read Operation

1. Write Operation

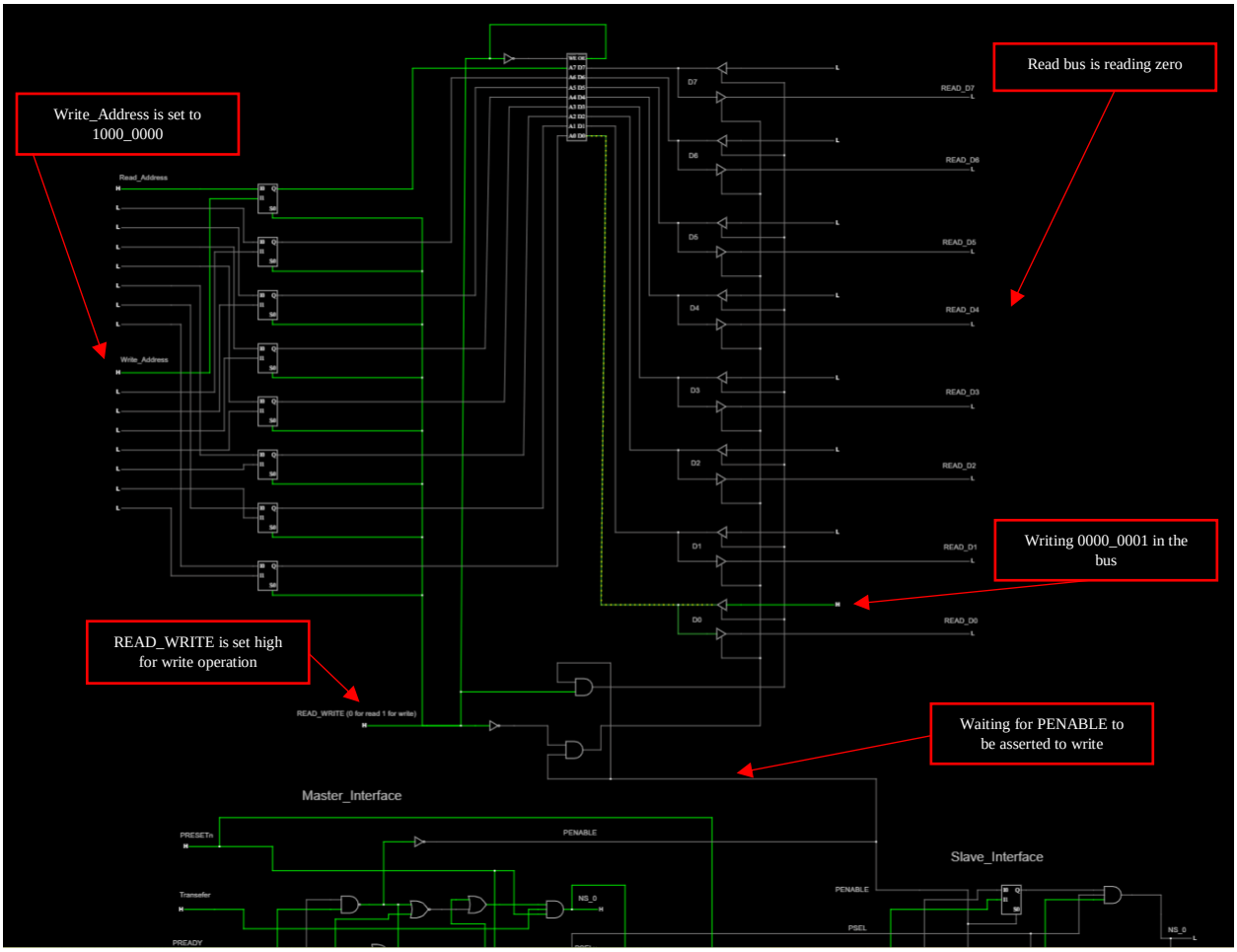

Figure 18: APB Write Operation.

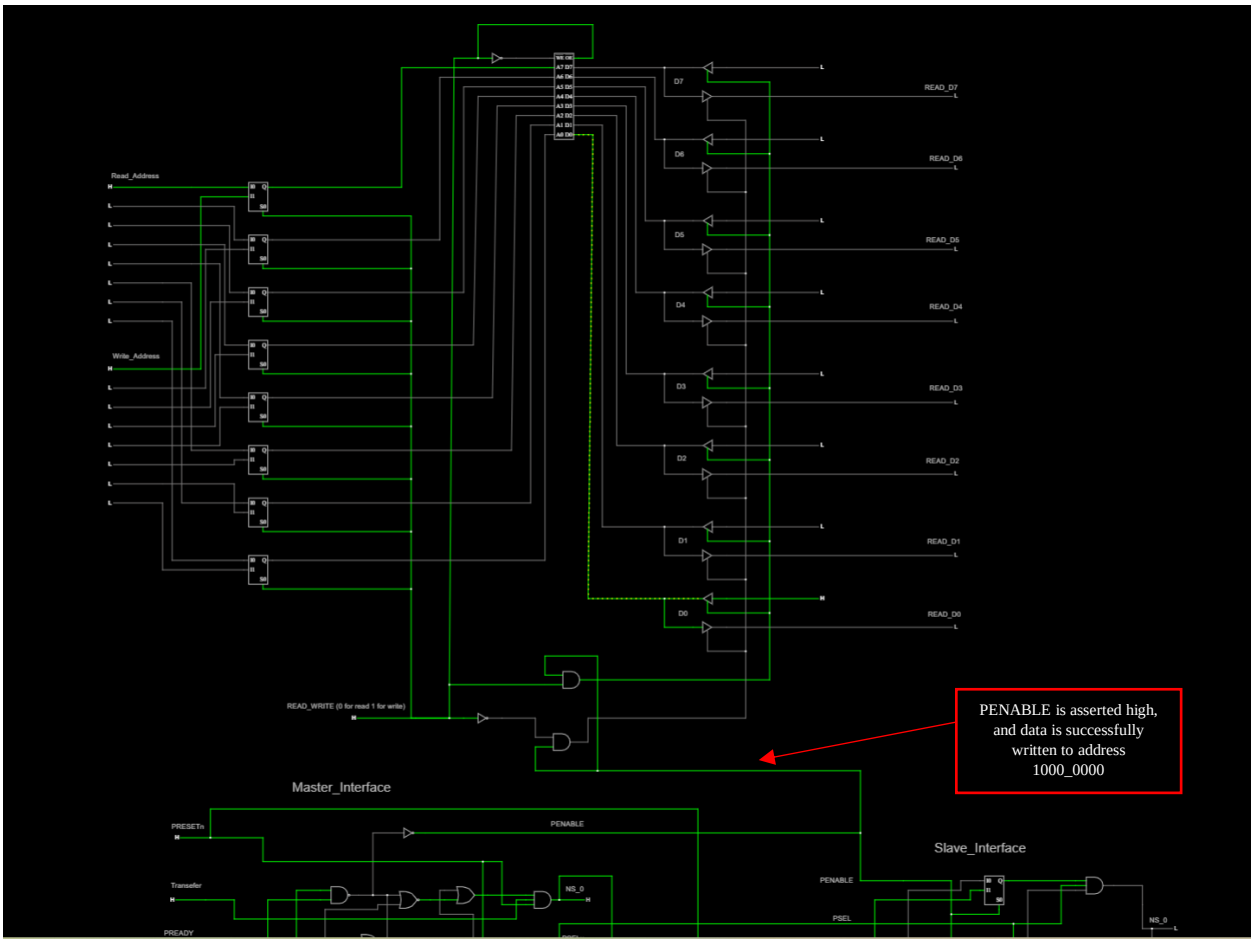

Figure 19: Successful Write Operation.

2. Read Operation

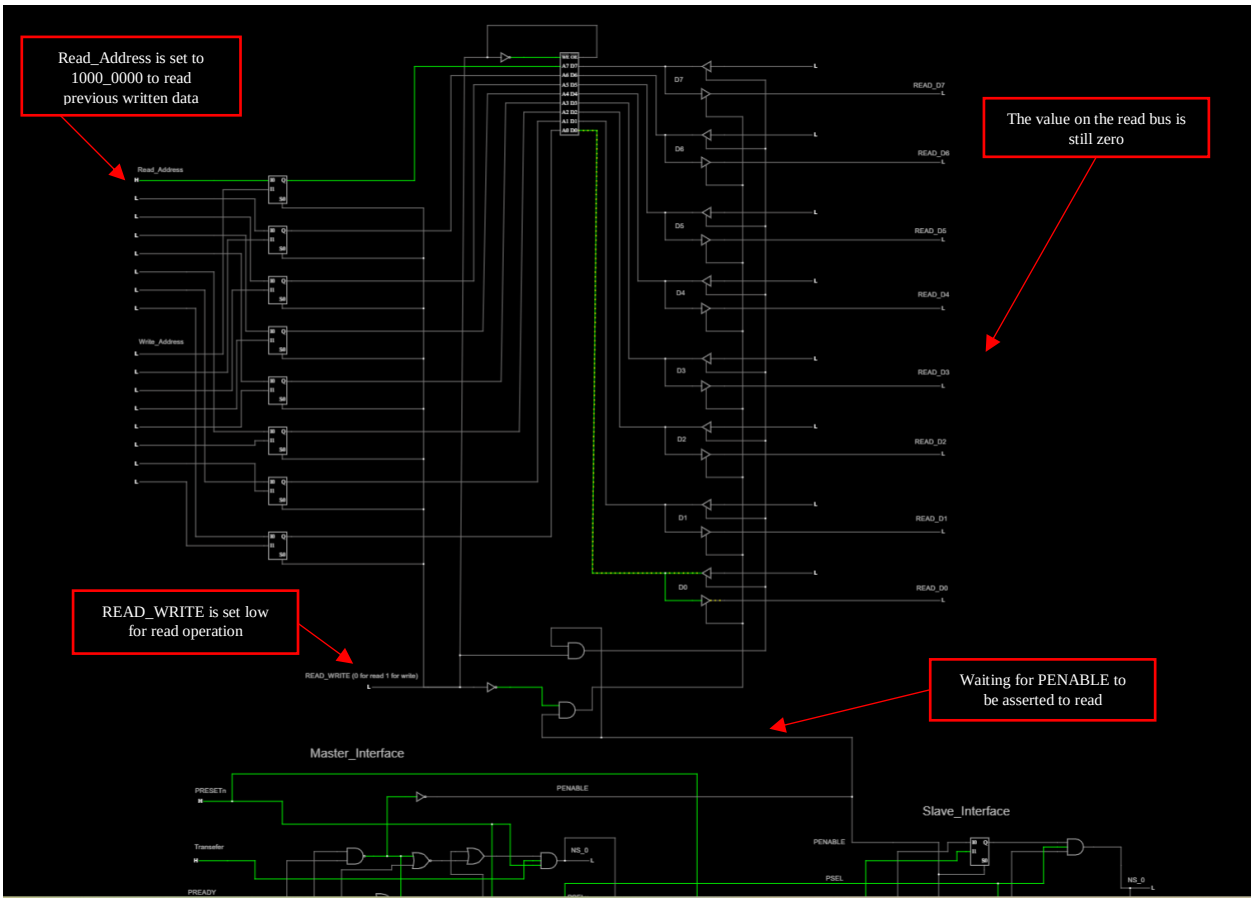

Figure 20: APB Read Operation.

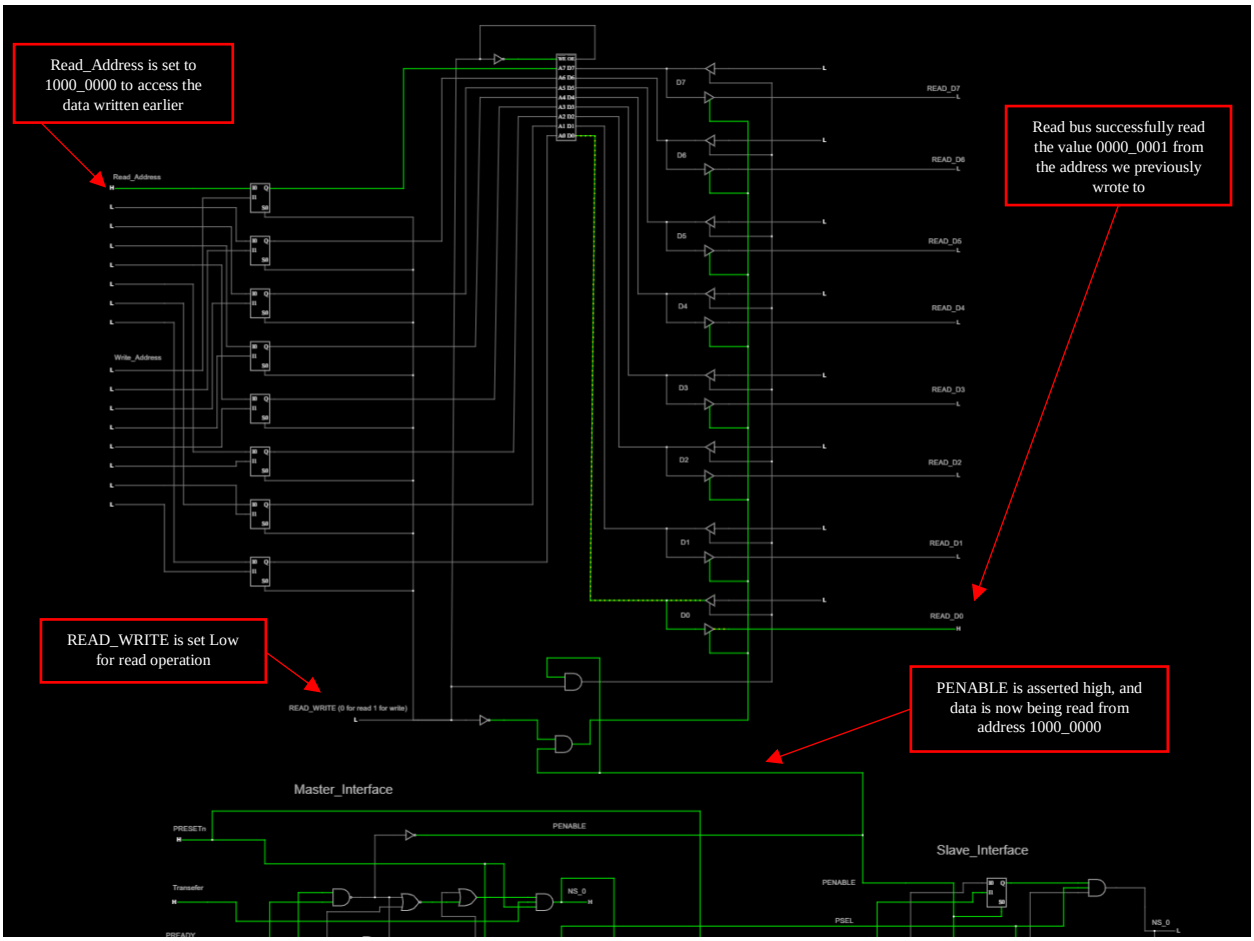

Figure 21: Successful Read Operation.