# C:\Users\aliye\Downloads\pngwing.com.pngInformation Technology Institute

# Digital Circuits

# Lab 1

# Submitted by:

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# Design Report

## Overview of Design

Ring Counter

7-Segment Decoder

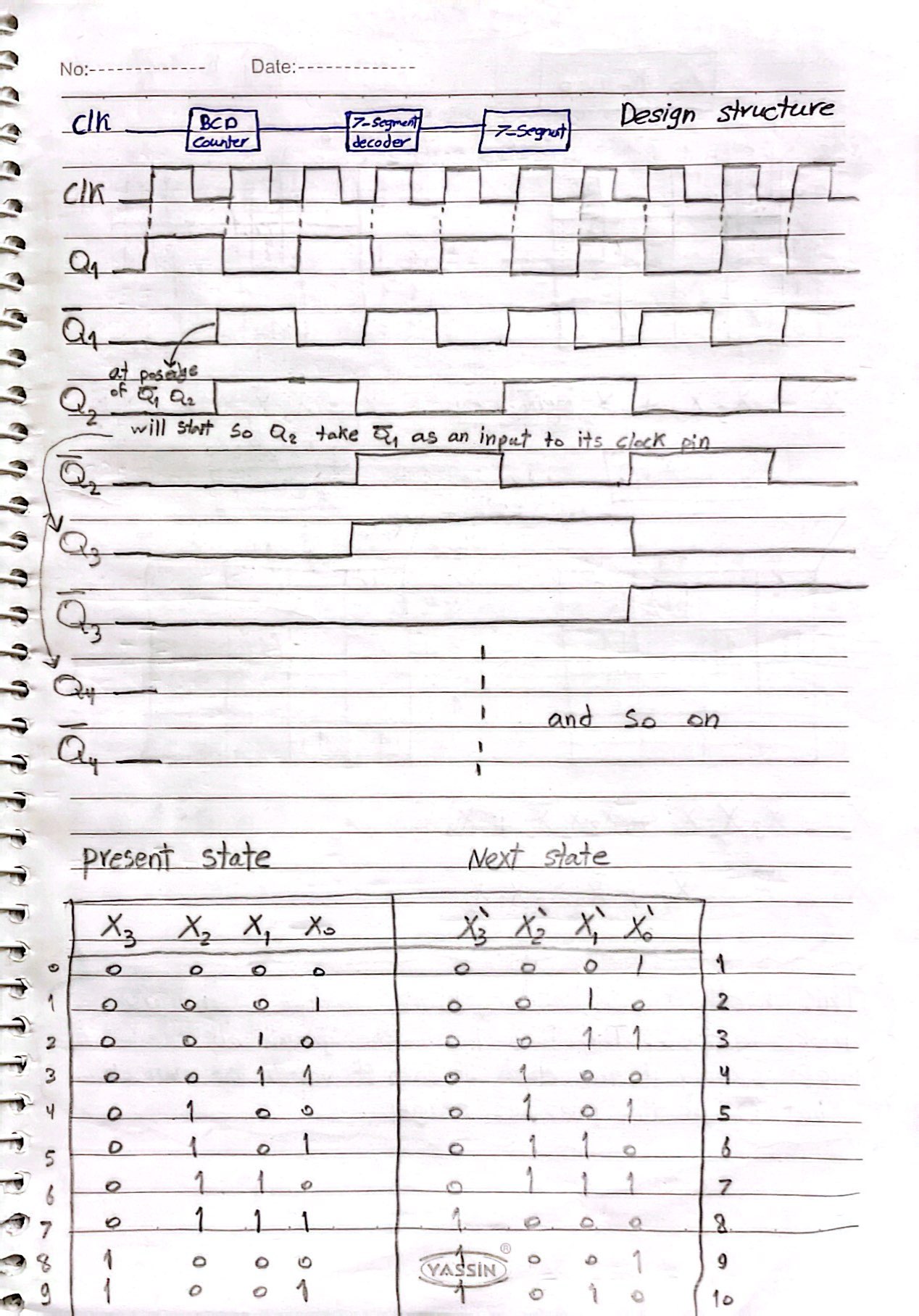
7-Segment Display

**CLK**

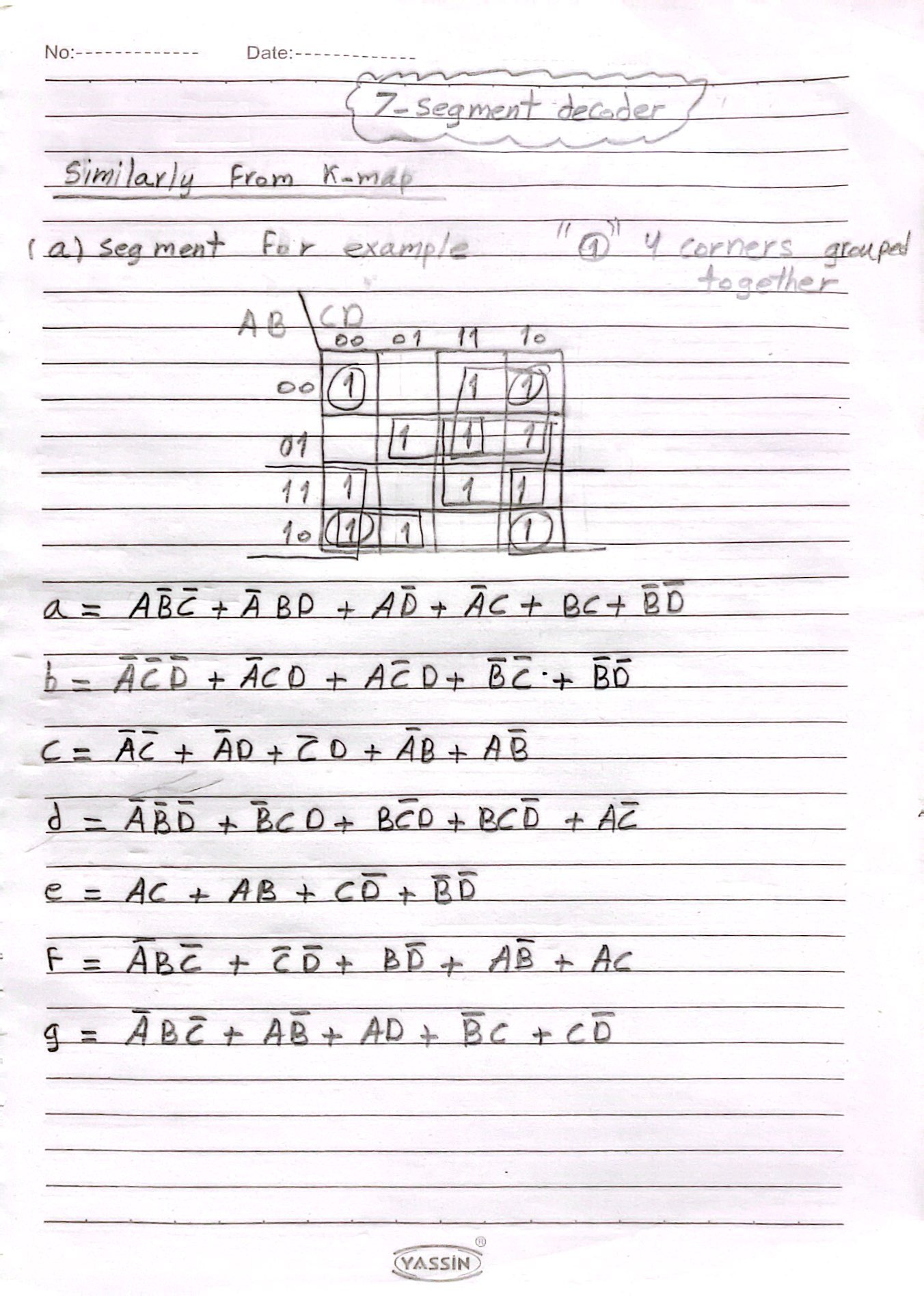
## Components Used

1. D-Flip Flops
2. AND, OR and NOT Gates
3. Input Logic
4. Clock Source
5. 7- Segment Display

## Step-by-step Description of the Design Process







## Screenshots of the Simulation

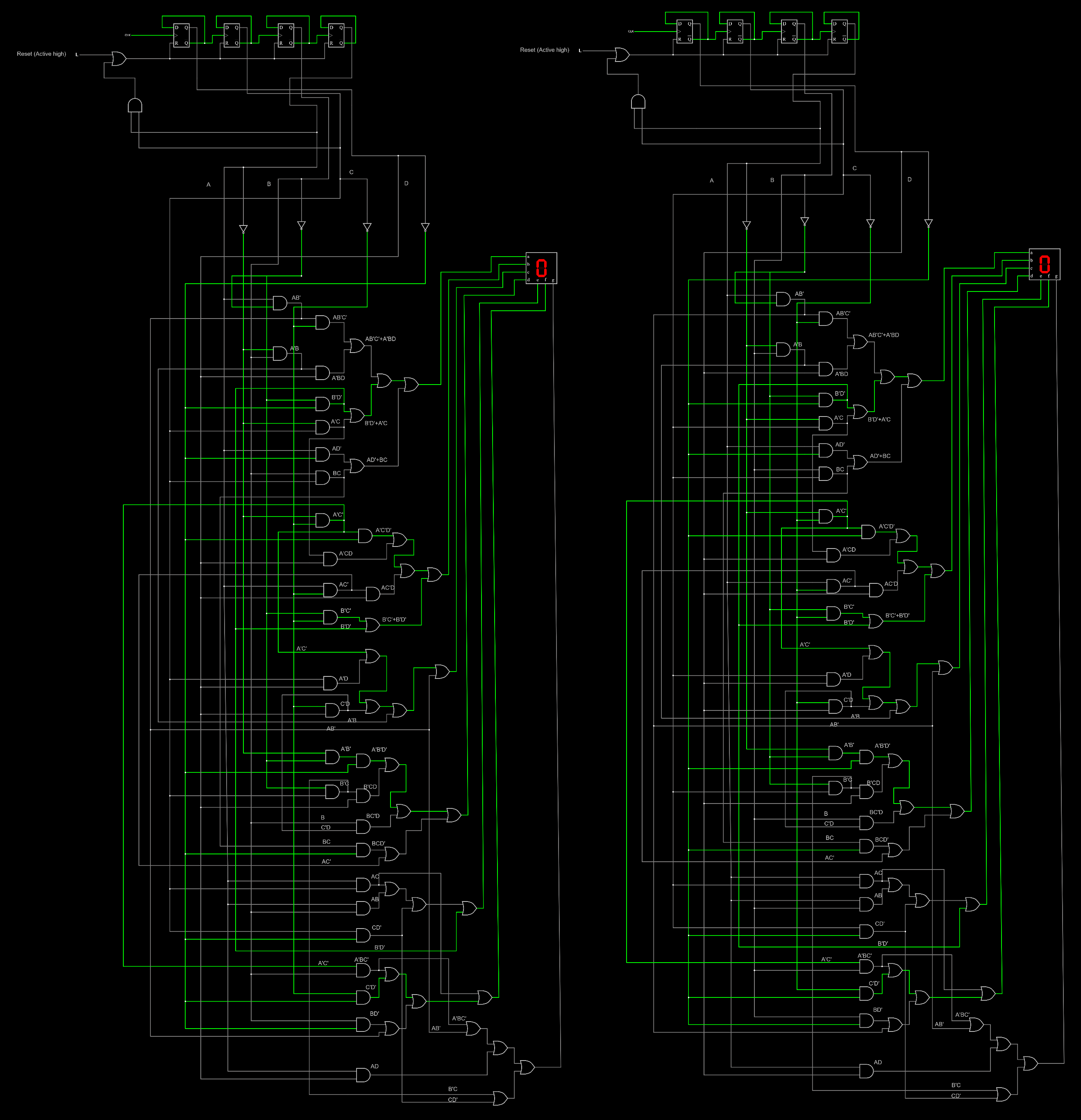


Figure 1: Start of simulation.



Figure 2: Simulation part 1.

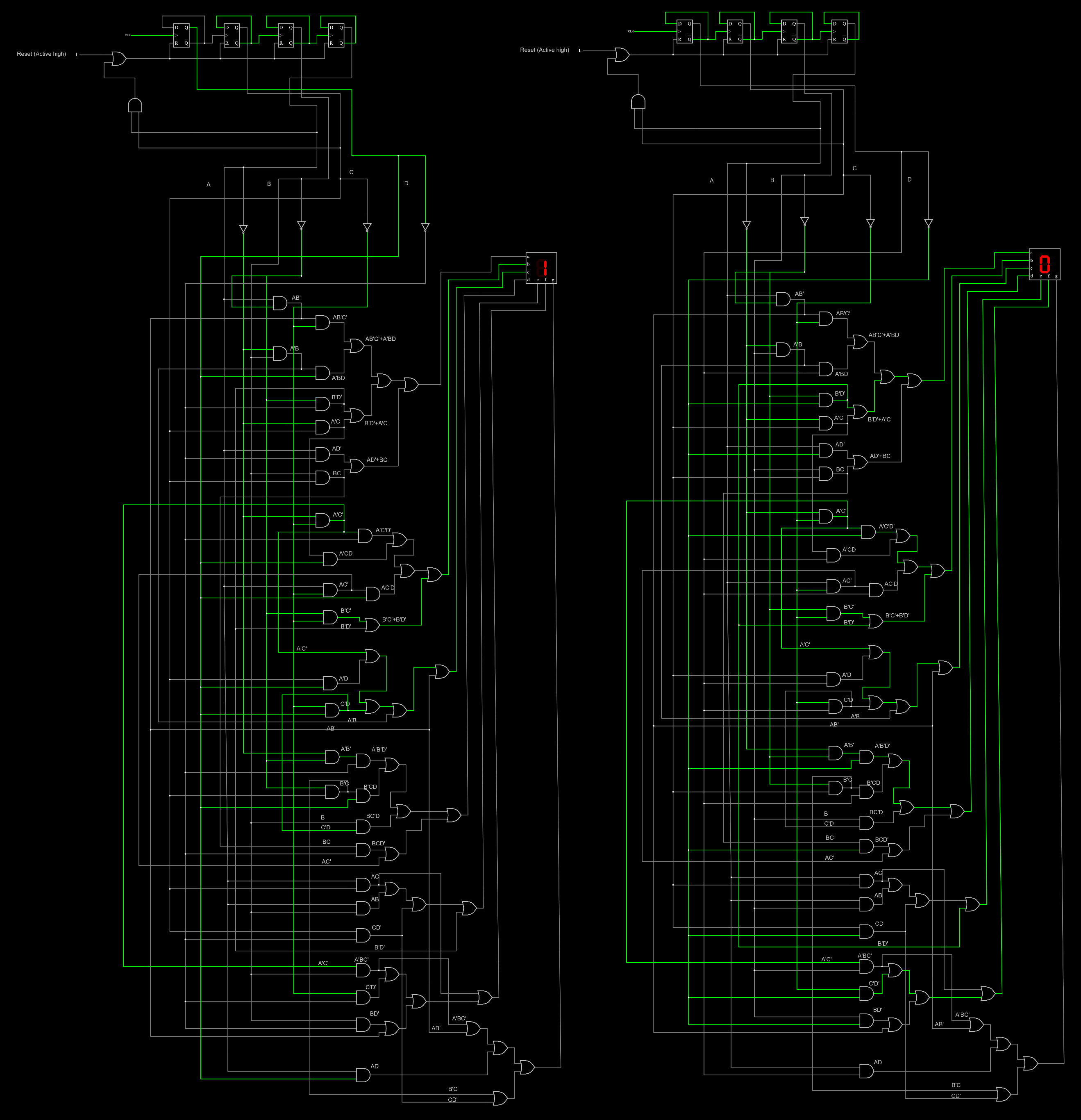


Figure 3: Simulation part 2.

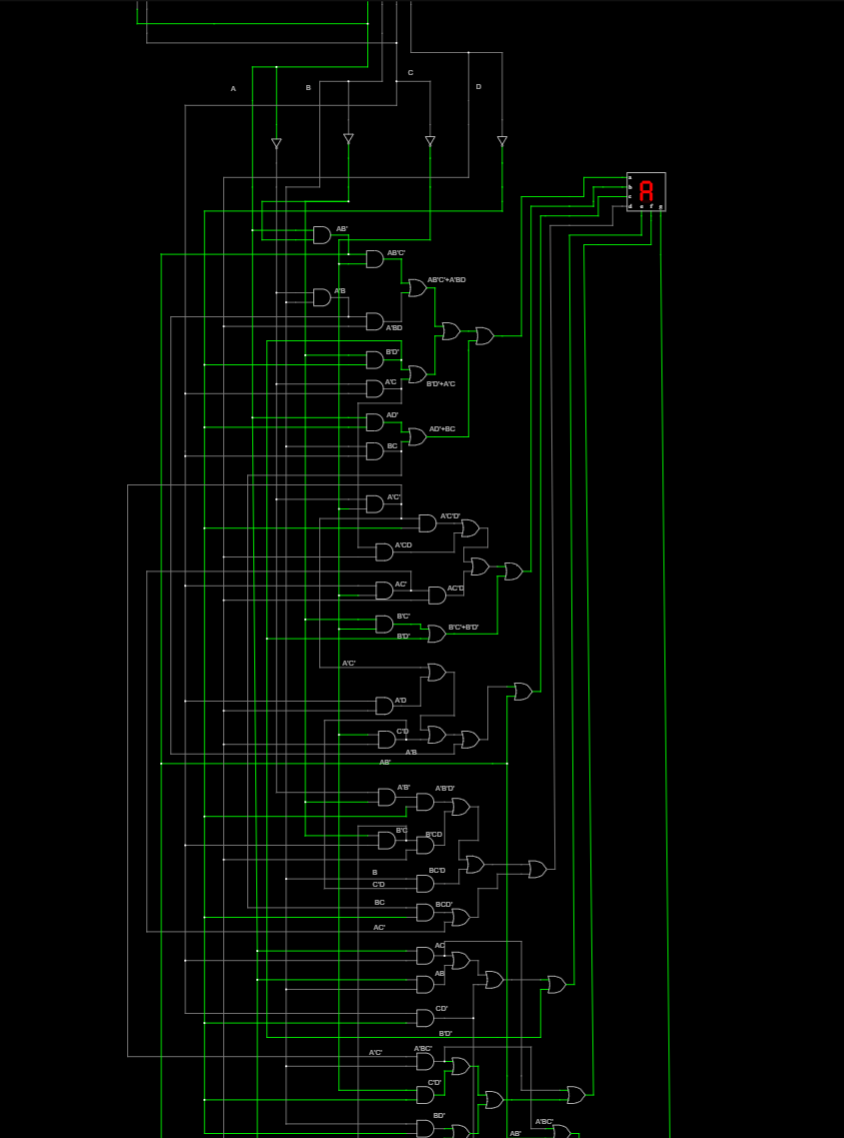


Figure 4: Simulation part 3.

## Issues Faced

Number 8 is not displayed correctly

Figure 5: Number 8 not displayed correctly.



This Node should be High

According to A B C D truth table:

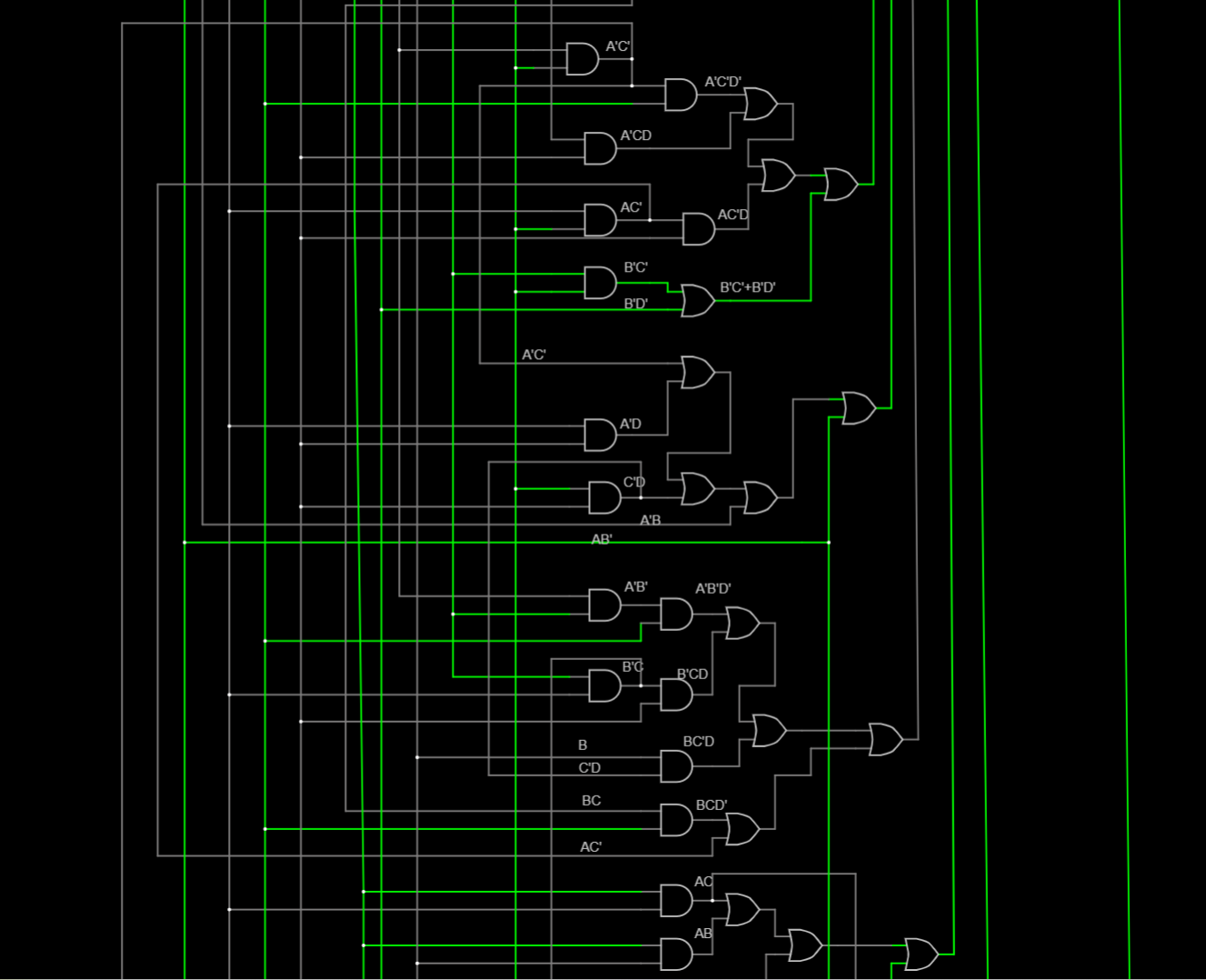
At number 8 I should have A=1, B=0, C=0, D=0 which is AB’C’D’

And (d) segment equation is:

d = A’B’D’ + B’CD + BC’D + BCD’ + AC’

Therefore, the argument that must be high to satisfy the high condition for d segment for number 8 will be AC’ which is part of AB’C’D’ and by checking its node I found out that:

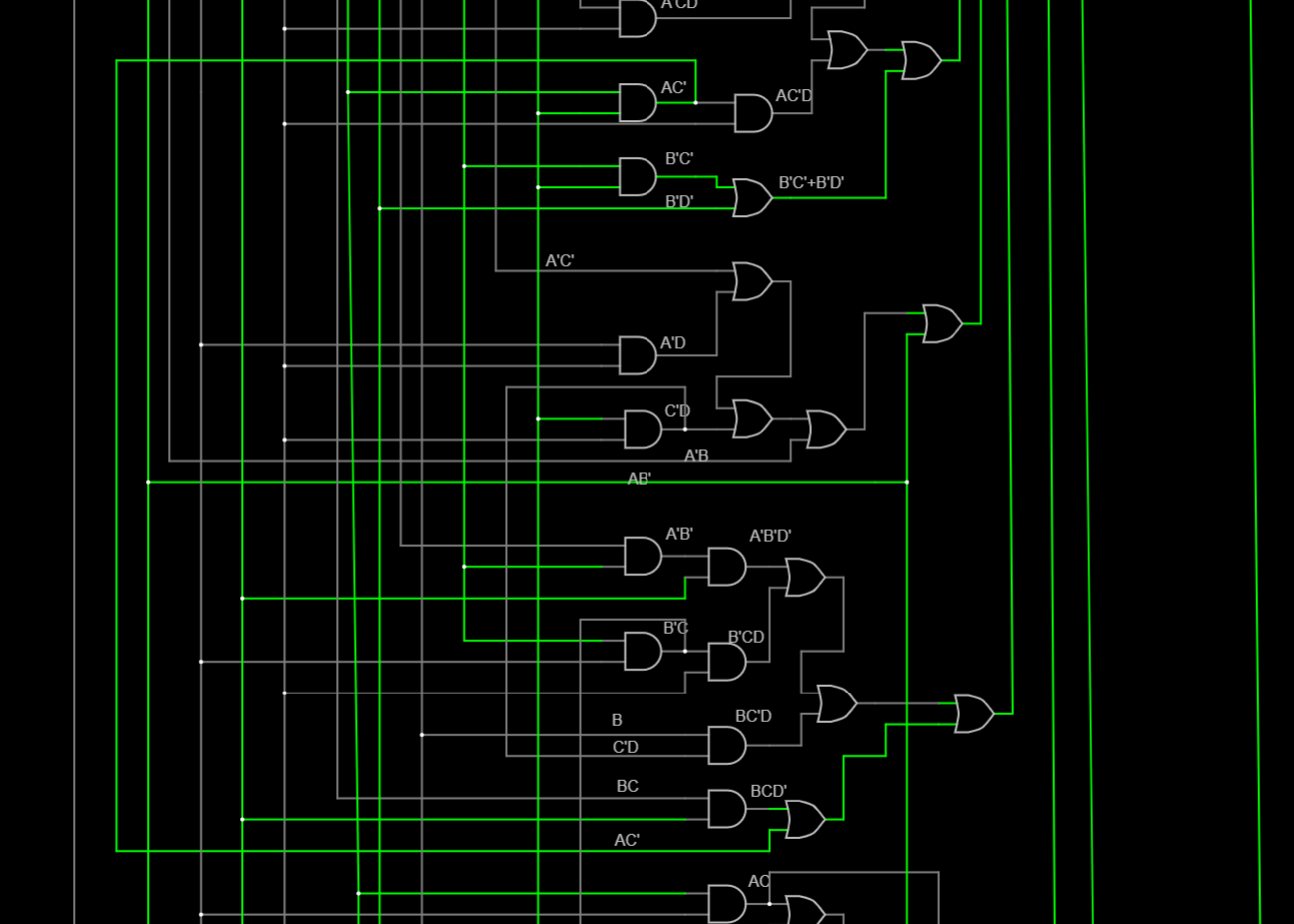
Figure 6: Analyzing and spotting the issue.



A is connected to C node instead of node A

Issue is in here

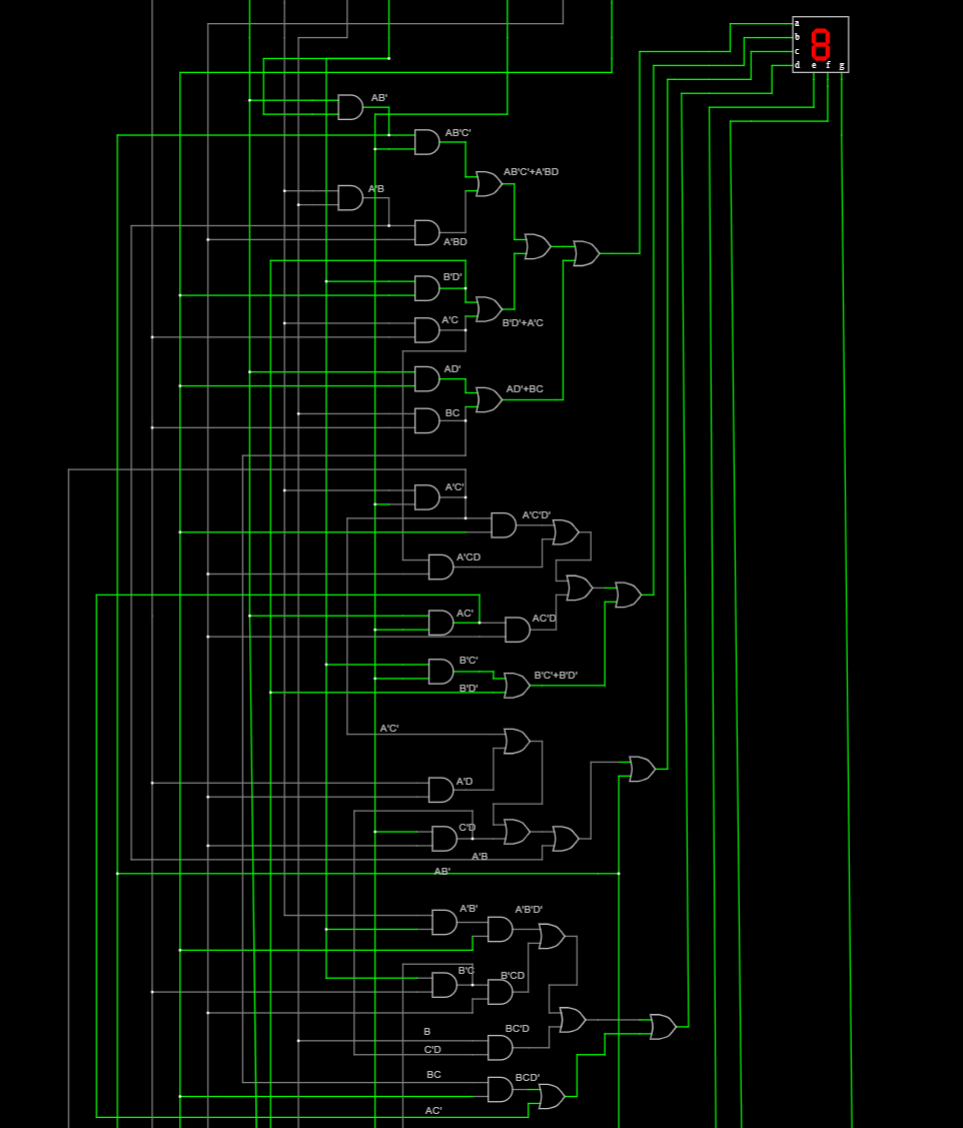
Figure 7: Corrected connection.



Fixed node A connection

AC’ is set to High correctly now

Figure 8: Issue fixed.



Now (d) segment is set correctly