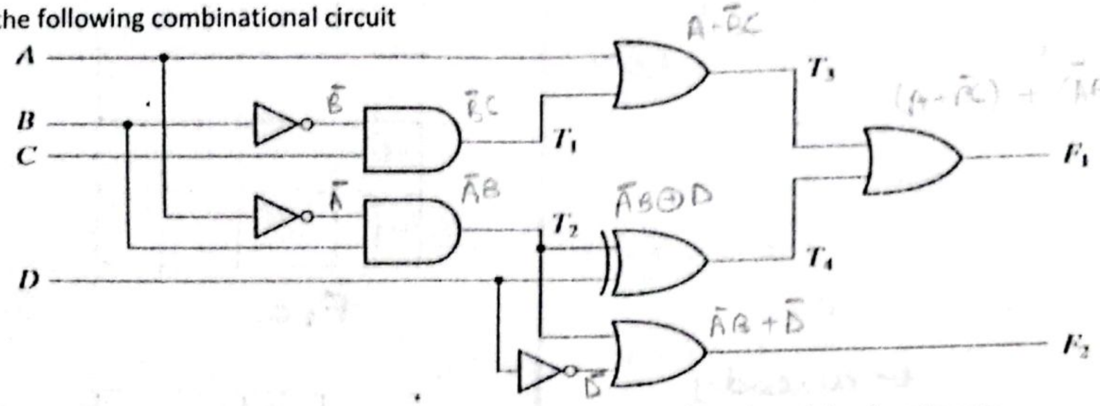
DIGITAL LOGIC & DESIGN (EE-227)
ASSIGNMENT #3

ID: 231-0501 **NAME:** ALIZA YASSER **SECTION:** A

1. Consider the following combinational circuit



a. Derive the Boolean expressions for the outputs **F1** and **F2** as a function of the four inputs.

b. List the truth table with 16 binary combinations of the four input variables. Then list the binary values for **T1** through T4 and outputs **F1** and **F2** in the table.

c. Simplify Boolean expressions of **F1** and **F2** using Boolean algebra and K-maps.

d. List the truth table for simplified expression **F1** and **F2** and compare both truth tables

EXPRESSIONS

$F_1 = (\bar{A} + \bar{B} \cdot C) + ((\bar{A} \cdot B) \oplus D)$, $T_1 = \bar{B} \cdot C$, $T_3 = A + \bar{B} \cdot C$

$F_2 = \bar{A}B + \bar{D}$, $T_2 = \bar{A} \cdot B$, $T_4 = \bar{A}B \oplus D$

TRUTH TABLE

	A	B	C	D	T1	T2	T3	T4	F1	F2
0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	1	1	0
2	0	0	1	0	1	0	1	0	1	1
3	0	0	1	1	1	0	1	1	1	0
4	0	1	0	0	0	1	0	1	1	1
5	0	1	0	1	0	1	0	0	0	1
6	0	1	1	0	0	1	0	1	1	1
7	0	1	1	1	0	1	0	0	0	1
8	1	0	0	0	0	0	1	0	1	1
9	1	0	0	1	0	0	1	1	1	0
10	1	0	1	0	1	0	1	0	1	1
11	1	0	1	1	1	0	1	1	1	0
12	1	1	0	0	0	0	1	0	1	1
13	1	1	0	1	0	0	1	1	1	0
14	1	1	1	0	0	0	1	0	1	1
15	1	1	1	1	0	0	1	1	1	0

SIMPLICATION OF EXPRESSIONS:

$F_1 = A + \bar{B}C + (\bar{A}B \oplus D)$

$= A + \bar{B}C + \bar{A}B\bar{D} + \overline{\bar{A}B}D$

$= A + \bar{B}C + \bar{A}B\bar{D} + (A+\bar{B})D$

$= A + B\bar{D} + \bar{B}C + AD + \bar{B}D$

$= A + AD + B\bar{D} + \bar{B}C + \bar{B}D$

$= A(1+D) + B\bar{D} + \bar{B}D + \bar{B}C$

$F_1 = A + (B \oplus D) + \bar{B}C$

$F_2 = \bar{A}B + \bar{D}$ ← already in simplified form

AB \ CD	00	01	11	10
00		1	1	1
01	1			1
11	1	1	1	1
10	1	1	1	1

$F_1 = A + CD' + B'D + BD'$

AB \ CD	00	01	11	10
00	1			1
01	1	1	1	1
11	1			1
10	1			1

$F_2 = A'B + C'D' + CD'$

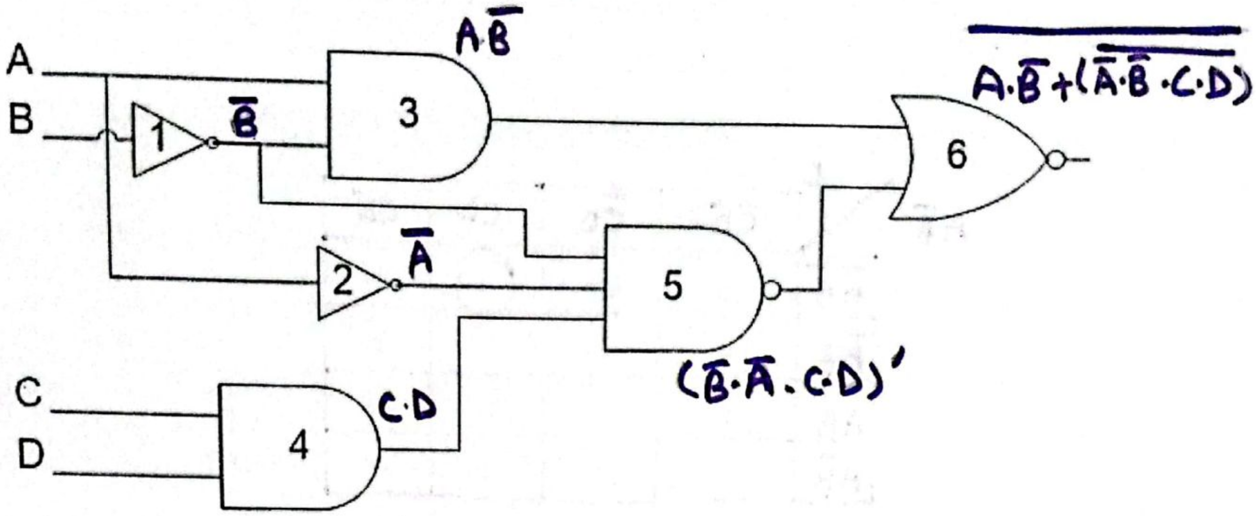
TRUTH TABLE

	A	B	C	D	F1	F2		A	B	C	D	F1	F2
0	0	0	0	0	0	1	8	1	0	0	0	1	1
1	0	0	0	1	1	0	9	1	0	0	1	1	0
2	0	0	1	0	1	1	10	1	0	1	0	1	1
3	0	0	1	1	1	0	11	1	0	1	1	1	0
4	0	1	0	0	1	1	12	1	1	0	0	1	1
5	0	1	0	1	0	1	13	1	1	0	1	1	0
6	0	1	1	0	1	1	14	1	1	1	0	1	1
7	0	1	1	1	0	1	15	1	1	1	1	1	0

COMPARE RESULTS:

By Comparing both the truth tables, we can see that output remains same and simplified expression doesn't change the output.

2. Consider the following combinational circuit



a. Derive the Boolean expressions for the output **F1** as a function of the four inputs.

b. List the truth table with 16 binary combinations of the four input variables. Then list the binary values output **F1** in the table.

c. Simplify Boolean expressions of **F1** using Boolean algebra and K-maps.

d. List the truth table for simplified expression **F1** and compare both truth tables.

EXPRESSION

$$F_1 = \overline{(A\cdot\bar{B}) + (\overline{\bar{A}\cdot\bar{B}\cdot(C\cdot D)})}$$

Simplification: $= (A B')' \cdot ((A'B'CD)')'$

$= (\bar{A} + \bar{\bar{B}}) \cdot (\bar{A}B'CD)$

$= (\bar{A}+B) \cdot (\bar{A}\bar{B}CD) = \bar{A}\bar{A}\bar{B}CD + B\bar{A}\bar{B}CD = \bar{A}\bar{B}CD + 0 = \bar{A}\bar{B}CD$

TRUTH TABLE

	A	B	C	D	F1	F_1 Simplified		A	B	C	D	F1	F_1 Simplified
0	0	0	0	0	0	0	8	1	0	0	0	0	0
1	0	0	0	1	0	0	9	1	0	0	1	0	0
2	0	0	1	0	0	0	10	1	0	1	0	0	0
3	0	0	1	1	1	1	11	1	0	1	1	0	0
4	0	1	0	0	0	0	12	1	1	0	0	0	0
5	0	1	0	1	0	0	13	1	1	0	1	0	0
6	0	1	1	0	0	0	14	1	1	1	0	0	0
7	0	1	1	1	0	0	15	1	1	1	1	0	0

SIMPLICATION OF EXPRESSION:

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	0
$\bar{A}B$	0	0	0	0
AB	0	0	0	0
$A\bar{B}$	0	0	0	0

From K.Map :- $F_1 = \bar{A}\bar{B}CD$

TRUTH TABLE

→ KMap

	A	B	C	D	F1
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

COMPARE RESULTS:

Comparing both truth tables gives the same answers as simplifying an expression has no effect on output.

3. Design a combinational circuit that converts a **three-bit Binary number** to a **3-bit Gray code.**

NOTE: Implement the circuit with exclusive-OR gates.

TABLE

	BINARY			GRAY CODE		
	A (B_2)	B (B_1)	C (B_0)	G2	G1	G0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	~~0~~ 1
7	1	1	1	1	0	0

SIMPLIFICATION:

For G_2:-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	0	0
A	1	1	1	1

$= A$

For G_1:-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	1	1
A	1	1	0	0

$= A\bar{B} + \bar{A}B$

$= A \oplus B$

For G_0:-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	0	1
A	0	1	0	1

$= B\bar{C} + \bar{B}C$

$= B \oplus C$

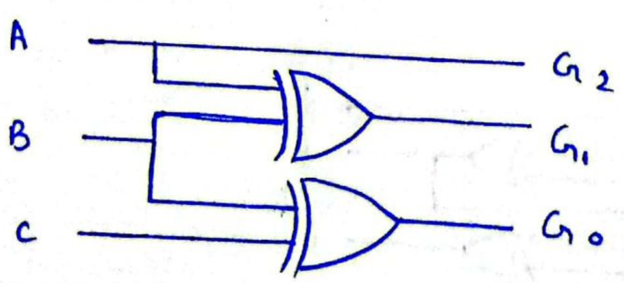
EXPRESSIONS:

$G_2 = \Sigma(4,5,6,7) = A$

$G_1 = \Sigma(2,3,4,5) = A \oplus B$

$G_0 = \Sigma(1,2,5,6) = B \oplus C$

Circuit :-



4. Design a combinational circuit that converts a **3-bit Gray code** to a three-bit Binary number.
NOTE: Implement the circuit with exclusive-OR gates.

TABLE

	GRAY CODE			BINARY		
	G2	G1	G0	A	B	C
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	1	0	1	0
3	0	1	0	0	1	1
4	1	1	0	1	0	0
5	1	1	1	1	0	1
6	1	0	1	1	1	0
7	1	0	0	1	1	1

SIMPLIFICATION:

For B_2:

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	0	0
A	1	1	1	1

$A = G_2$

For B_1:

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	1	1
A	1	1	0	0

$B = G_0 \oplus G_1$

For B_0:

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	0	1
A	1	0	1	0

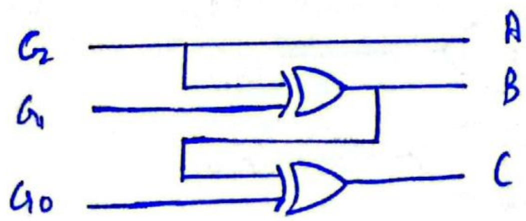
$C = G_2 \oplus (G_0 \oplus G_1)$

EXPRESSIONS:

$A = B_2 = G_2$

$B = B_1 = G_0 \oplus G_1$

$C = B_0 = G_2 \oplus G_0 \oplus G_1$



5. Design a combinational circuit that converts a bit four binary number to a four-bit Gray code.

	BINARY				GRAY CODE			
	A (B_3)	B (B_2)	C (B_1)	D (B_0)	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

SIMPLIFICATION:

For G_3:

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$= A$

For G_2:

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$= \bar{A}B + A\bar{B}$

$= A \oplus B$

For G_1:

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

$= \bar{B}C + B\bar{C}$

$= B \oplus C$

For G_0:

AB \ CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$= \bar{C}D + C\bar{D}$

$= C \oplus D$

EXPRESSIONS:

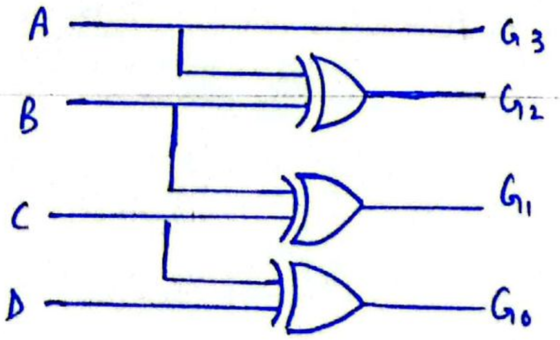
$G_3 = B_3 = A$

$G_2 = B_2 \oplus B_3 = A \oplus B$

$G_1 = B_1 \oplus B_2 = B \oplus C$

$G_0 = B_1 \oplus B_0 = C \oplus D$

Circuit:-



ASSIGNMENT # 3 [EE-227]

6. Design a combinational circuit that converts a BCD to an **8,4, -2, -1** code.

	BCD CODE				8,4, -2, -1 CODE			
					w	x	y	3
	A	B	C	D	8	4	-2	-1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	0	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	1	1	1
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	0	1	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	1	1	0	0
14	1	1	1	0	1	1	0	1
15	1	1	1	1	1	1	1	0

SIMPLIFICATION:

-2

AB \ CD	00	01	11	10
00		1		1
01		1		1
11	X	X	X	X
10		1	X	X

$y = \bar{C}D + C\bar{D}$

$= C \oplus D$

4

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	X	X	X	X
10		1	X	X

$x : B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$

8

AB \ CD	00	01	11	10
00				
01		1	1	1
11	X	X	X	X
10	1	1	X	X

$w : A + BD + BC$

-1

AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10		1	X	X

$z = D$

EXPRESSIONS:

$8 : A + BD + BC$

$4 : B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$

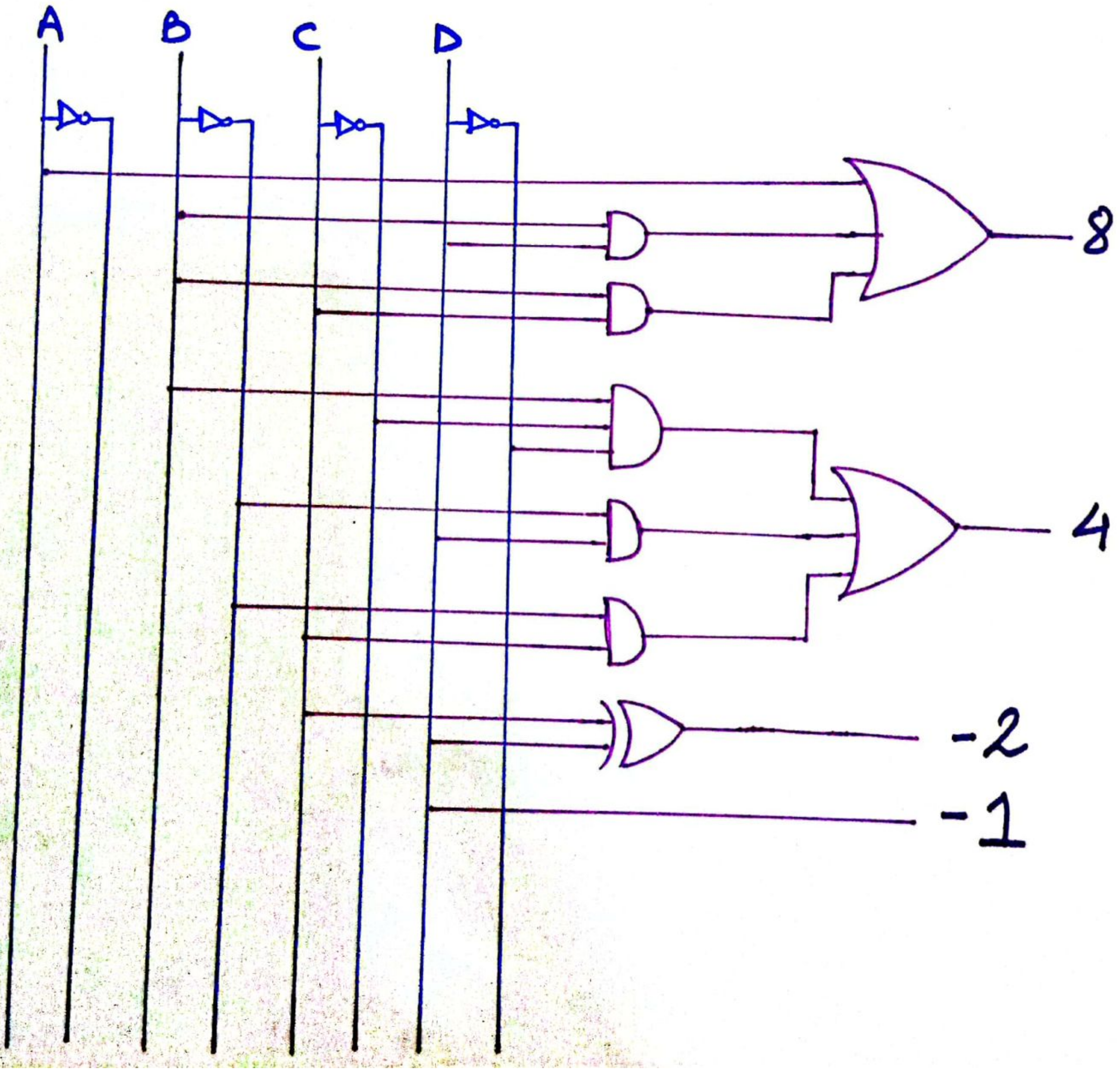
$-2 : \bar{C}D + C\bar{D} = C \oplus D$

$-1 : D$

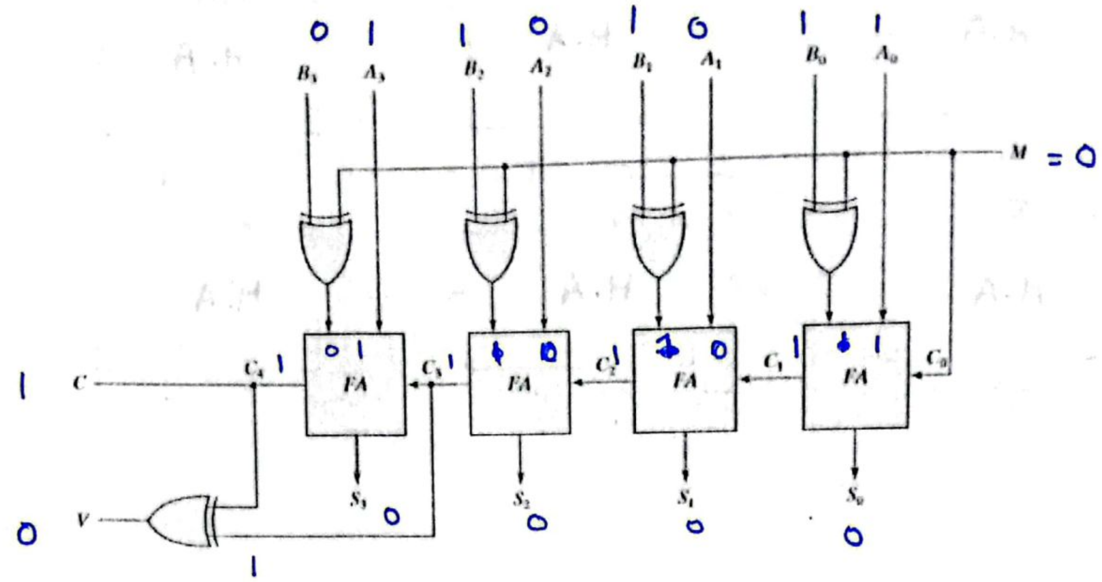
6. Design a combinational circuit that converts a BCD to an **8.4. -2. -1** code.

1

Circuit :



9. Perform unsigned Addition **A+B** where A= 9 and B= 7 using Following is **4-adder/subtractor** circuit? Also write short note on working of **C** and **V** bits for signed and unsigned addition/subtraction



A = 9 = 1001

B = 7 = 0111

A + B = 10000 = 16

There are cases:

if $V = C_4 \oplus C_3 = 1 \oplus 1 = 0$ then it means addition has been performed

if '0' is carried in '1' carried out in most significant bit means addition of negative numbers has been performed. The result will be non-negative.

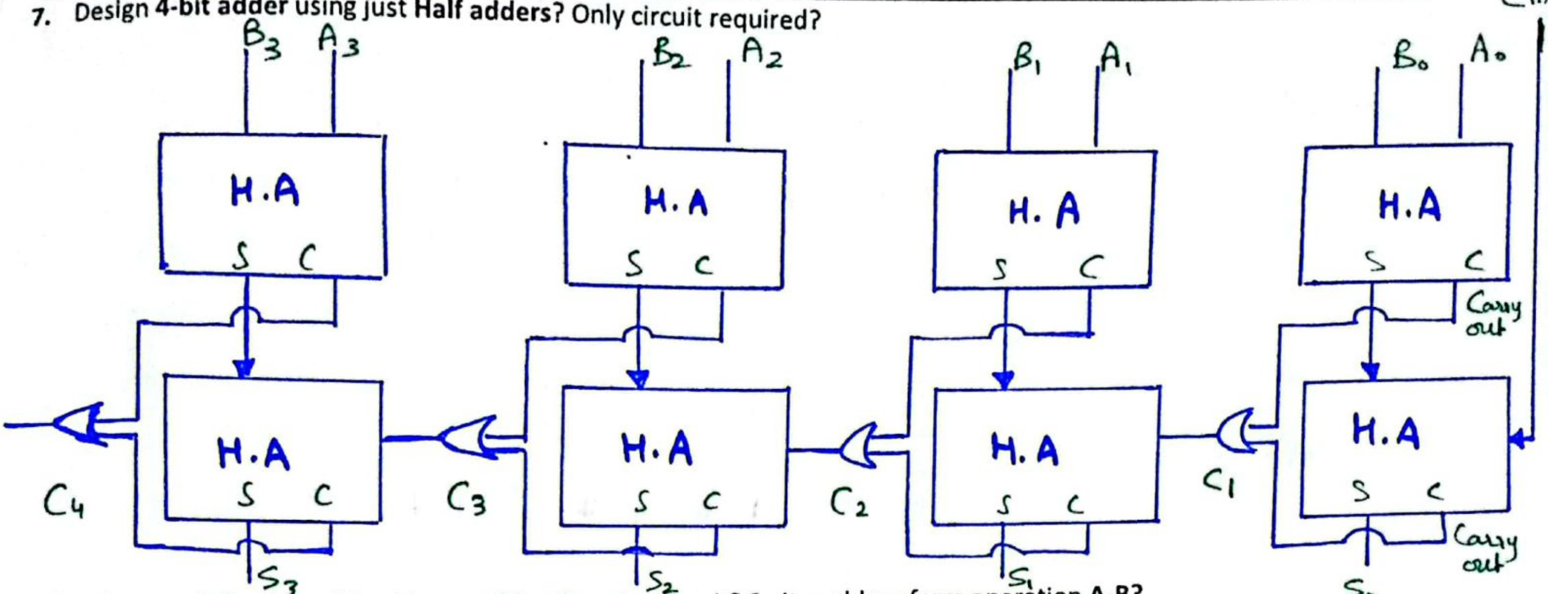
$V = 1 \oplus 0 = 1$

if '1' is carried in '0' carried out in most significant bit means addition of two non-negative numbers and getting a negative result.

$V = 0 \oplus 0 = 1$

ASSIGNMENT # 3 [EE-227]

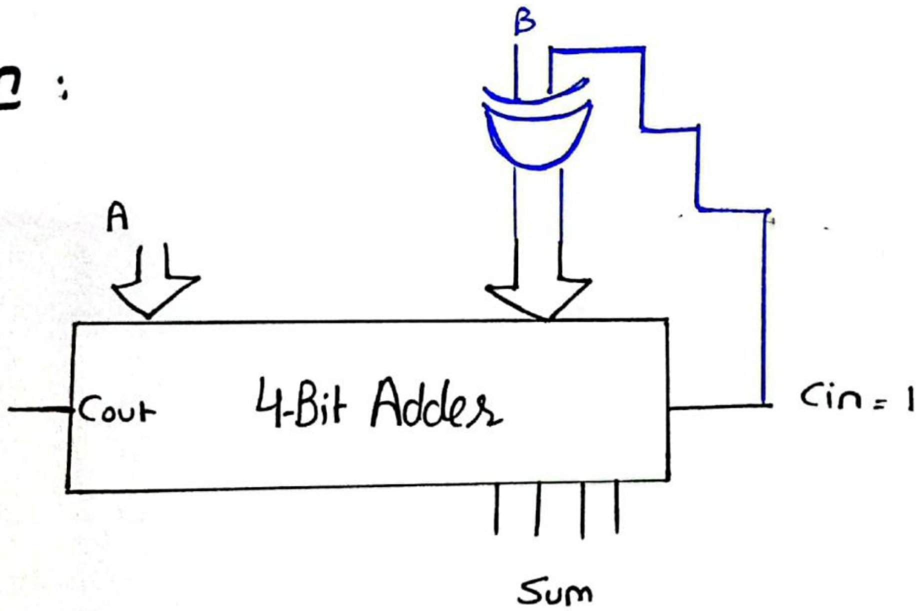
7. Design **4-bit adder** using just **Half adders?** Only circuit required?



8. Convert following **4-bit adder** to 4-bit subtractor circuit? So it could perform operation **A-B?**

Note: B could be represented in 2's complement

Solution :



$B \oplus 1 = B'$

$+ cin = 1 = 2's$ comp.

10. Design Circuit that accepts 4-bit BCD number as input and Detects BCD is valid/invalid?

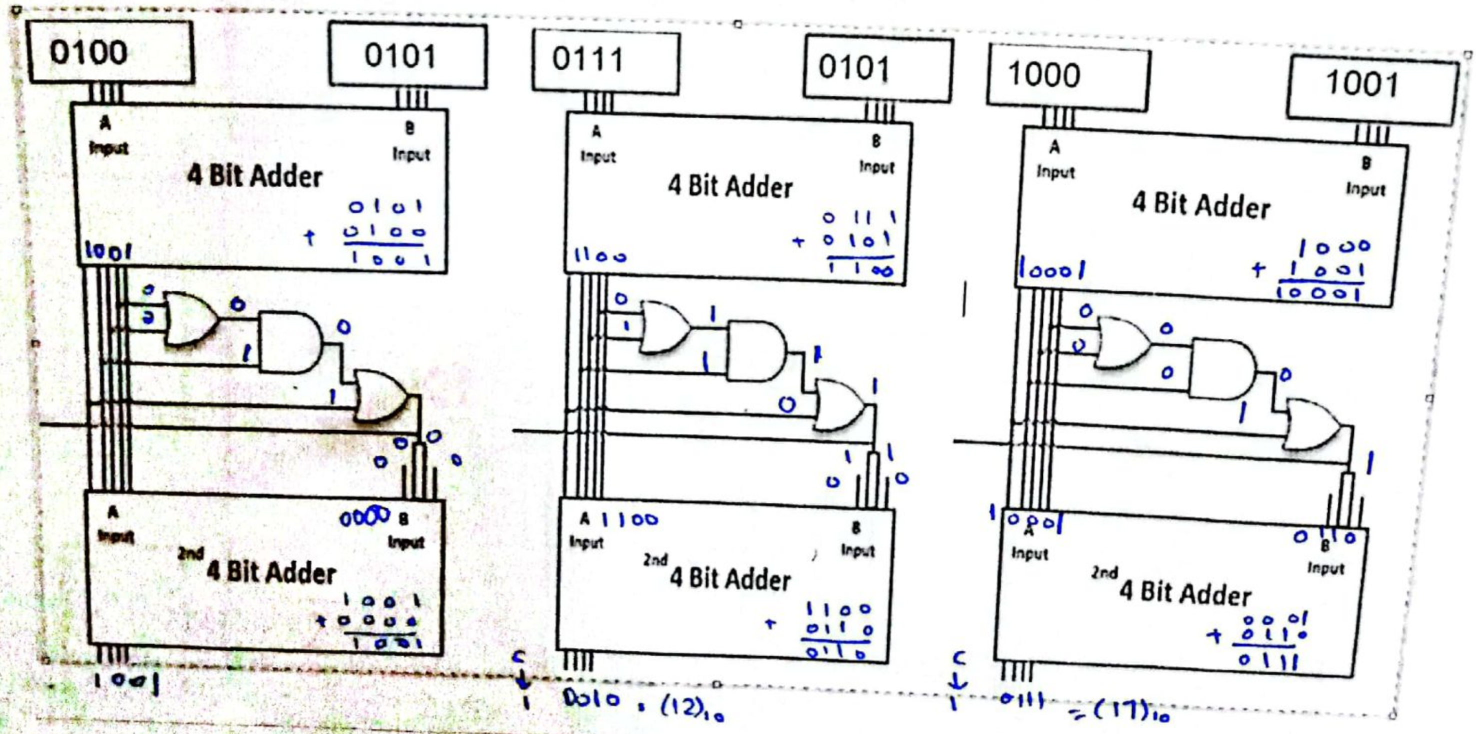
	A	B	C	D	F		A	B	C	D	F
0	0	0	0	0	1	8	1	0	0	0	1
1	0	0	0	1	1	9	1	0	0	1	1
2	0	0	1	0	1	10	1	0	1	0	0
3	0	0	1	1	1	11	1	0	1	1	0
4	0	1	0	0	1	12	1	1	0	0	0
5	0	1	0	1	1	13	1	1	0	1	0
6	0	1	1	0	1	14	1	1	1	0	0
7	0	1	1	1	1	15	1	1	1	1	0

SIMPLIFICATION:

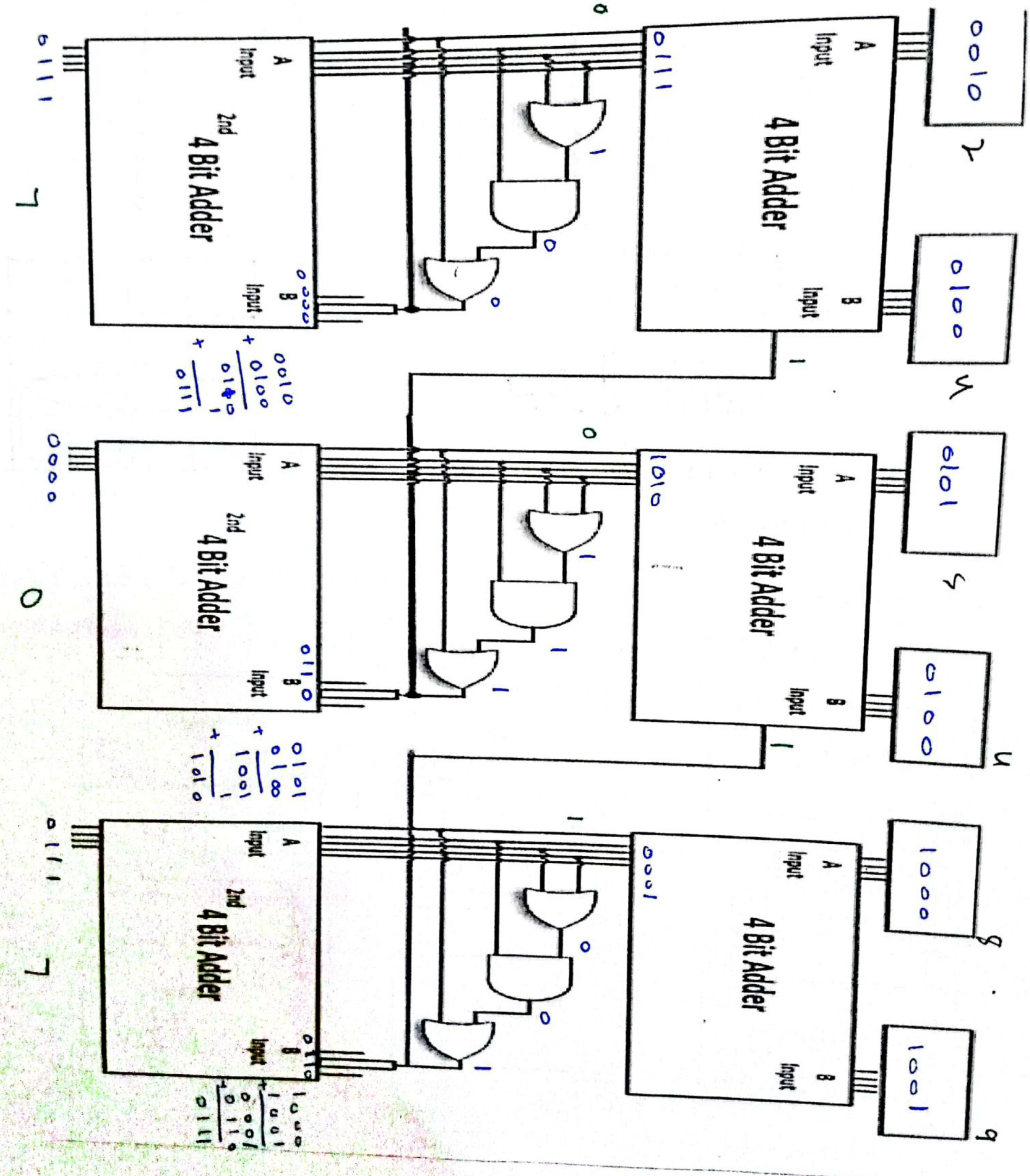
AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11				
10	1	1		

EXPRESSIONS: $A' + B'C'$

11. Perform BCD Addition using following circuit? BCD numbers are given in boxes on top?



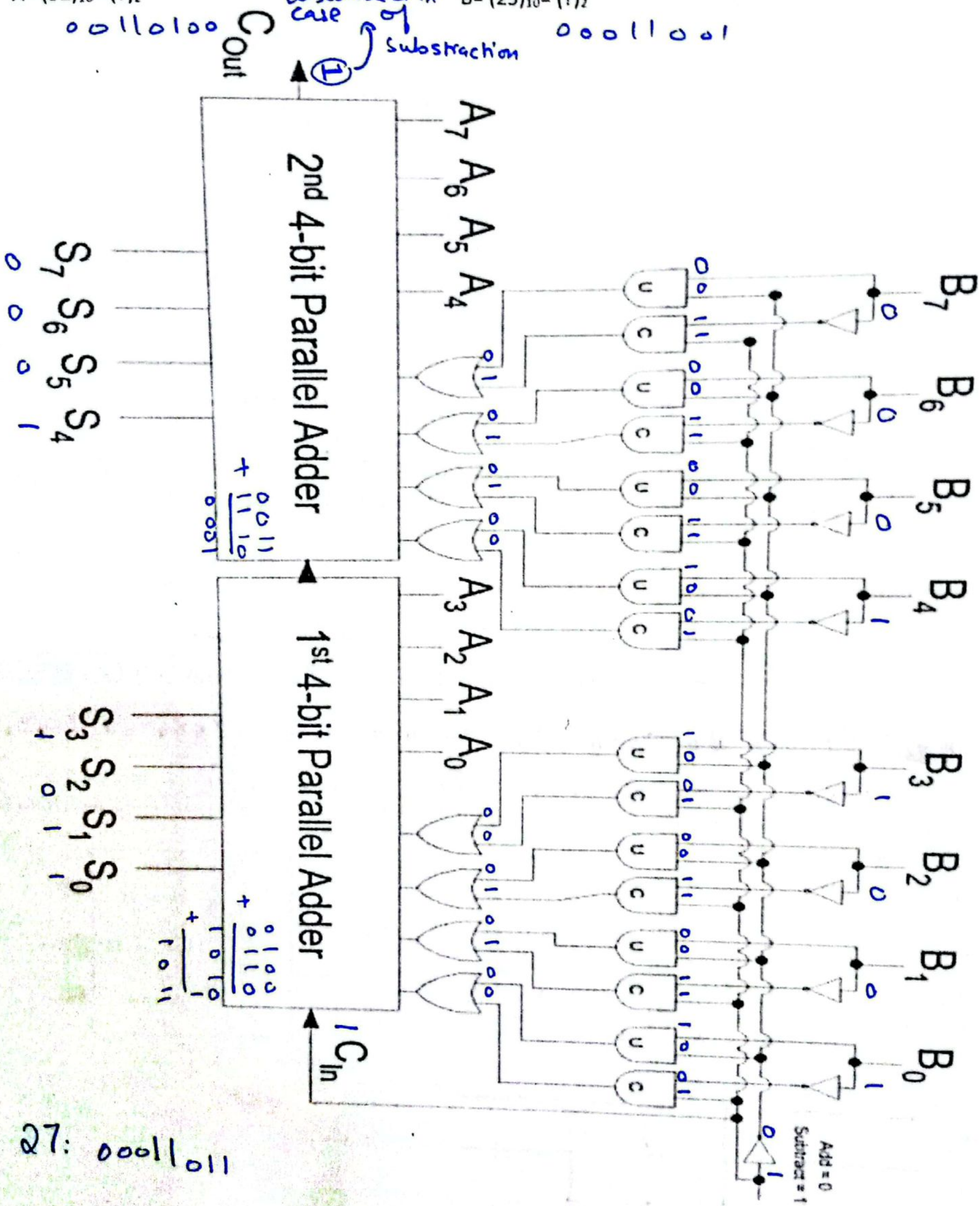
12. Perform BCD addition $(258)_{BCD}$+ $(449)_{BCD}$ using following circuit?



13. Implement the binary arithmetic operation (A-B), using the following 8-bit addition/Subtraction circuit?

$A = (52)_{10} = (?)_2$ 00110100

$B = (25)_{10} = (?)_2$ 00011001



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14. Design a single bit comparator from the following table? Write expression for **A==B, A<B and A>B**? Design circuit from expression using logic gates?

TABLE:

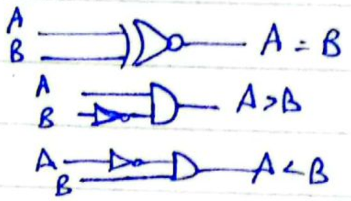
INPUT		OUTPUT		
A	B	A>B	A==B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

EXPRESSIONS

$F_{A==B} =$ $AB + \bar{A}\bar{B} = \overline{A \oplus B}$

$F_{A>B} =$ $A\bar{B}$

$F_{A<B} =$ $\bar{A}B$



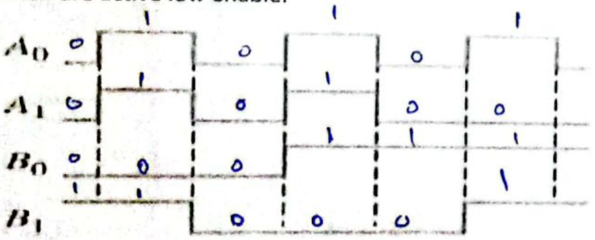
15. Write expression for **5-bit** comparator? (Use section **4.6**(Morris Mono) to design 5-bit comparator)

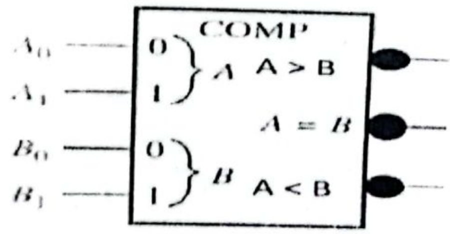
$A==B = (A_5 \oplus B_5)' \cdot (A_4 \oplus B_4)' \cdot (A_3 \oplus B_3)' \cdot (A_2 \oplus B_2)' \cdot (A_1 \oplus B_1)' \cdot (A_0 \oplus B_0)'$

$A>B = A_5 B_5' + x_5 A_4 B_4' + x_5 x_4 A_3 B_3' + x_5 x_4 x_3 A_2 B_2' + x_5 x_4 x_3 x_2 A_1 B_1' + x_5 x_4 x_3 x_2 x_1 A_0 B_0'$

$A<B = A_5' B_5 + x_5 A_4' B_4 + x_5 x_4 A_3' B_3 + x_5 x_4 x_3 A_2' B_2 + x_5 x_4 x_3 x_2 A_1' B_1 + x_5 x_4 x_3 x_2 x_1 A_0' B_0$

16. Apply the Waveform give below to the comparator circuit. Determine the output waveforms of **A==B, A<B, A>B** which are active low enable.



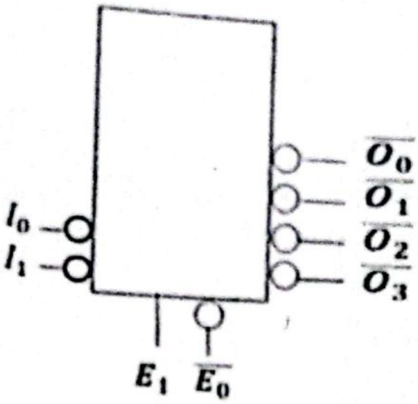


WAVEFORMS

ASSIGNMENT # 3 [EE-227]

17. Design following 2x4 Decoder? For reference see Section 4.9(figure 4.19)

BLOCK DIAGRAM



TABLE

INPUT				OUTPUT			
E_1	$\overline{E_0}$	$\overline{I_1}$	$\overline{I_0}$	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
X	1	X	X	1	1	1	1
0	X	X	X	1	1	1	1
1	0	1	1	0	1	1	1
1	0	1	0	1	0	1	1
1	0	0	1	1	1	0	1
1	0	0	0	1	1	1	0

EXPRESSIONS:

$\overline{O_0} = \overline{E_1 \overline{E_0} I_1 I_0} = \overline{E_1} + E_0 + \overline{I_1} + \overline{I_0}$

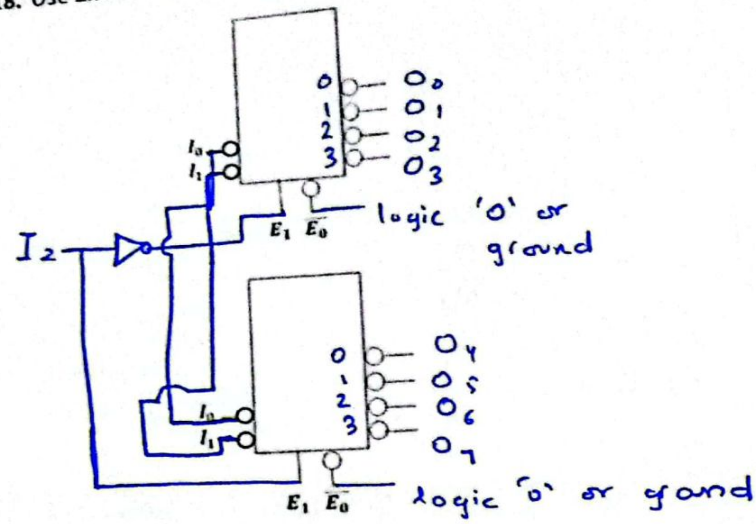
$\overline{O_1} = \overline{E_1 \overline{E_0} I_1 \overline{I_0}} = \overline{E_1} + E_0 + \overline{I_1} + I_0$

$\overline{O_2} = \overline{E_1 \overline{E_0} \overline{I_1} I_0} = \overline{E_1} + E_0 + I_1 + \overline{I_0}$

$\overline{O_2} = \overline{E_1 \overline{E_0} \overline{I_1} \overline{I_0}} = \overline{E_1} + E_0 + I_1 + I_0$

ASSIGNMENT # 3 [EE-227]

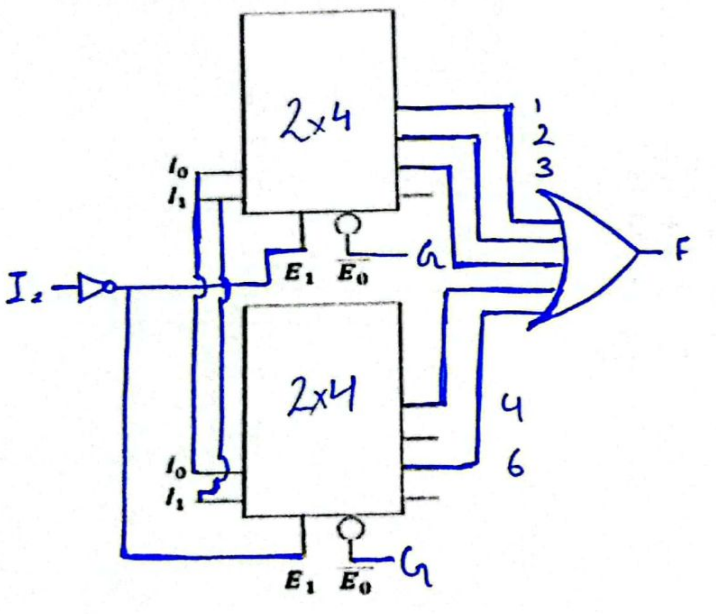
18. Use **2x4** decoder to design **3x8** decoder? Rename **OUTPUTS** and identify least and most decoder

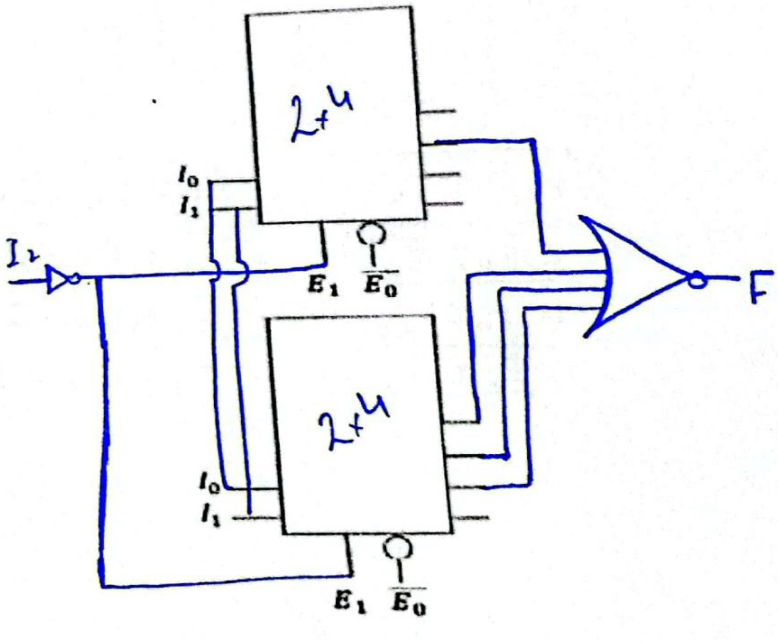


19. Use following 2x4 decoders to implement given function

a. F(A,B,C)= $\Sigma(0,1,2,4,6)$

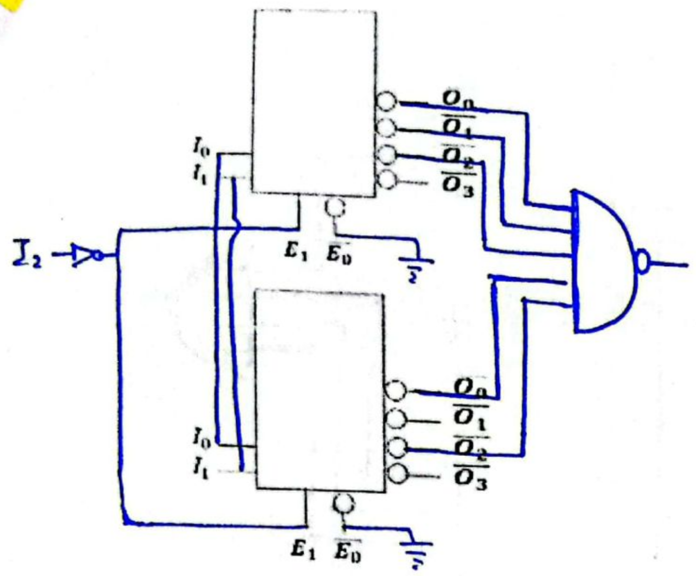
b. $F(A,B,C) = \prod(1,4,5,6)$



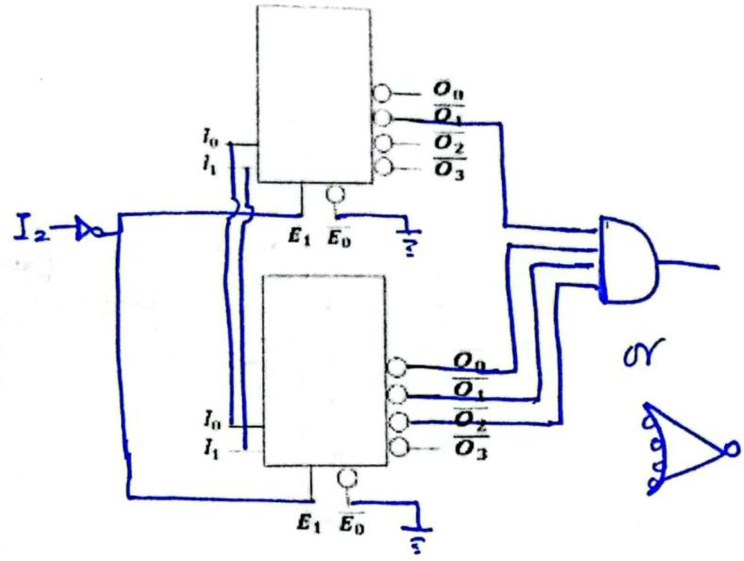


Scanned with CamScanner

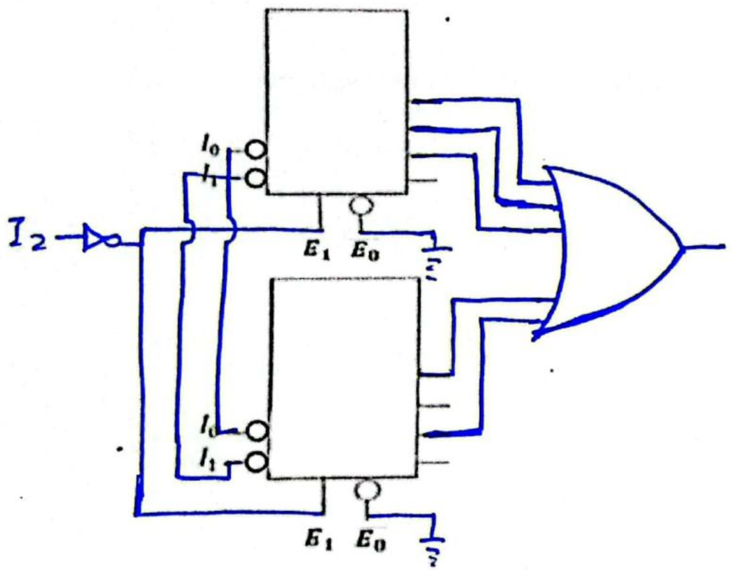
c. F(A,B,C)= $\sum(0,1,2,4,6)$



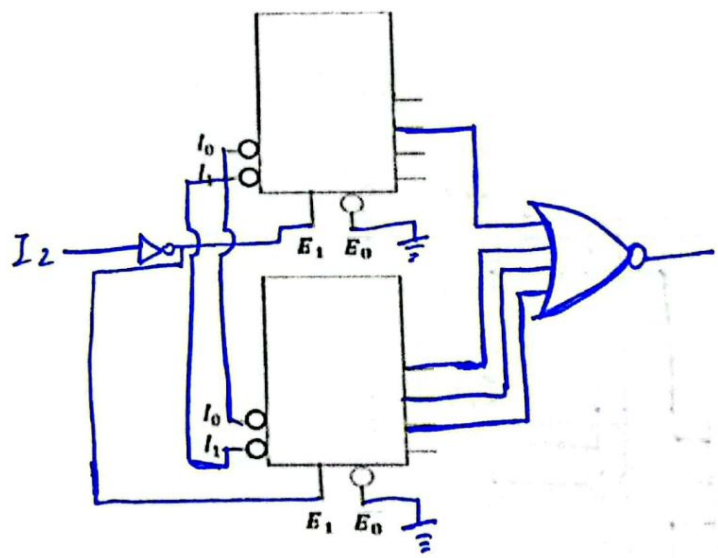
d. $F(A,B,C) = \prod(1,4,5,6)$



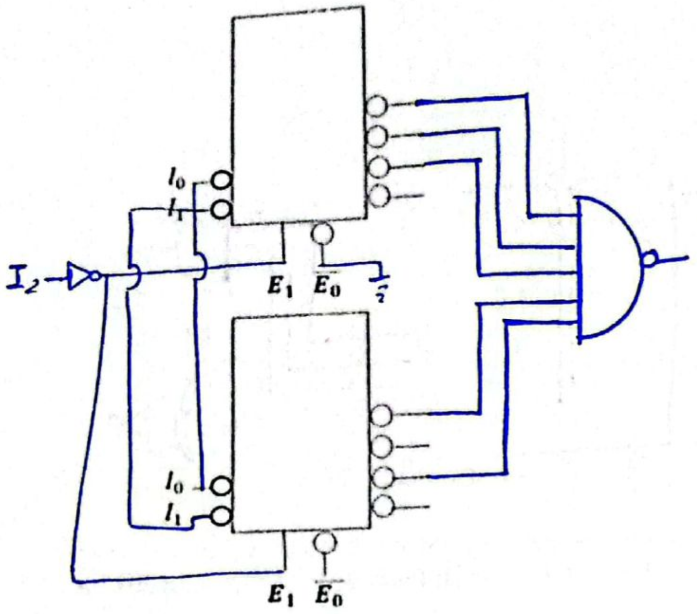
e. F(A,B,C)= $\sum(0,1,2,4,6)$



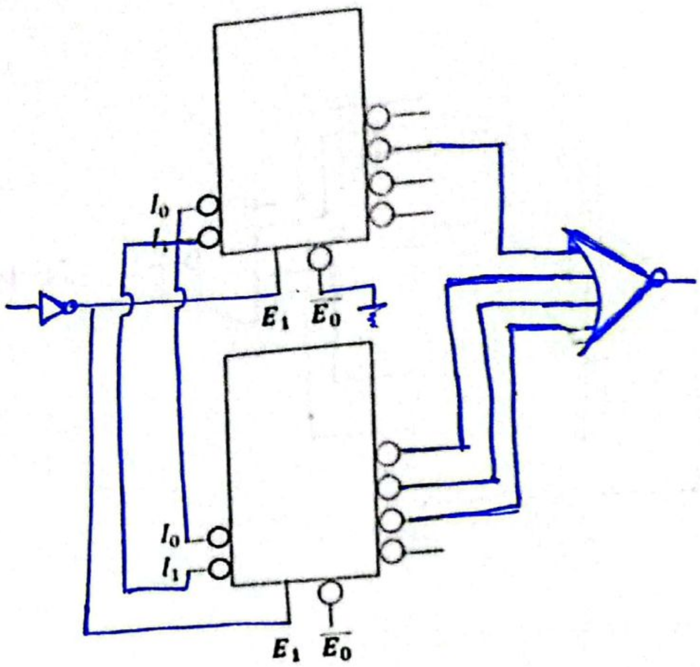
f. $F(A,B,C) = \prod(1,4,5,6)$



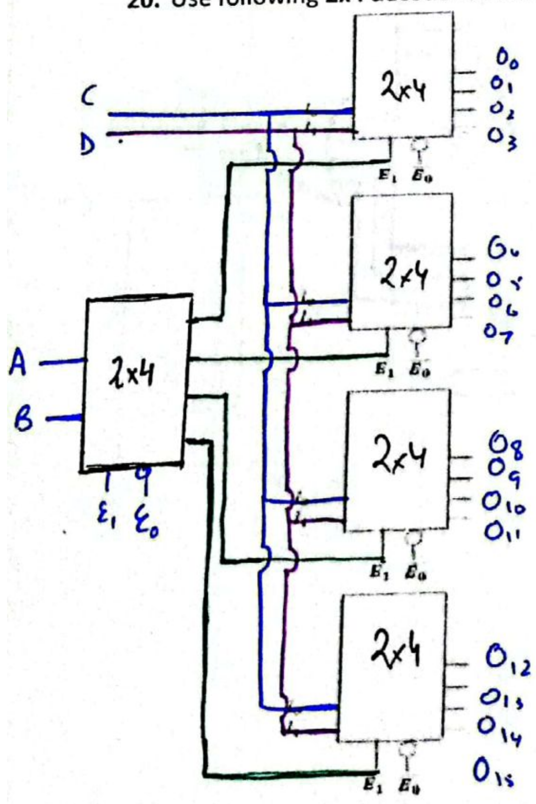
g. F(A,B,C)= $\sum(0,1,2,4,6)$



h. $F(A,B,C) = \prod(1,4,5,6)$



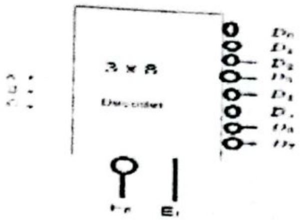
20. Use following **2x4 decoder** to construct **4 X 16 decoder**. You are not supposed to use any external gates?



ASSIGNMENT # 3 [EE-227]

21. Design following **3x8 Decoder**? For reference see Section 4.9(figure 4.18, table 4.6)

BLOCK DIAGRAM



TABLE

INPUT					OUTPUT							
$\overline{E_0}$	E_1	A	B	C	$\overline{D_0}$	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\overline{D_4}$	$\overline{D_5}$	$\overline{D_6}$	$\overline{D_7}$
1/0	0	X	X	X	1	1	1	1	1	1	1	1
1	0/1	X	X	X	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	0	1	1	1	1	0	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

EXPRESSIONS

$\overline{D_0} = (\overline{\bar{A}\bar{B}\bar{C}})$

$\overline{D_1} : (\overline{\bar{A}\bar{B}C})$

$\overline{D_2} = \overline{\bar{A}B\bar{C}}$

$\overline{D_3} = \overline{\bar{A}BC}$

$\overline{D_4} = \overline{A\bar{B}\bar{C}}$

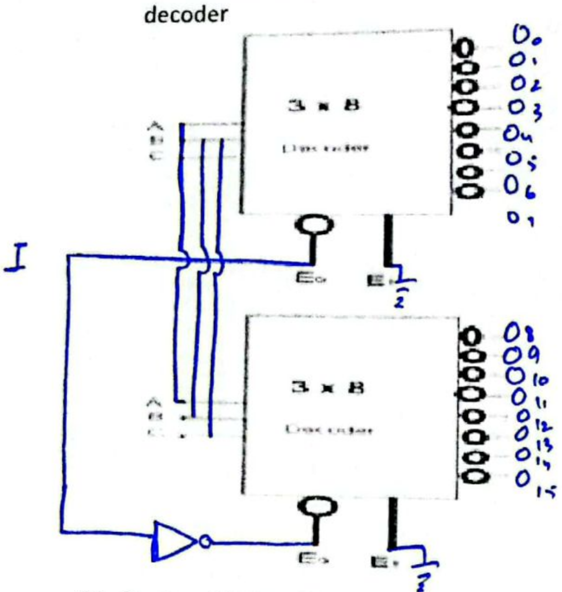
$\overline{D_5} = \overline{A\bar{B}C}$

$\overline{D_6} = \overline{AB\bar{C}}$

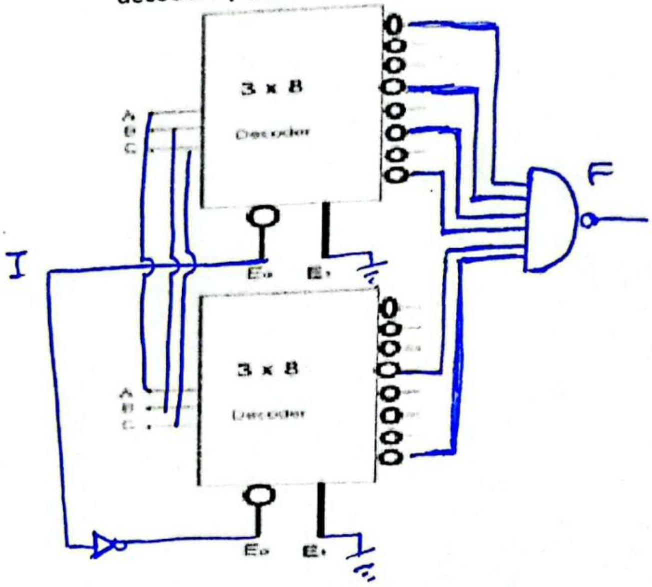
$\overline{D_7} = \overline{ABC}$

ASSIGNMENT # 3 [EE-227]

22. Use above designed **3 X 8** decoder to design **4 X 16** decoder



23. Implement following function using two 3 X 8 decoder **F(A,B,C,D)=** $\sum(0,3,5,7,11,15)$



24. Design 4X2 Low Priority Encoder? For reference see section 4.10(table 4.8)

TABLE

INPUT				OUTPUT		
D_0	D_1	D_2	D_3	A	B	Valid
0	0	0	0	X	X	0
1	X	X	X	0	0	1
0	1	X	X	0	1	1
0	0	1	X	1	0	1
0	0	0	1	1	1	1

SIMPLIFICATION AND EXPESSIONS

$A = \bar{D}_0 \bar{D}_1$

$B = \bar{D}_2 \bar{D}_0 + \bar{D}_0 D_1$

$B = \bar{D}_0 (D_1 + \bar{D}_2)$

D_0D_1 \ D_2D_3	00	01	11	10
00	X	1	1	1
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

D_0D_1 \ D_2D_3	00	01	11	10
00	X	1	0	0
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

$V = D_0 + D_1 + D_2 + D_3$

25. **Design 8 X 3 Low Priority Encoder?** For reference see slides Lec_17 uploaded on google classroom?

TABLE

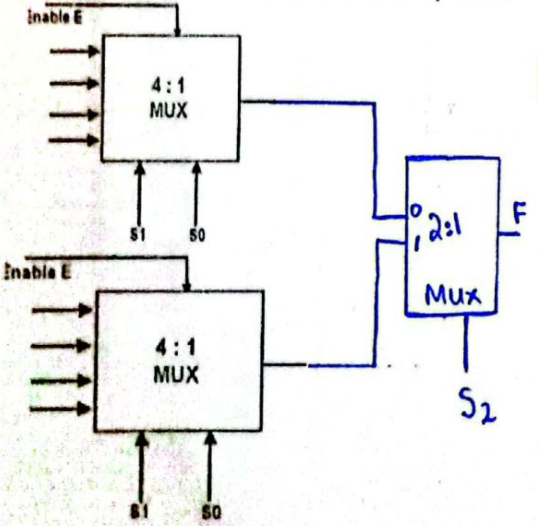
INPUTS							OUTPUTS		
I_0	I_1	I_3	I_4	I_5	I_6	I_7	O_0	O_1	O_2
1	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	X	0	0	1
0	0	1	X	X	X	X	0	1	1
0	0	0	1	X	X	X	1	0	0
0	0	0	0	1	X	X	1	0	1
0	0	0	0	0	1	X	1	1	0
0	0	0	0	0	0	1	1	1	1

$$O_0 = I_4\bar{I}_3\bar{I}_1\bar{I}_0 + I_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0 + I_6\bar{I}_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0 + I_7\bar{I}_6\bar{I}_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0$$

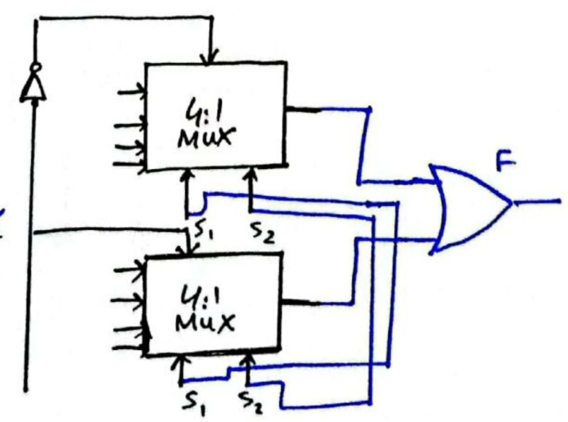
$$O_1 = I_3\bar{I}_1\bar{I}_0 + I_6\bar{I}_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0 + I_7\bar{I}_6\bar{I}_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0$$

$$O_2 = I_1\bar{I}_0 + I_3\bar{I}_1\bar{I}_0 + I_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0 + I_7\bar{I}_6\bar{I}_5\bar{I}_4\bar{I}_3\bar{I}_1\bar{I}_0$$

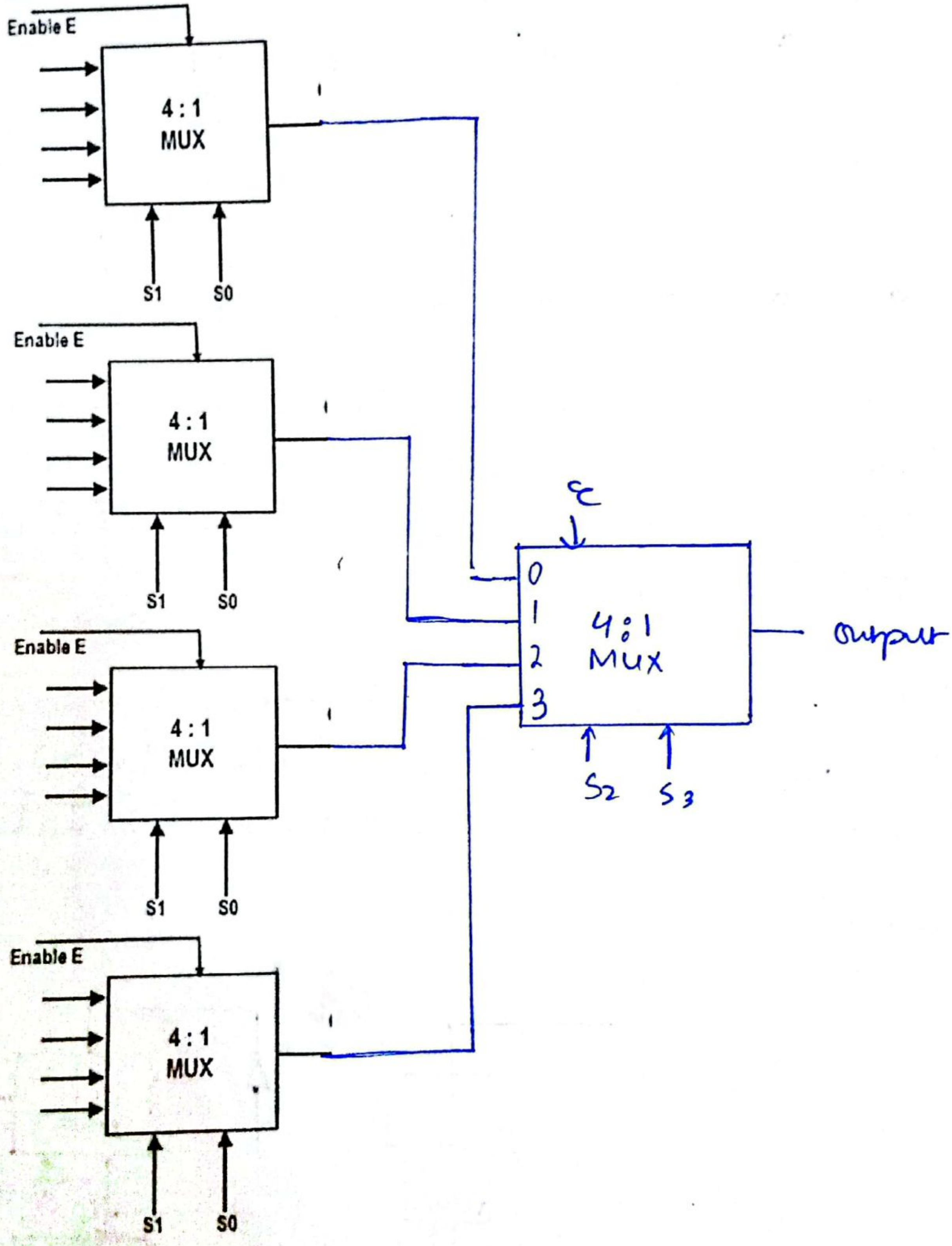
26. Use following **4 X 1 multiplexer** to create **8 X 1** multiplexer?



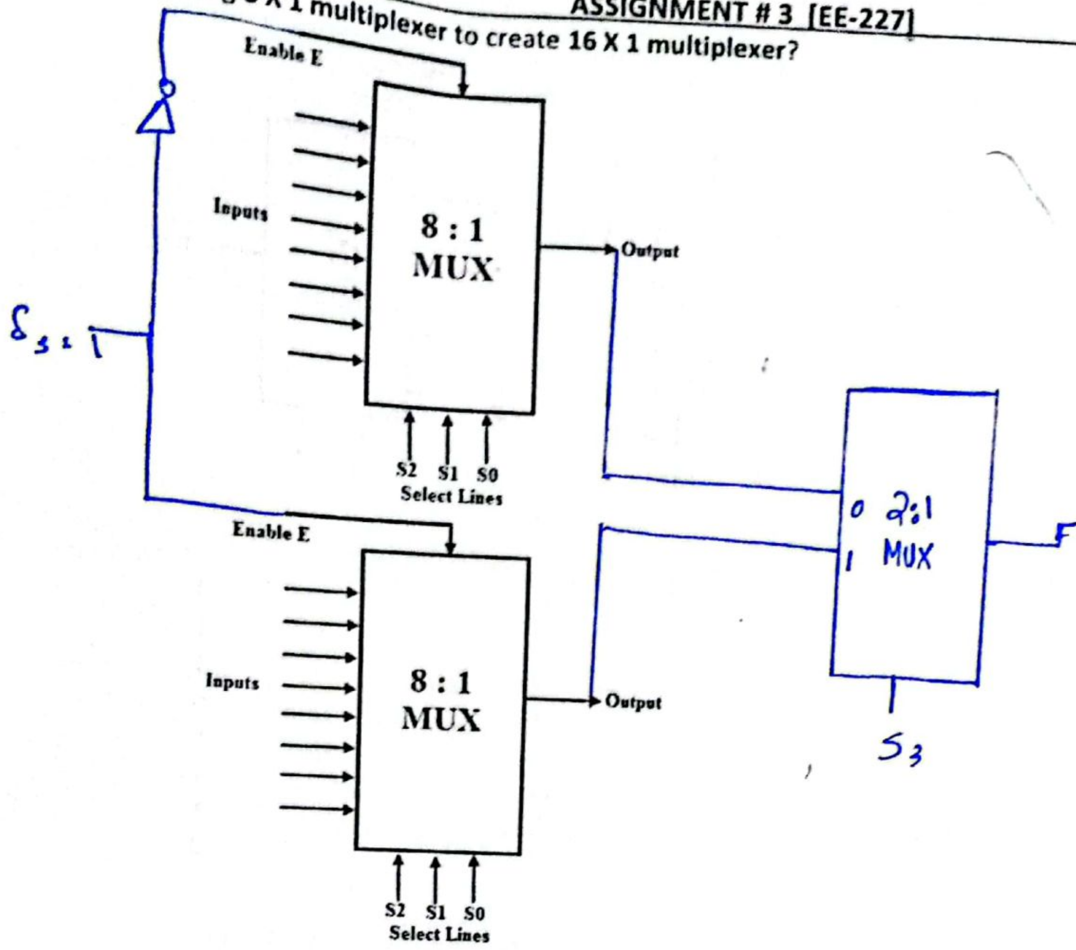
OR



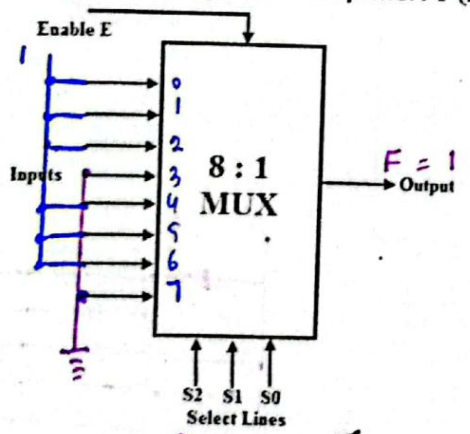
27. Use following 4 X 1 multiplexer to create 16 X 1 multiplexer?



28. Use following **8 X 1 multiplexer** to create **16 X 1 multiplexer?**



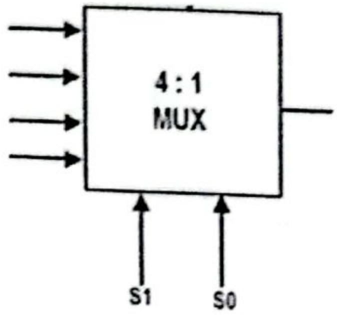
29. Implement given function using **8 X 1 multiplexer?** $F(x, y, z) = \sum(0, 1, 2, 4, 5, 6)$



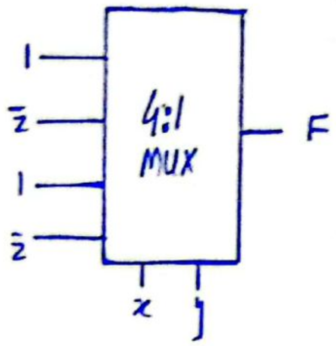
x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
1	0	0	1
1	0	1	1
1	1	0	1

ASSIGNMENT # 3 [EE-227]

30. Implement given function using **4 X 1 multiplexer?** $F(x, y, z) = \sum(0, 1, 2, 4, 5, 6)$



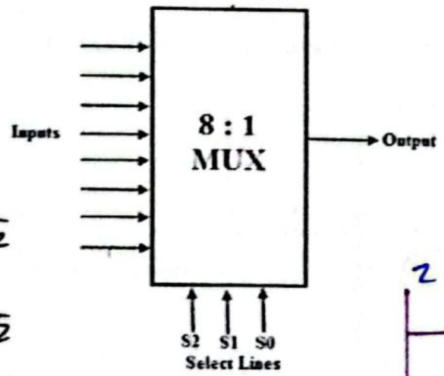
x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



TABLE

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

31. Implement given function using **8 X 1 multiplexer?** $F(w, x, y, z) = \sum(0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$



w	x	y	z	F	
0	0	0	0	1	$\bar{z}$
0	0	0	1	0	
0	0	1	0	1	$\bar{z}$
0	0	1	1	0	
0	1	0	0	0	z
0	1	0	1	1	
0	1	1	0	0	z
0	1	1	1	1	
1	0	0	0	1	$\bar{z}$
1	0	0	1	0	
1	0	1	0	1	$\bar{z}$
1	0	1	1	0	
1	1	0	0	1	1
1	1	0	1	1	
1	1	1	0	1	1
1	1	1	1	1