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Room 212, Building 321, East Campus, USTC

3rd year undergraduate student

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## Education

University of Science and Technology of China

HEFEI, ANHUI, CHINA

**B.S. in Computer Science (School of Gifted Young)**

Sept. 2014 – present

- GPA 3.75/4.30
- Enrolled in the Talent Program in Computer and Information Science and Technology

### Awards

- Outstanding Student Scholarship (Grade 2) in Sophomore Year
- Outstanding Student Scholarship (Grade 3) in Junior Year
- Outstanding Freshman Scholarship (Grade 3)

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## Research Experience

System Group Intern

MICROSOFT RESEARCH ASIA

**Efficient and Scalable Total-Order Message Scattering in Datacenter Network**

Jul. 2017 – present

- Offload reordering and buffering to endhost: separate control plane from data plane
- Minimax clock synchronization mechanism: low latency
- Logical equivalent of endhosts and switches: provide incremental deploy ability

Soft Robot Lab, instructed by [Xiaoping Chen](#)

UNIV. OF SCIENCE AND TECH. OF CHINA

**Motion Planning for Soft Multi-Segment Manipulators in 3D Environment**

Dec. 2016 – Mar. 2017

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## Work Experience

USTC Freeshell

UNIV. OF SCIENCE AND TECH. OF CHINA

**Maintainer**

Sept. 2014 – Jun. 2015

- Container-based IaaS service based on OpenVZ virtualization, supporting various Linux distributions.
- Reconstruct previous version with ceph and openstack working in progress

[USTC Opensource Mirrors](#)

UNIV. OF SCIENCE AND TECH. OF CHINA

**Maintainer**

Jul. 2015 – present

- One of the biggest opensource mirror in China.
- Test and deploy several kinds of block cache, finally improve the disk IO capability more than twice
- Deal with many kinds of performance or software/hardware issues

[Distributed File Storage](#)

UNIV. OF SCIENCE AND TECH. OF CHINA

**Team project of Principles and Design of Operating Systems**

Mar. 2016 – Jun. 2016

- Implement git-like(content hash as index) file/directory indexing API for web interface(implemented by others)
- Design and Implement synchronize operation based on concept of blockchain

Pipeline MIPS CPU on FPGA

UNIV. OF SCIENCE AND TECH. OF CHINA

**Course project of Computer Organization**

May. 2016

- Implemented in Verilog, 5 stage pipeline, 40 instructions, exception support.

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## Extracurricular Activities

**President, Linux User Group, USTC**

May. 2016 – June. 2017

**Vice President, Linux User Group, USTC**

May. 2015 – May. 2016

**Vice Minister, Technology team, Student Union, School of Gifted Young**

Sept. 2015 – May. 2016

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## Skills

**Programming:** C/C++, Python, Matlab, Bash, Verilog

**Linux:** Network management, Server maintaining

**Github:** <https://github.com/Alkaid-Benetrash>