Dreamcast
Hardware
Specification Outline

September 3rd 1999 13:43 Sega Enterprises Development Department

Contents

1 Outline of Dreamcast

This section is an outline of the Dreamcast system. For individual details please refer to the appropriate sections. Additionally with regards to the details of the various sections that follow this section, please refer to other material.

1.1 Outline

A feature of Dreamcast is that it is a system with high quality graphics capability, thanks to its PVR2 core, and superb quality audio which has been produced at a low cost and has a retail price of under $200. Additionally by including a modem as a standard specification, it allows the easy development of network/internet business.

1.2 System Specification

These are the hardware specifications of the basic Dreamcast system.

- CPU: Hitachi SH4 200MHz , Super Scalar RISC Processor , 360MIPs, 1.4GFLOPs
- ASIC: Image drawing VL/NEC HOLLY 100MHz , Audio YAMAHA AICA
- Polygon performance : At peak 3 million polygons/sec (triangle / quadrilateral) , 1.5 million polygons/sec visible
- Polygon functions: shadow , tri-linear MIPMAP , edge anti-aliasing, fog, Z buffering etc.
- 16MB Main memory(Can expand to a maximum of 32MB)
- 8MBTexture memory(Can expand to a maximum of 16MB)
- 2MB Boot ROM
- 128KB Flash memory
- 2MB audio memory(Can expand to a maximum of 8MB)
- Audio function: 64ch PCM / ADPCM / FM , 44.1KHz
- 4x～12x CAV-type GD-ROM drive(built-in 128KB buffer RAM)
- 4 Game ports (adapted for the optional light gun, storage device etc.)
- 4 port backup media (optional device)
- RTC(Real Time Clock) that has capability of battery backup
- 33.6kbps modem card
- Adapted for NTSC/PAL, VGA monitor image output

1.3 System Block

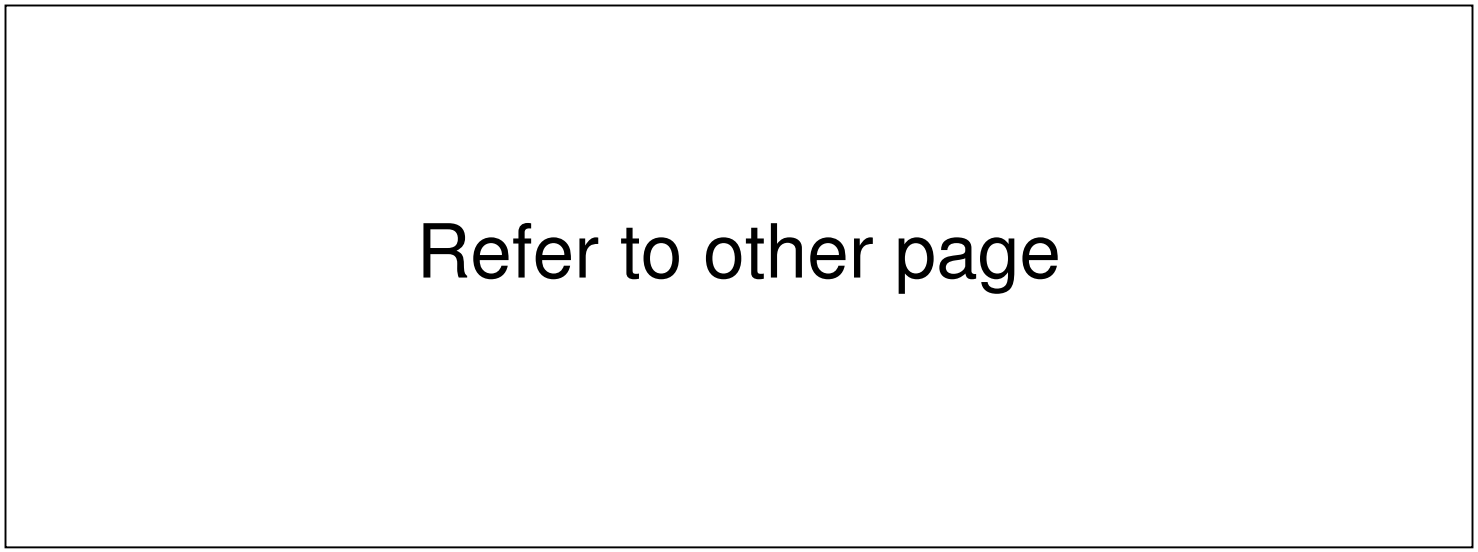


Figure 1-1 Dreamcast Block Diagram

Figure 1-1 is the system block diagram. A simple explanation of each block is below.

CPU

The main CPU is a Hitachi SH4 with an internal performance of 1.8V / 200MHz and external performance of 3.3V / 100MHz. The frequency of the clock (where the operation is based) is 33.3MHz output from the external PLL. SH4 processes game sequence, AI, 3D operation and 3D image drawing commands. Also the PIO i/f, which allows external I/O access, is used in video mode selection. (Explained later)

Main memory

In order to take advantage of SH4 performance, the SDRAM (which is the main memory) is directly connected to SH4. The bus width is 64bit with a movement frequency of 100MHz and at burst, it has a maximum transfer quantity of 800MB/s (a theoretical value) Additionally, SH4 does not share the texture data/audio data and the main memory SDRAM. There is 16MB of base system space.
The access speed is -7ns or an equivalent speed.

HOLLY

This has a built-in PVR2 core and supports image drawing. In other words HOLLY, which is the core of the interface supports CPU i/f, texture memory i/f and/ or the peripheral devices G1/G2 bus i/f and the Maple i/f.
HOLLY uses SH4 and the SH4 DMA to read the display list created in the main memory to generate 3D graphics internally. When using texture mappings, the texture data is read from the texture memory.
From SH4, it is accessed via the multiplexed 64bit address/data interface mode.
From HOLLY, each RGB 8bit image data is accessed via the video DAC/ encoder.

Texture (texture/frame buffer) memory

As a base system it has an area of 8MB(which can be expanded to a maximum of 16MB)and HOLLY occupies 4 16M bit SDRAM(8 when expanded).The data bus width is 16bit×4 and 16/32/64 bit access is possible. The memory is accessed from HOLLY at 100MHz using -7ns or equivalent.

G1 bus

The GD-ROM drive, Boot ROM and flash memory are buses in parallel connection and the bus has a multiplexed EIDE-like i/f and Boot ROM i/f. Part of the Boot ROM address line, the 8 bit of code that contains the system data, is multiplexed. The data bus width is 16 bit at the time of GD-ROM access and 8 bit for Boot ROM and Flash memory access. It is also subject to type 1 interrupted entry from the GD-ROM.
GD-ROM access uses an ATAPI like protocol. For details of the protocol, refer to a separate document.
In order to prevent hardware reconstruction and Illegal copies, this bus is not external on commercially produced Dreamcast hardware. In the case of the SET5 set for software Development, the Crossproducts Company debugging adapter base is connected to this and thus allows software debugging. In that case, the downloading of data occurs through this bus.

G2 bus

The G2 bus is a multiplexed clock bus and supports the audio IC, AICA ,and supports the connection of optional devices like the card-in unit (modem) and the externally connected debugging tool.
The bus clock is 25MHz and the bus width is 16bit. It is subject to interruptions from AICA, the modem and external devices.
With commercially produced Dreamcast hardware, this bus is on the outside and has is used as an expansion bus.

4x-12xGD-ROM

The drive reads using a CAV method and the data reading speed is 4x for normal space and 12x for high-density space. The drive has a 128KB buffer RAM and data is transferred through HOLLY. It delivers GD-DA (high-density digital audio) as opposed to AICA that is an audio IC.

Boot ROM

The system/boot ROM used by SH4 is connected to the G1 bus. There are 2MB of ROM space and a data bus width of 8 bit. The access time of the Dreamcast is set at 100ns.

Flash ROM

Information such as the Dreamcast system administration number is stored here.

Modem

It is a modem card featured as standard on the Dreamcast system as a card type unit and is connected to the G2 bus. The communication speed is 33.6Kbps and is equipped with a modular terminal.

AICA

AICA is a YAMAHA audio IC. It is a chip that has the primary objective of being in charge of the Dreamcast audio and reproduces 64ch PCM/ADPCM/FM stereo sound. Starting from the GD ROM it picks up audio signals or 33.8688MHz from the audio clock. Stereo sound generated within AICA becomes output from the external audio DAC/AMP.
As an internal configuration it is divided into an audio block and G2 bus i/f block and has a shared audio memory. The internal chip of the CPU uses an ARM7 core. A RTC (Real Time Clock) is also built-in. The audio block frequency is 22.5792MHz and the G2 bus i/f block frequency is 25MHz. As a peripheral i/f it supports audio memory i/f as well as MIDI i/f. The RTC has a 3V Lithium battery for backup purposes and a 32.768KHz x'tal.
Also, unlike video DAC/encoder, it allows video mode settings (switching) access.

Audio memory

AICA is connected to an audio memory occupying the 16M bit SDRAM (space is 2MB but can be expanded to a maximum of 8MB). The memory bus width is 16bit and access is at 67.7MHz.

External connection device

This is a device just like AICA and the modem that is located on the G2 bus and connected to a debugging tool etc.

Maple i/f

This is an original Sega peripheral interface supported by HOLLY that is a serial-type control pad interface. The Dreamcast console supports up to 4 ports. Additionally, this port supports the control pad (Light Gun) as well as connected backup media (which is explained later). The maximum port transferring rate is 2Mbps.

Backup media (B/U)

Backup media is optional support used for saving application data. It is connected through the Maple port and HUB (control pad) and a maximum of 4 can be connected.

MIDI i/f

This supports MIDI IN/OUT for the purpose of audio development.

Video output

Image information generated by HOLLY passes through the video DAC/encoder (Digital-Video-Encoder) and becomes output compatible with general NTSC/PAL monitors as well as a VGA. NTSC/PAL video signal output from a Video DAC/encoder and stereo sound output from AICA becomes output from the RCA connector. The cable connected to the RCA connector can be a multi-purpose commercial product. Opposed to the VGA monitor, analogue RGB/ synchronised signal etc will become output from the expansion VGA connector. The NTSC/PAL, VGA etc. video modes depend on the type of cable connected to the connector and that information is reflected in the SH4 I /O. This can be switched from SH4 to HOLLY using the AICA image register settings.

Audio output

Stereo sound generated by AICA passes through the audio DAC/AMP and video output generated by HOLLY and becomes output from the RCA connector and/or the expansion VGA connector.

PLL

This is for creating each clock in the system and has an attached 13.5MHz x'tal. The frequency of the output clock (or the output destination) is 33.3MHz(SH4) and 54MHz(HOLLY)

Other

The power unit has 100～120V AC, 50/60Hz input and supplies DC3.3V or DC5.0V to the system. The DC1.8V, DC2.4V for the SH4 interior / HOLLY internal power supply are created by a separate electrical power source IC.

----End of Outline----

2 CPU: SH4

The CPU used in the Dreamcast system is a SH4 (HITACHI) and with respect to 3D game programming it is mainly responsible for the processing of the game sequence, AI, physical calculations and 3D conversions. Below is an explanation of the SH4 settings and peripherals.

2.1 Features of SH4

Table 2-1 describes the main functions of SH4.

Core	
Instruction core	32bit RISC, 16bit Instruction
Pipe line	5 stage
FPU	single/ double accuracy IEEE754
Clock	Internal 200 MHz, external 100 MHz, peripheral clock 50MHz
Performance	360MIPS (core), 1.4GFLOP (matrix multiplication)
Super Scalar	2
Cache	I$: 8KB, D$: 16KB (Both are direct mapping). There are index / RAM functions
Other	high-speed packet transfer through the store queue function is possible (32B)
Peripherals	
calculation	Matrix multiplication, 1/√
DMAC	4 channel, DDT mode
Memory i/f	SDRAM i/f, Multiplex i/f
MMU	Page Size: 1KB, 4KB, 64KB, 1MB
UBC	2 Break Point
SCI	synchronised clock, synchronised pace
Timer	3 Channel
RTC	Real Time Clock, Alarm, calendar
Process and package	
Electrical power consumed	1.8W
Voltage	External: 3.3 VDC, Internal1.8 VDC
Process	0.25um, 2.4V / 3.3V
Package	256 BGA
Die Size	49mm^2

Table 2-1 Features of SH4

2.2 SH4 Settings

With respect to the Dreamcast system, SH4 uses the settings described in table 2-2. (Note that it is slightly endian)

The operational mode, described in table 2-3, is dependent on the MD [7:0] pin and these pins can be used as other functions and is internally sampled when the reset is cancelled. The clock mode is the same except that after booting, the software can be used for further settings.

Category	Setting
External clock	100 MHz (Cycle Time: 10ns)
Internal clock	200 MHz (Cycle Time: 5ns)
Endian	Little Endian (Intel-style)

Table 2-2 Configuration of SH4

Mode pin	Setting	Operation
MD7	0	SH4 is master mode operation
MD6	1	area0 is MPX operation
MD5	1	All the buses are little endian
MD4	0	64 bit bus width operation
MD3	0	64 bit bus width operation
MD2	1	Clock mode
MD1	0	Clock mode
MD0	1	Clock mode

Table 2-3 SH4 operation mode settings

2.3 Main memory

The main memory of the system is directly connected to the CPU: SH4 and used as the SH4 program code and work memory. The supported memory size depends on the memory cost. The main memory specification is described in table 2-4. The basic configuration is an SDRAM with 16MB of space and two 64M bit (bus width 32bit).

Memory size	16MB
Technology	2 64Mbit SDRAM (4bank x 512k word x 32bit)
Total bus width	64 bit
Burst sequence	Sequential
Number of internal banks	4
Bus width of 1 chip	32 bit
Frequency	100MHz
BBW	800MB/s

Table 2-4 The main memory base specification

2.3.1 The memory configuration

Table 2-5 is the configuration details and figure 2-1 is the memory configuration.

Space	Number	Each RAM	C_{LOAD} (Addr/Ctrl/Data)	Fig.
16MB …base	2	4 x 512k x 32bit SDRAM (64Mbit)	5 pF / 5 pF / 7 pF	2-1

Table 2-5 The main memory configuration

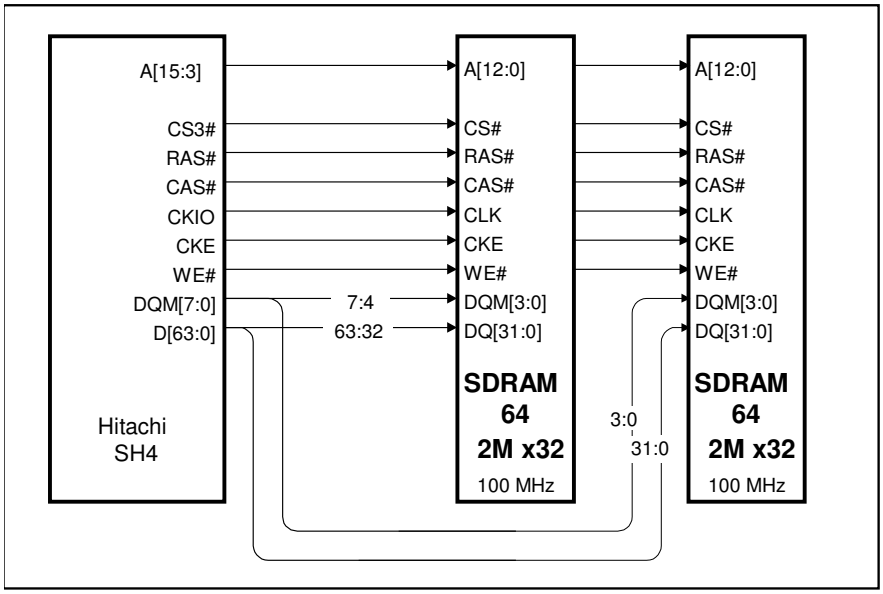


Figure 2-1 Configuration of 16MB SDRAM…Uses 2 64Mbit (4 x 512k x 32bit)

2.3.2 SDRAM Control

The BSC (Bus State Controller) in SH4 controls the SDRAM, all of the SDRAM control signals, refreshing and pre-charging.

The SDRAM needs to be set after the point when the power has just been switched on but before the SDRAM has yet to be accessed.

SH4 uses the software to generate the SDRAM configuration cycle. Writing in the SH4 register generates the configuration cycle.

The settings are cited below.

- The SDRAM burst length is set as 4. Only this setting is possible.
  Also the CAS latency is set as 3.
  The burst sequence is set as sequential access.
- The SH4 internal refresh counter is set as 2048 times per 32msec.
- SH4 is set as ラスdown mode.
  This is to speed up access when using the same row address. (However in this mode, you are prohibited from having the WAIT function on for a long time.)

SH4 is the only SDRAM access master. Access from HOLLY to the SDRAM uses the SH4 DMA cycle. Due to SH4 DDT mode DMA, 1 external device can become the logical bus master.

With channel 0, an On Demand DMA (ODD) protocol is possible. Due to the ODD, the external device can program the SH4 DMAC channel0. From this HOLLY is able access the SDRAM efficiently.

2.4 System memory mapping

The external SH4 bus is a 64-bit data bus that allows a 26-bit address bus and 1 byte access. The internal address is 32 bit. Additionally SH4 has a multiplex data/address mode (MPX). It is directly connected to the SDRAM and uses CS3# for chip selection. CS3#area can be accessed in ラスdown mode.

The SH4 system memory map is divided into 7 areas. Each area is defined by an address and 7 decoded external chip selections become (CS#[6:0]) output.

Table 2-6 is the memory map and area configuration. For details on each function, refer to the relevant section.

Area	*Physical Address*	*Type*	*Function*	*Size*	*Access*	*Note*
0 (CS1)	$00000000 - $001FFFFF	MPX	Boot ROM	2MB	1/2/4/32B	
	$00200000 - $0021FFFF		Flash Memory	128KB	1/2/4/32B	
	$005F6800 - $005F69FF		System Control Reg.	512B	4B	
	$005F6C00 - $005F6CFF		Maple Control Reg.	256B	4B	
	$005F7000 - $005F70FF		GD-ROM	256B	1/2B	
	$005F7400 - $005F74FF		G1 Control Reg.	256B	4B	
	$005F7800 - $005F78FF		G2 Control Reg.	256B	4B	
	$005F7C00 - $005F7CFF		PVR Control Reg.	256B	4B	
	$005F8000 - $005F9FFF		TA/PVR Core Reg.	8KB	4/32B	
	$00600000 - $006007FF		MODEM	2KB	1B	
	$00700000 - $00707FFF		AICA sound Reg.	32KB	4B	
	$00710000 - $00710007		AICA RTC Reg.	8B	4B	
	$00800000 - $009FFFFF		AICA Memory	2MB	4B	
	$01000000 - $01FFFFFF		G2 External area	16MB	1/2/4/32B	
1 (CS1)	$04000000 - $047FFFFF	MPX	Texture Mem.(64bit)	8MB	2/4/32B	(RD/WR)
	$05000000 - $057FFFFF		Texture Mem. (32bit)	8MB	2/4/32B	(RD/WR)
2 (CS2)	$08000000 - $0BFFFFFF	-	*Unassigned*	64MB	-	Reserve
3 (CS3)	$0C000000 - $0C7FFFFF	SDRAM	Work SDRAM	16MB	1/2/4/32B	Main Memory
4 (CS4)	$10000000 - $107FFFFF	MPX	Polygon Converter	8Mbyte	32B	TA FIFO
	$10800000 - $10FFFFFF		YUV Converter	8Mbyte	32B	TA FIFO
	$11000000 - $117FFFFF		Texture Mem. (WR)	8Mbyte	32B	(WR only)
5 (CS5)	$14000000 - $17FFFFFF	MPX	Ex. Device	64MB	1/2/4/32B	
6 (CS6)	$18000000 - $1BFFFFFF	-	*Unassigned*	64MB	64MB	reserve

Table 2-6 memory mapping

2.5 CPU bus interface

SH4 uses 2 different bus protocols depending on the area of the CPU bus. Depending on which memory area is accessed, one of the 2 choices below is selected.

1) Direct operation to the SDRAM
2) MPX operation to HOLLY

The MPX interface is an interface for the multiplex address/data. With respect to areas 0,1,4 and 5 of SH4, MPX operation is possible.

<1> area 0 = Boot ROM, GD-ROM, modem, HOLLY/AICA control register, external device area
<2> area 1 = Texture memory access
<3> area 4 = TA area within HOLLY (FIFO, YUV converter, texture memory access)
<4> area 5 = external device area on the G2 bus.

With regards to direct operations involving the SDRAM, please refer to the previous section titled SDRAM control.

2.6 Interrupt

With regards to interruptions from the exterior of SH4, the following exist.

- NMI interrupt
- SH4 external interrupt(Level Trigger)

The debugging adapter controls JTAG interruptions.
(The debugging adapter is a software development tool that allows the reset of the Dreamcast system and JTAG interruptions etc.)
NMI is not used.
SH4 external interruptions (as a signal it is CIRL [2:1]) are controlled by HOLLY. Interruptions from HOLLY to SH4 are from HOLLY internally and from each device on the G1/G2 bus.

- HOLLY internally (PVR2 core, DMA part) interrupt…level trigger
- GD-ROM interruption (interruption from the G1 bus)
- AICA interruption (interruption from the G2 bus)
- MODEM interruption (interruption from the G2 bus)
- Reserve (interruption from external device connected to the G2 bus)

The outline of the connection is described in diagram 2-2 below.
If an interruption occurs from within HOLLY, GD-ROM, AICA, RESERVE etc., HOLLY will maintain the status in its internal register and record the interrupt signal as level 'L'. (It allows signal level changes of IRL#[2:1]. With regards to the other IRL#0,3 signals, it is connected to the 'H' level) When the interrupt signal becomes level 'L', SH4 will read the HOLLY internal interruption register and jump to the appropriate vector routine interruption.

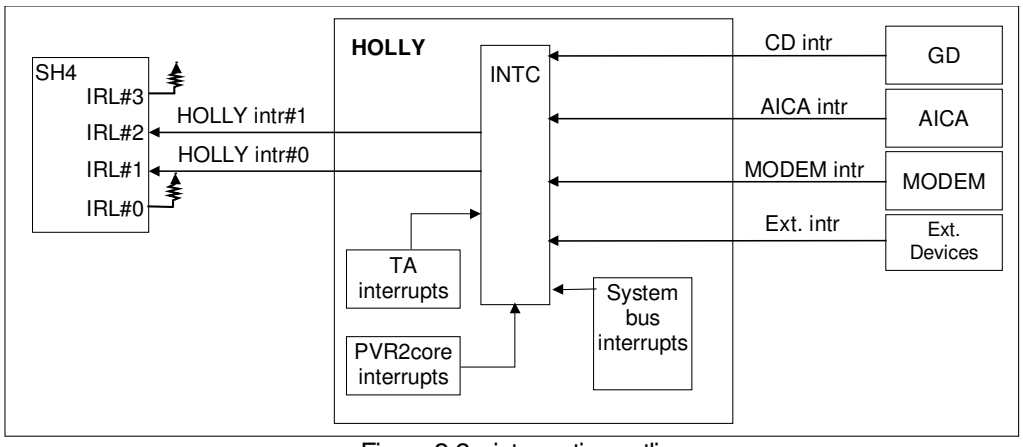


Figure 2-2 interruption outline

2.7 PIO i/f

The SH4 PIO interface is used in the reading of the Dreamcast system image mode settings. The allocation of each signal line of the PIO interface (PIO [9:0]) is described in figure 2-3 and table 2-7.

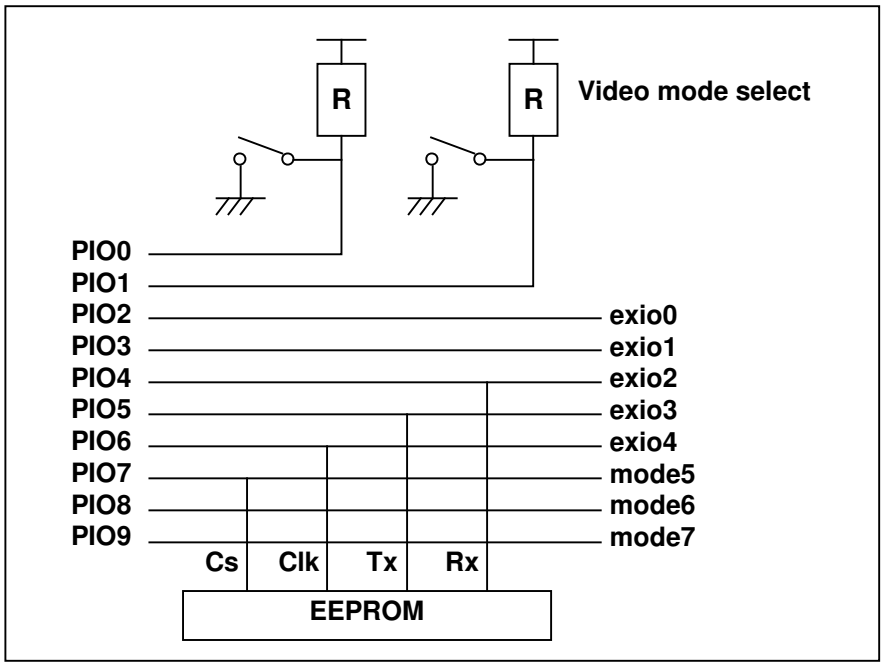


Figure 2-3 Allocation of PIO[9:0]

2.8 SCI i/f

SH4 has 2 serial interfaces (SCI) . With regard to the Dreamcast system, only one of these is a multi-purpose serial port in the console that is supported.

--End of CPU--

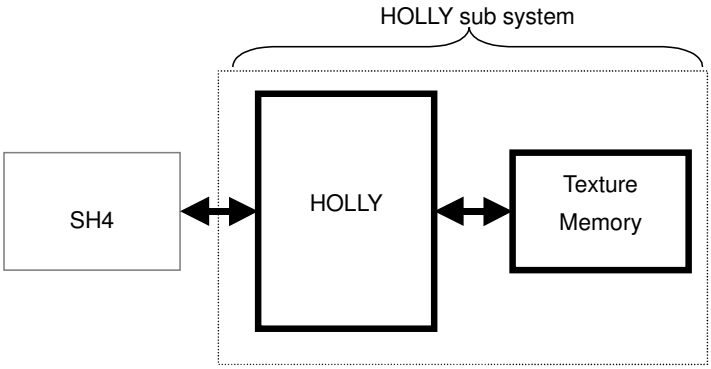
3 Draw image processor: HOLLY

The HOLLY chip is a product-version Dreamcast graphics processor with a built-in PowerVR2 core, which is part of the Power VR family and the next generation game console version after the PC PowerVR PCX2.

The internal part of HOLLY is divided into the system bus and core.

The system bus is an interface between the SH4 and Core, G1, G2, game pad and especially controls DMA movements.

The core is only used to draw images. From SH4 it is accessed through the system bus. Additionally with PCX2, flat parameter generation and tile parameter generation which was perofrmed by Pentium(R) has completely become converted to hardware and made faster.



3.1 HOLLY subsystem

Figure 3-1 is the HOLLY sub system.

* With regards to an explanation about the pin, refer to the pin list 0.

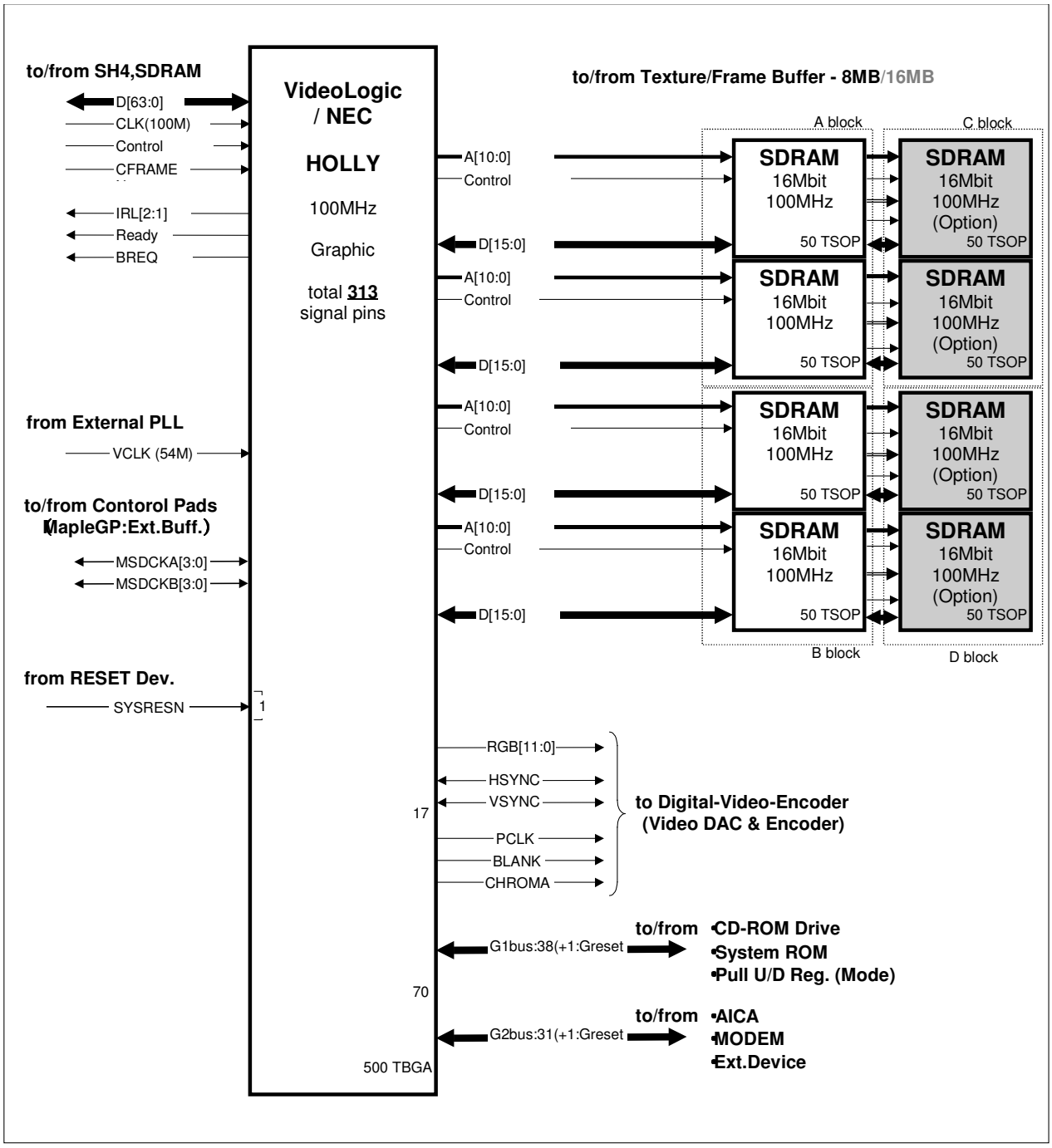


Figure 3-1 Block diagram of the HOLLY sub system

3.2 Chip specification

The main chip specifications for HOLLY are described below.

- Package 500pin T－BGA
- Process 0.2μm
- SH4 i/f clock 100MHz
- Draw image clock 100MHz
- Pixel clock 13.5MHz (Input 54Hz from the external PLL is internally 分周 before use.)
- Power supply DC2.4/3.3V (core 2.4V, all signal pins 3.3V. 5V pressure-withstanding pins are not supported)

3.3 List of pins

The pin list of the HOLLY chip is below.

If the first letter of the signal name is 'C', it is a CPU bus related signal while ones starting with 'L' are texture memory related signals.

Additionally the texture memories of blocks C and D are only connected when the texture memory is at 16MB. Normally (at 8MB), nothing will be connected.

Pin name	i/o	Explanation
System-related signals		
SYSRESN	input	Resets whole of HOLLY
VCLK	input	Displayed clock(13.5MHz) Not synchronised with the draw image clock
TESTN	input	The test pin of the chip 0:chip testing mode 1: normal operation
Pin name	i/o	Explanation
CPU related signal		
CCKIO	input	The operational clock of the chip. Connects the CPU clock
CCs[5,4,1,0]N	input	Connects SH4 /CS n
CFRAMEN	input	Connects SH4 /FRAME
CRDWR	input	Connects the SH4 /RDWR 0:write 1:read
CIRL[2:1]N	output	Interrupts the CPU
CRDYN	output	CPU /READY
CDBREQN	output	CPU /Data Bus Request
CBAVLN	input	CPU /Bus Availability
CTRN	output	DMA-Transfer Request
CTDACKN	input	DMA-Transfer Data Acknowledge
CID[1:0]	input	DMA-Channel number
CAD[63:0]	In/output	CPU address/data multiplex bus
Pin name	i/o	Details

Texture memory related signals		
SDACLK	Output	Blocks A and C (32 bit) texture memory clock ** C is only used in 16MB expansion.
SDBCLK	Output	B and D (32bit) texture memory clock ** D is only used in 16MB expansion.
SDACS0N	Output	Block A- chip selection
SDBCS0N	Output	Block B- chip selection
SDACS1N	output	Block C- chip selection (only used in 16MB expansion)
SDBCS1N	output	Block D- chip selection (only used in 16MB expansion)
SDARASN	output	Blocks A and C- RAS
SDBRASN	output	Blocks B and D- RAS
SDACASN	output	Blocks A and C- CAS
SDBCASN	output	Blocks B and D- CAS
SDA[1:0]DQM	output	Block A- DQM
SDB[1:0]DQM	output	Block B- DQM
SDAWEN	output	Blocks A and C- write
SDBWEN	output	Blocks B and D- write
SDA0A[10:0]	output	Blocks A and C- address0
SDA1A[10:0]	output	Blocks A and C- address1
SDB0A[10:0]	output	Blocks B and D - address0
SDB1A[10:0]	output	Blocks B and D- address1
SDAA11	output	Blocks A and C- address
SDBA11	output	Blocks B and D- address
SDA0D[15:0]	In/output	Blocks A and C- lowest data[15:0]
SDA1D[31:16]	In/output	Blocks A and C- highest data[31:16]
SDB0D[15:0]	In/output	Blocks B and D- lowest data[15:0]
SDB1D[31:16]	In/output	Blocks B and D- highest data[31:16]
Pin name	i/o	Explanation
Common Signals		
GRESN	output	Reset for device
Pin name	i/o	Explanation
G1 bus related signals		
G1D[7:0]	In/output	G1 data bus-lowest 8bit
G1RAD[15:8]	In/output	G1data bus- highest 8bit Adapted to ROM address[7:0]
G1RAL[10:8]	Output	ROM address[10:8]
G1MRA[18:11]	In/output	Mode ROM address[18:11]

G1RAH[20:19]	Output	ROM address[20:19]
G1CS[1:0]N	Output	GD-ROM chip selection
G1ROMCSN	Output	Boot ROM chip selection
G1FMCSN	output	Flash memory chip selection
G1RDN	output	Boot ROM read signal
G1WRN	output	Boot ROM light signal (for Flash ROM, normally not connected)
G1IORDY	input	GD-ROM IO ready
G1DREQ	input	GD-ROM DMA request
G1DACKN	output	GD-ROM DMA acknowledge
G1INTRQ	input	GD-ROM interrupt
Pin name	i/o	Explanation
G2 bus related signals		
G2AD[15:0]	In/output	Address/data multiplex bus
G2BHN	output	Highest data(G2AD[15:8]) valid
G2BLN	output	Lowest data(G2AD[7:0]) valid
G2FRN	output	Frame signal
G2CLK	output	G2bus/clock
G2TRN	input	/TargetReady
G2DSN	In/output	/DeviceSelect
G2STN	Input	/Stop
G2RQAICN	Input	AICA /TransferRequest
G2RQEX0N	Input	External Device0 /TransferRequest
G2RQEX1N	Input	External Device1 /TransferRequest
G2RQDEVN	Input	Debugger /TransferRequest
G2MDMCSN	Output	Modem chip select
G2IRAICN	Input	AICA interruption
G2IRMDMN	Input	Modem interruption
G2IREXTN	Input	External device interrupt
Pin name	i/o	Explanation
Video related signal		
HSYNC	In/output	Horizontally synchronised TV signal Becomes slave (input) due to the register signals Just after reset, it is slave mode
VSYNC	In/output	Vertically synchronised TV signals Becomes slave (input) due to the register settings Just after reset, it is slave mode
PCLK	Output	Pixel clock
BLANK	Output	Blanking signal 0:blanking

CHROMA	output	Chroma key fix signal 0: transparent pixel
RGB[11:0]	output	Highest or the lowest 'bit' of pixel data 1 pixel is 24 bit
Pin name	i/o	Explanation
G1 bus related signal		
MSDCKA[3:0]	In/output	Game pad/ bus A side
MSDCKB[3:0]	In/output	Game pad/ bus B side

Table 3-1

3.4 Texture (Texture/Frame Buffer) Memory

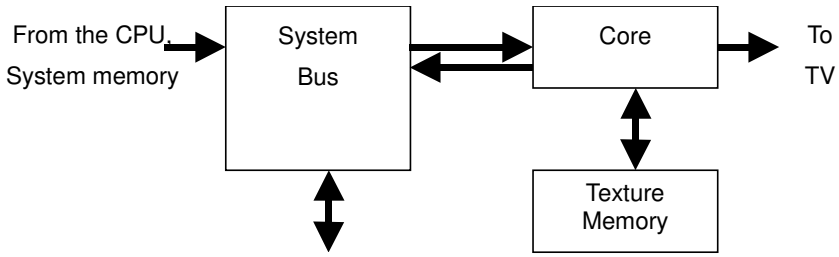
HOLLY is connected to a 16Mbit SDRAM×4 memory 8MB(can expand up to 16MB) memory which is accessed at 100MHz and allows 16/32/64 bit data access. 1 byte access is not supported. 32 bit SDRAM does not allow specification. Table 3-1 below describes details of the used memory in the Dreamcast base system.

Memory space	8 MB(16Mbit×4)
Technology	16 M bit SDRAM (2 x 256k x 16bit) x 4
Total bus width	64bit(16/32 bit access possible but 8 bit is not)
Bus width of 1 chip	16 bit
Frequency	100 MHz
BBW	800 MB/s

Figure 3-1 HOLLY texture/frame buffer memory specification

3.5 Internal configuration- Part1

The interior of HOLLY is divided into the following 2 parts.



3.5.1 System Bus

Access from the CPU, with some exceptions, occurs through the system bus block.

The system bus is suitable for the DMA of the CPU. It is also suitable for single access of the CPU but due to its transfer capabilities, use from the DMA is recommended.

3.5.2 Core

The drawing of images occur through this block.

Access to the core block is through the system bus block. (Described earlier)

The types of access are described below.

- transfer of the polygon list (draw image)
- writing texture data
- reading texture RAM
- Reading and writing of the core register

3.6 Internal configuration- Part 2

The 3 blocks described below basically configure HOLLY.

3.6.1 PVR block

This is a rendering engine and includes the PVR 2 core as well as the texture memory arbiter.

3.6.2 Tile Accelerator(TA) block

This is a block that converts writing from the CPU or polygon data transferred from the main memory through the DMA, and uses the hardware to convert it into PowerVR format and includes YUV conversion, FPU etc.

3.6.3 System bus block

This is a block that transfers data from each block inside HOLLY to the internal bus. Transfer between the main memory and each device connected to HOLLY uses the SH4 DMA (DDT mode).

Below is an explanation of the bus configuration and each interface block.

The configuration is such that each interface block within the system bus block sandwiches the root bus , and access between each device is via the root bus. The root bus has a bus width of 32bit and an operational clock of 50MHz. The data transferring speed including arbitration is 123MHz (13clk/32B).

Each interface block connected to the root bus is described below.

- **SH4 i/f**

The HITACHI SH4 (internal 200MHz operation), which is the CPU, is an interface for accessing the root bus and connected to the 64 bit A/D (MPX) bus. It is accessed from areas CS0, CS1, CS5 where wait control is possible

- **DDT i/f**

This uses the SH4 DDT function to access the CPU main memory. The device on the root bus becomes the master bus and if you use DMA transferring to the main memory, DDT i/f becomes the target of each device from and is transferred to the main memory. Additionally it controls DMA access from the main memory .

- **PVR i/f**

This is the master/target device of the root bus and performs transfers between the PVR block and the TA block (access register). The data transfer is in units of 32B. There is also a DMA function.

- **Maple i/f**

This is a root bus master/ target device that transfers between the control pad etc. and maple device. The data is transferred in units of 32B. There is also a DMA function.

- **G1 bus i/f**

This is the master/ target device of the root bus and performs the transfer between the GD-ROM drive connected to the bus and the ROM/FLASH. The data is transferred in units of 32B. There is also a DMA function.

- **G2 bus i/f**

This is a master/ target device on the root bus and performs the transfer between the audio chip AICA, that is connected to the bus, the modem and the optional external device. The data is transferred in units of 32B. There is also a DMA function.

The ' Bus Arbiter ' (connected to the root bus) performs the arbitration of the root bus and is set from SH4. It is connected to the SH4 i/f.

3.7 Outline of drawing images

HOLLY's image drawing specifications are described below.

- Tile data generation by the hardware
- Removal of the backface polygon due to the hardware (select from register)

- draw image primitive: triangle (can strip) and quadrilateral (can not strip)
- Triangle strip (1～∞)
- Flat shading

- Texture colour：ARGB1555,565,4444
- On-chip palette: 2K byte
- YUV420,422
- Quantumise shrink texture: can shrink up to 1/4 ~1/8
- Rectangular texture, twiddle texture
- Cramp texture co-ordinates , flipping (mirroring)
- Chroma key fix

- Perspective texture mapping
- MIP map
- texture filtering：
  - point sampling
  – bilinear filtering
  – trilinear filtering
  – unisotropic filtering (Unisotropic)
- grow shading (RGBA specification /intensity specification can be selected)
- Specular Highlight
- Shadow (within shadow volume it displays separate texture)
- Simple reduce brightness shadow (1/4,1/2,3/4 simple shadow)
- 4x4 dithering
- rectangular clipping of pixel unit or tile unit
- colour cramp
- Fog：LUT method, linear/Exp.
- Fog colour settings are possible.
- Interpolation of the maxima α
- α blending: Open GL compatible
- automatic sorting of α polygon possible
- Depth comparison: Open GL compatible
- Edge anti-aliasing
- BAMP mapping

- 16.7 million colours displayed
- Flicker filtering

- Internal 3D pixel format: 32BPP RGBA (16bit texture is expanded 24bit internally, then used.)
- CPU co-ordinate data format: 32bit , minimum number of fluctuations(IEEE754)
- Texture cache size: 128 entry

Etc.

Table 3-2 describes the NTSC/PAL modes suites to HOLLY.

With regard to the interlace mode, 'single density' displays the same image as the EVEN/ ODD field and 'double density' displays a different image to the EVEN/ODD field. Double density is better for the vertical resolution when viewing but the 'flicker' phenomenon occurs. In this case, if you use the mode where you assign part of HOLLY's texture memory as the frame buffer, flickers are reduced.

Resolution	**Refresh rate and interlace mode**	**Reference**
320x240	60 Hz non-interlace	NTSC low-res non-interlace
320x240	30 Hz interlace	NTSC low-res single density interlace
640x240	60 Hz non-interlace	NTSC high-res. Non-interlace
640x240	30 Hz interlace	NTSC high-res. single density interlace
640x480	30 Hz interlace	NTSC double density interlace (Flicker free possible)
320x240	50 Hz non-interlace	PAL low-res non-interlace
320x240	25 Hz interlace	PAL low-res single density interlace
640x240	50 Hz non-interlace	PAL high-res. non-interlace
640x240	25 Hz interlace	PAL high-res. single density interlace
640x480	25 Hz interlace	PAL double density interlace (Flicker free possible)

Table 3-2 NTSC/PAL resolution display

The texture memory stores the data below in the shared memory. Although it does not have the transfer capability of the system memory, the CPU can be used as a work area.

- texture data
- frame buffer

When displaying the interlace, depending on what colour is displayed, the flickering lustre may be annoying. This is called 'flicker' and the Dreamcast system supports the flicker filtering functions that are described below.

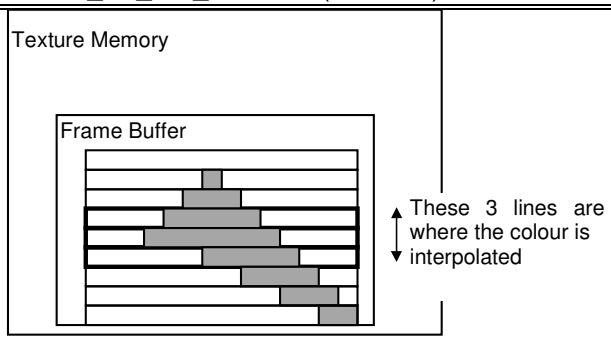


Diagram 3-2 Flicker filtering

Apart from the NTSC/PAL display mode, HOLLY uses settings from SH4 to display the VGA resolution that you can select from table 3-3. Additionally VGA monitor output from the Dreamcast console is not adapted for the A/ V connector but for another special connector.

Resolution	Refresh rate and interlace mode	Note
640x480	60Hz non interlace	VGA

Table 3-3 VGA Resolution

3.8 External interface specification

The interface specifications of HOLLY and each supported device are described below.

G1 bus

The G1 bus is connected to the GD-ROM drive and the ROM/ FLASH (space 2MB and bus width 8bit). Access to the GD-ROM uses an interface similar to EIDE (similar to ATA) but part of the bus signal line has multiplexed signal lines that are used for ROM/FLASH access. Additionally part of the address line to ROM/FLASH has multiplexed MODE signals which are incorporated in the system information. The bus operation is not synchronised and at the time of GD-ROM access the data bus width is 16 bit although at the time of ROM/FLASH access, it is 8 bit. The real transfer speed at the time of GD-ROM access is 10MB/s (2880ns/32B).

G2 bus

G2 bus is a bus like PCI that has an operational 25MHz clock and a bus width of 16 bit and is in parallel connection to the audio IC AICA, the modem and the optional external device. The real transfer speed is 40MB/s (19 clk/32B).

Maple

This is an original Sega peripheral interface that supports the connection of peripheral devices such as the control pad and backup media. Up to 4 ports can be connected. Data transmission occurs by the synchronised serial method. The maximum data transfer rate is 2Mbps and the real transfer speed of the port is 128KB/s. With regard to details on specifications, refer to Appendix. Maple i/f or other material.

3.9 Data path

The data path between HOLLY and each device is described below.

1) The following types of access are possible from SH4 to each block or device.

- write (only) from the (**SH4**) to the (**TA block(data FIFO)**)

  (Add 'It goes through SH4i/f and ' to the beginning of the next 4 lines.)

  PVR i/f then reads/writes to the (**texture memory**), (**PVR2 core**) and (**TA block (register)**)

  Maple i/f then reads/writes to the (**Maple Device**)

  G1 bus i/f then reads/writes to the (**ROM/FLASH**) and (**GD-ROM drive**)

  G2 bus i/f then reads/writes to the (**AICA (register/memory)**), (**MODEM**) and (**optional external device**)

2) The main paths supporting DMA transfer access from each device other than SH4 are described below.

- write (only) from (**main memory**) to (**TA block (data FIFO)**)
- read/write from (**Maple device**) to (**main memory**), (**PVR2 core**) and (**each G2 device**)
- read/write from (**each G1 device**) to (**main memory**), (**PVR2 core**) and (**each G2 device**)
- read/write from (**each G2 device**) to (**main memory**) and (**PVR2 core**)

For details on the G1/G2 bus cycle, timing etc and the bus specifications, refer to the material on each bus. Also, for details on the specifications of each device on the bus, refer to each relevant section. Regarding the locations of each G1/G2 device from SH4 (address: memory) map, refer to the section (CPU: SH4) titled memory map.

3.10 Interruption processing by HOLLY

HOLLY is the interrupt master for SH4 and is subject to interruption signals from each block or from each device connected to the interface and has a INTERRUPT CONTROLLER which generates interruptions to SH4. When interruptions are generated from each block, HOLLY will internally store the status of each interruption on the interrupt register and assign a change in level for SH4 IRL1, 2. Each type of interruption can be masked and the INTERRUPT CONTROLLER performs masks or clears.

As stated before, there are 2 types of interruptions- ones from the interior of HOLLY such as the PVR2 core block and ones from each device connected to the G1/G2 bus. With regards to the reasons for these interruptions, please read the descriptions for each block below. (For the processing of SH4 interruptions please refer to the section (CPU: SH4). It will be under Interruptions.)

Below are the interruptions for each interface block within the '**System Bus Block**'.

* PVR i/f

- DMA End (Completion of DMA transfer: same for below)
- PVR Illegal address set
- DMA over run

* Maple i/f

- DMA End
- V Blank over
- DMA over run
- Write FIFO Overflow
- Illegal command
- Illegal addressing

* G1 bus i/f

- DMA End
- Illegal Address set
- DMA over run
- ROM/FLASH access at DMA
- From GD-ROM drive (Interruption from the GD-ROM)

* G2 bus i/f

- DMA(AICA)End
- DMA(Ex0)End
- DMA(Ex1)End
- DMA(Dev)End
- DMA(AICA)Illegal address set
- DMA(Ex0)Illegal Address set
- DMA(Ex1)Illegal Address set
- DMA(Dev)Illegal Address set

- DMA(AICA)over run
- DMA(Ex0)over run
- DMA(Ex1)over run
- DMA(Dev)over run
- Time out
- From AICA(Interruption from the sound chip AICA)
- From Modem (interruption from the modem)
- From ExDEV(interruption from the optional external device)

* DDT i/f

- DMA(ch2) completed
- Sort DMA Command Error

* SH4 i/f

- Time out
- Accessing to inhibited area

* Bus Arbiter

- Root Bus Reset Time Out

Interruptions from the '**PVR core block**' are described below.

- V blank in (Once at the starting point)
- V blank out (1 line before that display starts)
- H Blank In: each H, several H and/or select from the specified line of the register
- End of Render ISP
- End of Render TSP
- End of Render Video
- Hazard Processing (This occurs when you are using Strip Buffer and draw image does not occur on time.)
- ISP Out of Cache (Overflow of ISP Buffer)

Interruptions from the '**Tile Accelerator Block**' are described below.

- End of Opaque (Transfer of Opaque Polygon complete)
- End of Translucent (Transfer of Translucent Polygon complete)
- End of Opaque Modifier (Transfer of Opaque Modifier Volume complete)
- End of Translucent Modifier (Transfer of Translucent Modifier Volume complete)
- End of YUV Transfer (Transfer of YUV422 data complete)
- ISP/TSP Parameter Over flow ISP or overflow of TSP parameter)
- Object List Overflow (Object List Pointer Overflow)
- FIFO Overflow (FIFO Overflow)
- Illegal Parameter (Occurrence of abnormal data)

4 Audio processor : AICA

AICA which is a YAMAHA made audio IC, is a refined version of the audio IC SCSP used in the Sega Saturn. With respect to the Dreamcast system it generates 64ch PCM / ADPCM /stereo sound.

4.1 AICA peripheral connection

Figure 4-1 is a connection diagram of AICA peripherals.

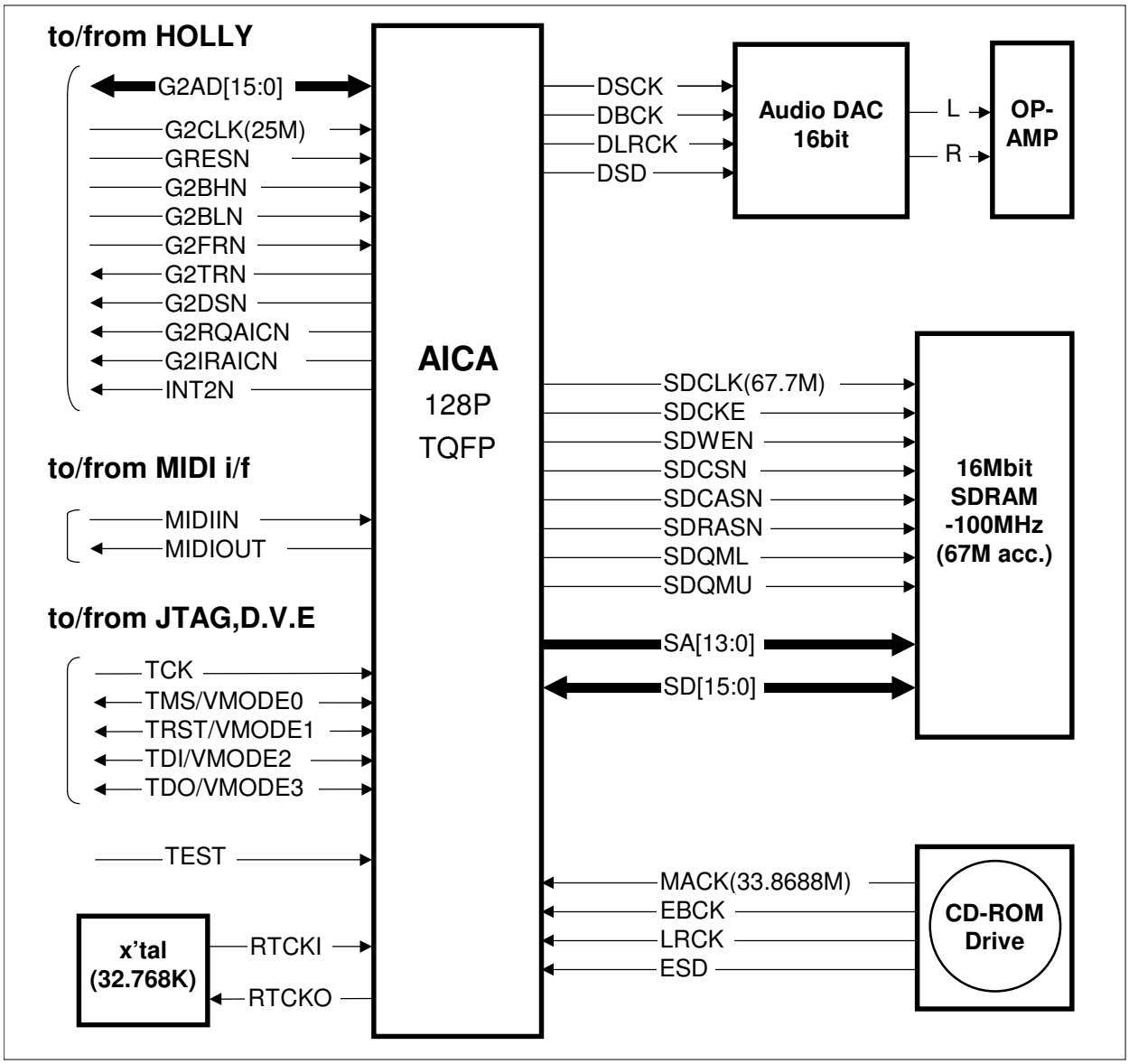


Figure 4-1 AICA peripheral connection diagram

4.2 Chip specification

The main chip specifications for AICA are described below.

- Package 128pin TQFP
- Process 0.35μm
- sound source clock 22.5792MHz
- system i/f clock 25.0MHz
- Power supply 3.3V

4.3 pin specification

Table 4-1 below contains the specifications of the signal pin.

PIN NAME	I/O	FREQ.	DESCRIPTION	I/F level
VDD3			System's 3.3V power supply	
VRTC			Power supply pin to RTCpin	
VSS			System's GND pin	
G2CLK	I	25M	Clock signal used by the HOLLY I/F(G2 BUS) block	LVTTL
G2AD[15:0]	I/O	25M	Address signal pin used by the HOLLY I/F(G2 BUS)	LVTTL
G2BHN	I	25M	Signal pin used by the HOLLY I/F(G2BUS) and represents the 'High Enable' of data or the bus mode	LVTTL
G2BLN	I	25M	Signal pin used by the HOLLY I/F (G2BUS) and represents the 'Low Enable' of data or the bus mode.	LVTTL
G2FRN	I	25M	With respect to the G2 BUS I/F, it is a signal pin that represents the start or completion of a cycle.	LVTTL
G2TRN	O	25M	With respect to the G2 BUS I/F, it is used to control the cycle	LVTTL
G2DSN	O	25M	With respect to the G2 BUS I/F, it is used to control the cycle	LVTTL
G2RQAICN	O	25M	This is a signal pin used by the HOLLY I/F (G2 BUS) and is a DMA request signal.	LVTTL
GRESETN	I		This is a system reset signal from HOLLY(G2 BUS)	LVTTL
G2IRAICN	O		interrupt signal from AICA	LVTTL
MACK	I	1024Fs	Sound block clock(Fs = 44.1KHz)	LVTTL
ESD1	I	1024Fs	Digital Audio Data #1 from outside	LVTTL
EBCK1	I	1024Fs	Digital Audio Clock #1 from outside	LVTTL
LRCK1	I	1024Fs	Digital Audio LR Clock #1 from outside	LVTTL
ESD2	I	1024Fs	Digital Audio Data #2 from outside	LVTTL
EBCK2	I	1024Fs	Digital Audio Clock #2 from outside	LVTTL
LRCK2	I	1024Fs	Digital Audio LR Clock #2 from outside	LVTTL
DSCK	O	256Fs	clock signal to external DAC	LVTTL
DSD	O	44.1K	Digital Audio Data to external DAC	LVTTL
DBCK	O	44.1K	Digital Audio Clock to external DAC	LVTTL
DLRCK	O	44.1K	Digital Audio LR Clock to external DAC	LVTTL
MIDIIN	I		MIDI interface signal	LVTTL
MIDIOUT	O		MIDI interface signal	LVTTL
SD[15:0]	I/O	67.8M	Wave Memory(external SDRAM)Data	LVTTL
SA[13:0]	O	67.8M	Wave Memory Address output	LVTTL
SDQML	O	67.8M	Control signal to Wave Memory	LVTTL
SDQMU	O	67.8M	Control signal to Wave Memory	LVTTL
SDCLK	O	67.8M	Clock signal to Wave Memory	LVTTL
SDCKE	O	67.8M	Clock enable signal to Wave Memory	LVTTL
SDWEN	O	67.8M	control signal(write) to wave memory	LVTTL
SDCSN	O	67.8M	control signal(chip select) to wave memory	LVTTL
SDCASN	O	67.8M	control signal(CAS) to wave memory	LVTTL
SDRASN	O	67.8M	control signal(RAS) to wave memory	LVTTL
RTCKI	I	32K	Clock pin for RTC	LVTTL
RTCKO	O	32K	clock pin for RTC	LVTTL
TCK	I		Clock signal for JTAG I/F	LVTTL
VMODE0/TMS	I		Mode signal to DVE(VideoDAC.Encoder) / JTAG Mode Selection	LVTTL
VMODE1/TRST	I		mode signal to DVE / JTAG reset signal	LVTTL
VMODE2/TDI	I		mode signal to DVE / JTAG data input signal	LVTTL
VMODE3/TDO	O		mode signal to DVE / JTAG data output signal	LVTTL
TEST	I		mode signal to DVE and JTAG I/F switching signal	LVTTL

Table 4-1 AICA signal pin list

4.4 Main configuration and spec

Figure 4-2 is a block diagram of the interior of AICA.

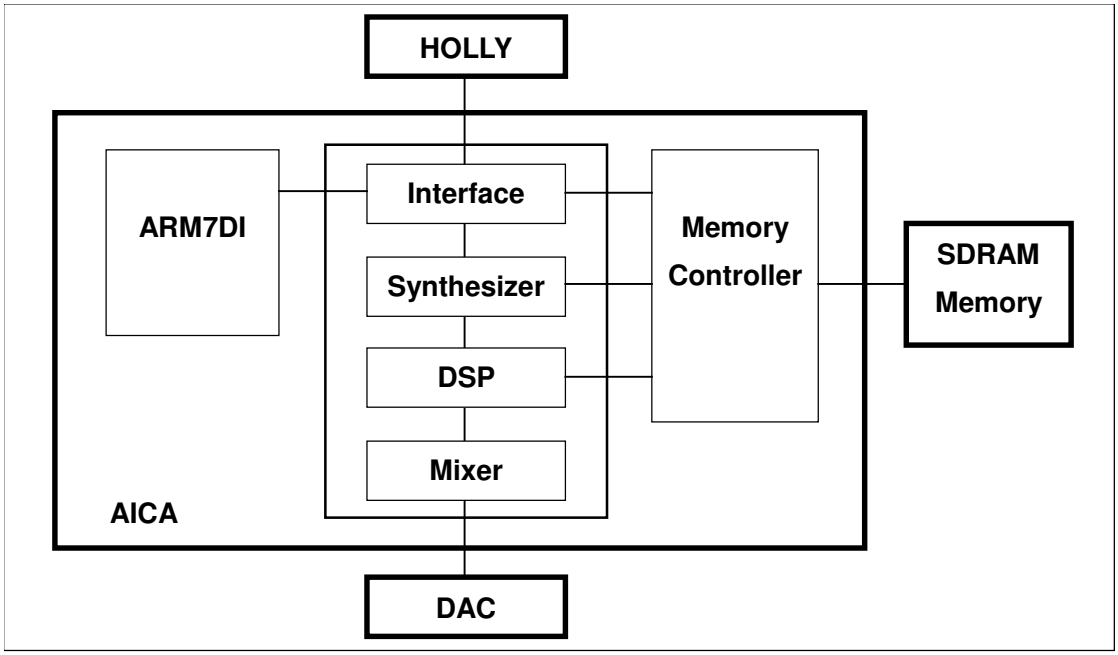


Figure 4-2 block diagram of the interior of AICA

The main block configuration of AICA is divided into the sound block (sound source part) and internal CPU and secondly the memory i/f block. The sound block is a block that includes the interface part, sound source part and the DSP part. The interface part is a block that is an interface of exchange with the Dreamcast system, through the internal CPU and the HOLLY G2 bus i/f, including SH4, RTC and MIDI. The internal CPU uses ARM7DI. The step of DSP is 128 step. The external memory uses the SDRAM (explained later). The sound block and the the internal CPU has a 22.5792MHz clock supplied from the GD-ROM drive and just like the memory i/f, it is 67.7376MHz from the GD-ROM drive clock. The HOLLY i/f is a 25 MHz clock supplied from the G2 bus.

With regard to external sound input, there are 2 types of audio signal input. With the Dreamcast system, there is 1 type of input from the GD-ROM drive GD-DA (LRCK, BCK, and SDATA). As stated before, the 33.8688 MHz clock supplied from the GD-ROM drive is converted to the sampling frequency 44.1KHz in the internal PLL, operational sound block clock as well as the memory i/f clock.

Apart from the memory i/f shared by each block (external SDRAM), AICA has 2, 3V Lithium batteries attached which allows the support of RTC (Real Time Clock) with backup and the MIDI i/f used for development. The internal CPU supports the JTAG i/f.

The specification of the sound source part is displayed in table 4-2 and represents the main sound source specs for AICA. The maximum number of simultaneous sounds is 64 sounds and each slot has an independent LFO. The ADPCM is a maximum of 1oct and the pitch can be changed. The PCM format is 8/16bit Liner, 4bit ADPCM.

PCM channel	64ch	ADPCM and combined use
PCM format	16bit / 8bit	
ADPCM decoder	64ch	PCM and combined use, 4bit ->16bit
Time fluctuation filter	64ch	Features 64Ch 4 segment EG suitable for time fluctuation filter
Monaural MIX	Hard	Volume adjusted by using the master volume
Loop	Forward	
Sampling frequency	44.1KHz	

Table 4-2 main sound source spec

4.5 Audio Memory

The (audio) memory that is externally connected to AICA is shared by the internal CPU and/or the sound source within the sound block, DSP and the external i/f. Table 4-2 shows the details used by the memory.

Memory space	2MB (can be expanded to a maximum of 8MB)
Technology	16Mbit SDRAM (2 bank x 512kword x 16bit)
Number of memory chips used	1
Bus Width of chip	16 bit
Operational specification CLT	2(fixed)
Operational specification BL	Full Page (fixed)
Frequency	67.7376MHz

Table 4-2 AICA audio memory specification

4.6 RTC (Real Time Clock)

AICA has an internal chip with a RTC (Real Time Clock) operating at 2.0~3.5V. AICA has 3V lithium battery for the RTC that can be used for battery back up. The 32.768 kHz x'tal used as the clock source is also attached. The power consumed is less than 10μA and the battery backup period is approximately 270 days. (Battery equivalent to ML3032 when recharging.)

4.7 Audio In/Output

Digital audio signals created by AICA can be mixed with the digital audio signal input from the GD-ROM drive 48Fs(=2.1168MHz) and the output passes through the external analogue DAC and/or the encoder and becomes output from the RCA connector and the expansion VGA connector. The external analogue DAC has 256Fs(=11.2896MHz) clock and/or 64Fs(=2.8224MHz) Digital Audio (DSD, DBCK, DLRCK) output.
(AICA has 2 types of Digital Audio input but the Dreamcast system only uses the one from the GD-ROM drive.)

4.8 Setting the image mode

AICA has a register that sets the various types of Dreamcast image (video) modes such as NTSC/PAL and VGA that are accessed from SH4. The content of that register reflects the image mode set by the draw image processor HOLLY from SH4. From AICA the image mode depending on the register value becomes mode signal(VMODE0～3) output from the D.V.E (Digital Video Encoder).
With regards to image mode settings please refer to 7.4 (video output and/or image mode setting method)

4.9 MIDI interface

The MIDI interface (MIDI IN/OUT) is supported for audio development.
MIDI interface becomes a 3.3V signal output to G2 i/f.

4.10 Interrupt

Interruptions are generated through the G2 bus and against HOLLY. Interruptions from the sound block are a type of interruption generated by AICA internally.
For details on interruptions refer to the sections (CPU: SH4) and (draw image processor HOLLY)

-- End of AICA --

5 Boot ROM

The Boot ROM is mapped to area0of SH4 and is accessed by the CPU. With respect to its location on the system, it is connected to the multiplexed G1 bus from the HOLLY ROM i/f. The G1 bus only has an 8 bit ROM interface when the SH4 Boot ROM is accessed.

5.1 Boot ROM configuration

The Boot ROM stores the data described below.

There are 2MB of ROM space. Table 5-1 contains estimates for the amounts of space used for data within the Boot ROM.

Details of the data	Necessary space
IPL	0.25MB
Multi player (includes draw image/audio data)	0.75MB
Kanji Font	1MB
TOTAL	2MB

Table 5-1 Details of the ROM data

5.2 Specifying a ROM

The ROM is a 16M bit (2MB) mask ROM with a 8 bit bus width and has an access time of 100~240ns.

The table below is the specified ROM details used by the Dreamcast system.

ROM type	Mask ROM
ROM size	16Mbit
Bus width	8 bit
Access time	100ns～240ns

Table 5-2 Specifying ROM

5.3 About the access cycle to the ROM

As stated previously the Boot ROM is located on the G1bus. With regards to the bus cycle set-up or hold of an address, reading and writing is possible. The pulse width can be specified through the HOLLY register. Regarding the number of access cycles, 1 byte, 2 byte and 4-byte access is possible.

-- End of Boot ROM--

6 GD-ROM

The GD-ROM drive incorporated in the Dreamcast system is connected to the G1 bus which has HOLLY as the master and the GD-ROM data goes through HOLLY before it is read by the CPU. The reading of data is by the CAV method and the transferring of data is approximately 4 times the speed in the normal area and approximately 6~12 times the speed in the high-density area. It is stored in the drive's 128KB corrected memory.

Opposed to the Audio IC AICA, it supplies the digital audio playback signal and the 33.8688MHz clock that is the audio clock source. Additionally there is a 33.8688MHz x'tal built into the drive.

6.1 Specification outline

The specification outline is below.

(Functions)

- adapted to GD-ROM (Giga Byte Disc: Sega original)
- Replay of CD-DA and GD-DA, stop ,pause ,both directions jump ,both directions scan replay
- Open and close door
- Compatible with various CD formats…CD-DA, CD-ROM XA, Photo CD, Video CD, CD Extra

(Performance)

- Digital Audio output 48Fs (Fs=44.1 kHz)
- Read method CAV
- Correction memory space 128KB (buffering, DA shock proof and shared)
- data transfer speed

Single density area approx. 600KB/s (4x speed)
Double density area approx. 900 (6x speed)～1800 KB/s (12x speed)
From the buffer approx. 11.1 MB/s (PIO Mode3)
Approx. 13.3 MB/s (Multi word DMA Mode2)

- 1/3 stroke average access time
  Less than 350ms (when first shipped)
- Full stroke average access time
  Less than 600ms (when first shipped)
- Error rate

CD-ROM Mode1	less than 1×10^{-12}
CD-ROM Mode2 form1	less than 1×10^{-12}
CD-ROM Mode2 form2	less than 1×10^{-9}
CD-DA	less than 1×10^{-9}
GD-ROM Mode1	less than 1×10^{-12}
GD-DA	less than 1×10^{-9}

- Disc data space

General CD	approx. 656MB(CD-ROM Mode1)
GD	approx. 1020MB(GD-ROM Mode1)

(Power)

- 3.3V ± 5%
- 5.0V ± 5%
- 12.0V ± 10%

(Possible operational temperature)
0℃ ~ 55℃ 20% ~ 85%RH

6.2 Interface

With regards to the Dreamcast console and the GD-ROM drive interface protocol, please refer to the separate document 'GD-ROM protocol SPI specification design'.

6.3 Digital audio

Audio signals from the GD-ROM (BCK, LRCK, SDATA) are clock synchronised 48Fs(Fs=44.1KHz) and input into the AICA external audio input pin then digitally mixed with audio generated from AICA internally before it becomes output.

-- End of GD-ROM --

7 Other

Options, peripheral devices and settings that have not been explained yet, are described below.

7.1 Control Pad

The Dreamcast system control pad is accessed through the HOLLY Maple i/f and supports up to 4 pads. Additionally this port is adapted for the use of the light gun as well as the backup media described later.

With regard to the Maple interface, please refer to separate documentation or the section (draw image processor: HOLLY), Appendix and the description of the Maple interface.

7.2 Backup media

This is used to backup (save etc) game data and is connected to the control pad sharing the HUB connected to the HOLLY Maple i/f. The Dreamcast console can directly support up to 4 media. With regard to details of the backup media please refer to other documents.

7.3 Modem

The communication speed is 33.6Kbps and the card has a LINE terminal. The compression of data, correcting of errors etc. is performed by SH4. With respect to details on the modem, please refer to separate documents.

7.4 Video output/ image mode settings method

As stated in the section (draw image processor: HOLLY), the Dreamcast system can use various video modes to display graphics. Since the Dreamcast console is compatible with various types of monitors, there are many types of connectors that are supported. Below are the various supported connectors and the signals from the connector.

- RCA connector : Audio signal(L,R), composite video signal
- S image connector : S image signal(imageY+S signal , Chroma signal)
- Expansion VGA connector : Audio signal(L,R),analogue RGB, composite,sync (H,V),mode signal, power
- (5V,12V)

(* Expansion connector is an optional connector for RF converter, RGB cable, and VGA cable)

The selection of the image display mode is through the insertion and removal of the monitor's expansion VGA connector and that information is reflected in the SH4 PIO interface (PIO [1:0]). Setting occurs from SH4 to HOLLY or each image mode register of AICA. RGB signal and/or the image mode signal output is from each individual chip.
Table 7-1 shows the relationship between SH4: PIO and the image mode. Figure 7-1 shows the image mode setting method.

PIO1	PIO0	MODE
1	1	TV(NTSC/PAL)
1	0	VBS/Y+S/C
0	1	RGB
0	0	VGA

Table 7-1 SH4:PIO image mode settings

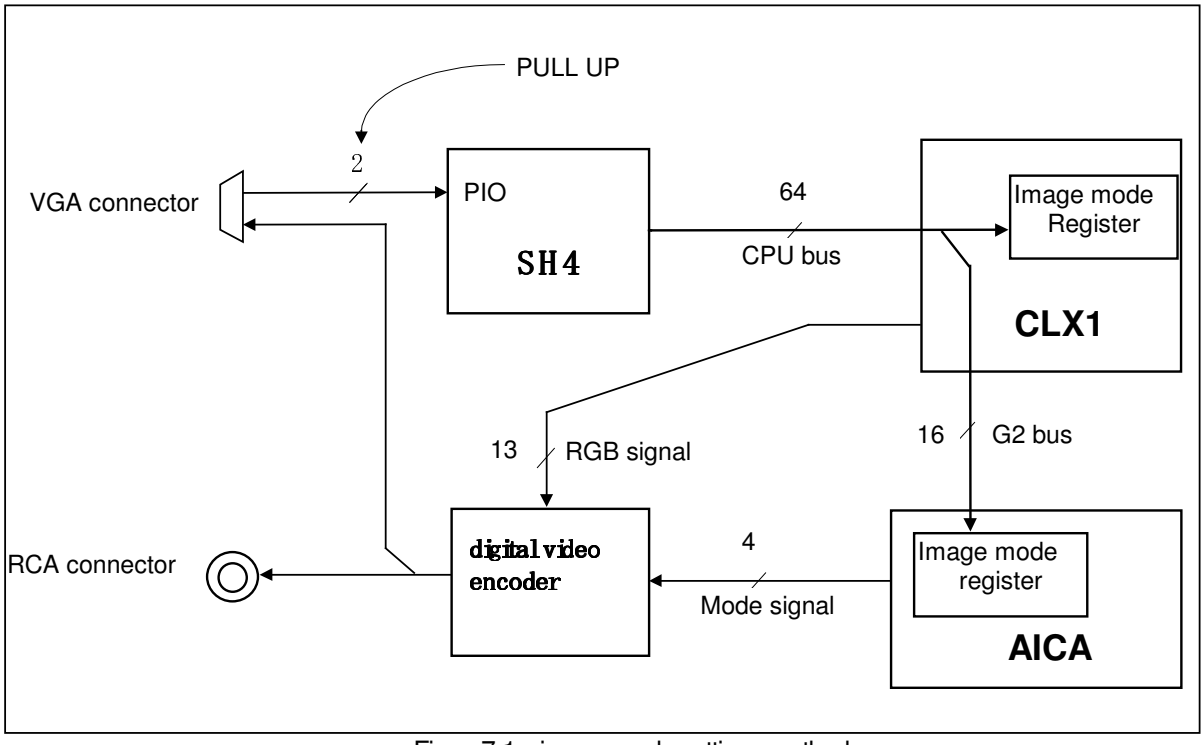


Figure7-1 image mode settings method

From HOLLY, the 24bit RGB image information (each RGB 8bit) is sent in units of 12 bit to the Digital-Video-Encoder (video DAC/encoder). The original 24 bit image data is divided into 12bit(RGB [11:0]) of MSB (RGB [11:0] = R [7:0], G [7:4]) and 12 bit of LSB (RGB [11:0] = G [3:0], B [7:0]). Then it is sent to the 54 Hz clock (which is double the 27Hz VGA pixel-clock) in a synchronised manner where it alternates between MSB and LSB. For details refer to a separate specification design document.

PLL

This is a main clock source device that does not include the system RTC and sound. Its 1 x'tal allows it to supply each clock. The clock supplies SH4 and HOLLY.

Each output from this PLL is unified regardless whether or not the video spec of the image mode is NTSC/PAL etc. Below is the list (units are <MHz>)

x'tal	To SH4	To HOLLY/pixel
13.5	33.33333	54.0

Table 7-2 output clock list

7.5 Power Supply

The console has a built-in unit which has a domestic power supply of 100 ~120V AC which is directly inputted. Each of the 3.3 / 5.0 / 12.0V DC power supplies supply the main /GD-ROM power supply which includes the CPU, graphic chip, memory IC, peripheral IC etc. The 1.8V DC or 2.4V DC internal power supply from SH4/HOLLYis supplied from a separate power supply IC rather than 3.3V DC.

7.6 Reset Sequence

The reset sequence of Dreamcast is described below.

-- End of other--

Appendix . Maple i/f

Supplementary explanation of the Maple i/f is below. With respect to the details of the Maple i/f specifications, please refer to separate material.

Maple i/f is an original Sega peripheral interface and is a serial interface that supports the connection of the control pad and backup media (B/U) etc. The Dreamcast console supports a maximum of 4 ports and devices can be connected to a maximum of 4 ports. With regards to the backup media, they are connected to the control pad that shares the HUB connected to the console's Maple port.

	(Port 0)	(Port 1)	(Port 2)	(Port 3)
Signal line	SDCKA0	SDCKA1	SDCKA2	SDCKA3
Signal line	SDCKB0	SDCKB1	SDCKB2	SDCKB3
power cable common to each port	VCC	VCC	VCC	VCC
power cable common to each port	GND	GND	GND	GND

Table C-1 Signal lines used by Maple i/f

Table C-1 is a list of signal lines used by the Maple i/f. The data transmission uses the synchronised serial method and talking in terms of 1 port, there are a total of 4 lines- the power cable (VCC, GND), SDCKA (both directions) data cable and SDCKB (both directions). The sending of data in both directions is 半2重 and the data transfer rate is a maximum of 2Mbps or a minimum of 250Kbps. Data transmission occurs in the units of frames (smallest unit) and the content of the frame starts from the START pattern which signifies the start of data transmission. A 1024 byte long (DATA) pattern, (parity) and (END) pattern configure it. (Parity) is horizontal and 8bit and is automatically added by the hardware when sending and deleted upon receiving. The configuration of the controller consists of a 32 bit system register(SYSREG), sent data table Address Register(AREG), Status register(SREG), Assigned Parameter Clear Register(IREG), received data store address boundary setting Register(BREG) and a 32bit×8 word sent FIFO (TxD FIFO) from the received FIFO(RxD FIFO).

The basic operations are described below.
The peripheral controllers are synchronised to the V_BLANK signal (can be set to be postponed by the system register) and the sent data on the main memory which is described by the sent data table address register and is loaded to the sent FIFO (master operation)
Sent data is configured by the command+sent data store address+sent out data. Commands are to the peripheral controller, and set the length of command completion output port and sent out data. If there is no indication that the command is complete then as soon as the sent FIFO becomes empty, sent data in the main memory is loaded in 32 byte units by the sent FIFO. The sent data store address has a lead address for storing sent data. Sent data is data that is administered by the Maple protocol and is transferred to the peripheral devices in units of 4 bytes. Sent data from the peripheral device are in 4 byte units and is transferred to the main memory as soon as the sent FIFO becomes full. However, even if FIFO isn't full, as soon as sending is complete it forces 32-byte transfer. (valid data+invalid data)
If the peripheral device is not connected and time out, frame error etc. occurs, the 32bit value of 0xffffffff is written into the sent data store address that is appropriate for the command. (The lead data for the sent data store address is guaranteed except when the data is 0xffffffff because of the software protocol)
Once the string of operations has finished, the peripheral controller will stop operating and reflect the situation in the status register.

----------End----------