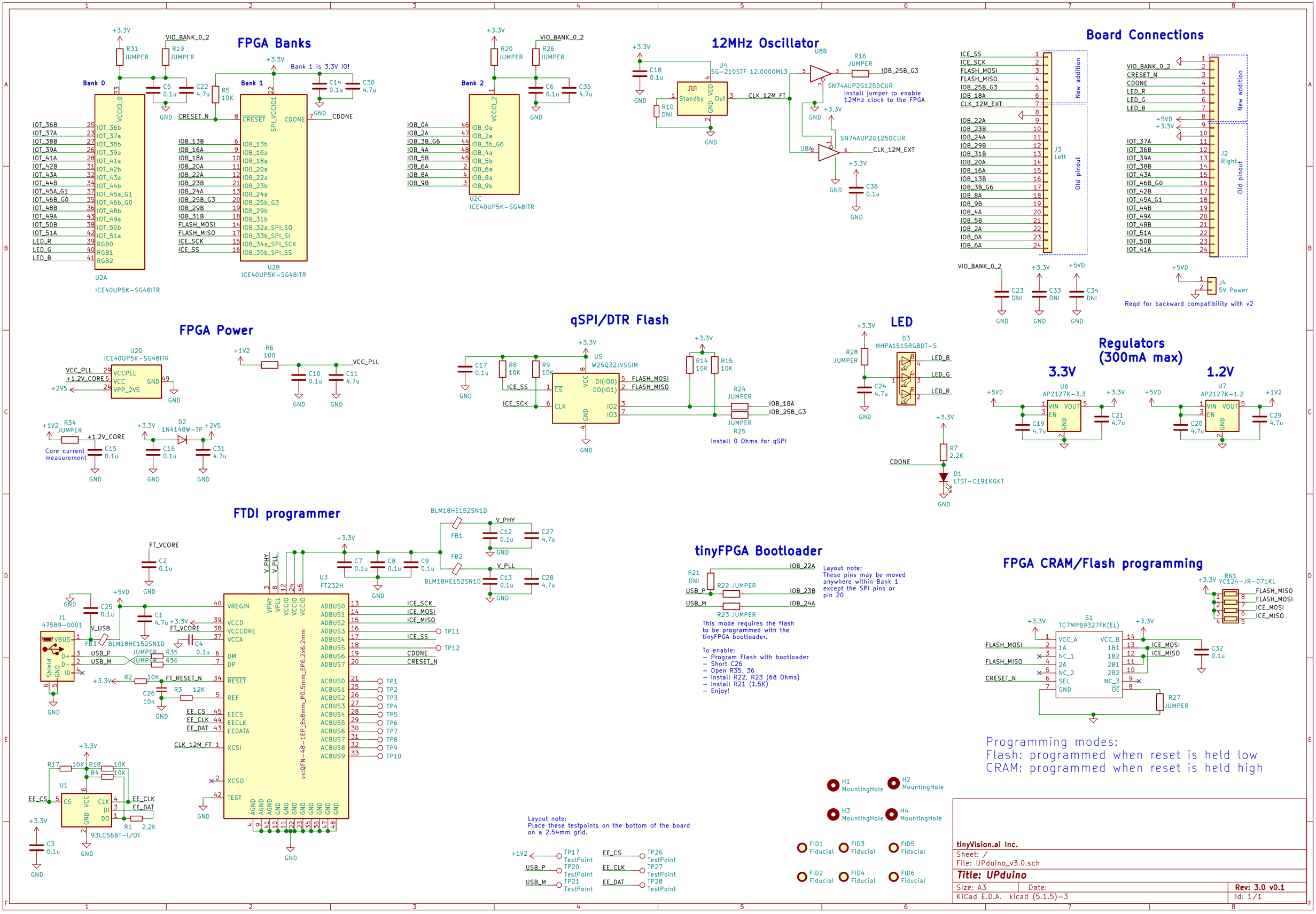
FPGA Banks
Bank 0
Bank 1
Bank 2
Bank 1 is 3.3V IO!
U2A
ICE40UP5K-SG48ITR
U2B
ICE40UP5K-SG48ITR
U2C
ICE40UP5K-SG48ITR
12MHz Oscillator
U4
SG-210STF 12.0000ML3
Standby
SN74AUP2G125DCUR
Install jumper to enable 12MHz clock to the FPGA
Board Connections
New addition
Old pinout
J3 Left
J2 Right
J4 5V Power
Reqd for backward compatibility with v2
FPGA Power
U2D
ICE40UP5K-SG48ITR
Core current measurement
qSPI/DTR Flash
U5
W25Q32JVSSIM
Install 0 Ohms for qSPI
LED
D3
MHPA1515RGBDT-S
D1
LTST-C191KGKT
Regulators (300mA max)
3.3V
U6
AP2127K-3.3
1.2V
U7
AP2127K-1.2
FTDI programmer
U3
FT232H
J1
47589-0001
U1
93LC56BT-I/OT
tinyFPGA Bootloader
Layout note:
These pins may be moved anywhere within Bank 1 except the SPI pins or pin 20
This mode requires the flash to be programmed with the tinyFPGA bootloader.
To enable:
– Program Flash with bootloader
– Short C26
– Open R35, 36
– Install R22, R23 (68 Ohms)
– Install R21 (1.5K)
– Enjoy!
FPGA CRAM/Flash programming
RN1
YC124-JR-071KL
S1
TC7MPB9327FK(EL)
Programming modes:
Flash: programmed when reset is held low
CRAM: programmed when reset is held high
Layout note:
Place these testpoints on the bottom of the board on a 2.54mm grid.
H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
FID1 Fiducial
FID2 Fiducial
FID3 Fiducial
FID4 Fiducial
FID5 Fiducial
FID6 Fiducial
tinyVision.ai Inc.
Sheet: /
File: UPduino_v3.0.sch
Title: UPduino
Size: A3
Date:
Rev: 3.0 v0.1
KiCad E.D.A. kicad (5.1.5)-3
Id: 1/1