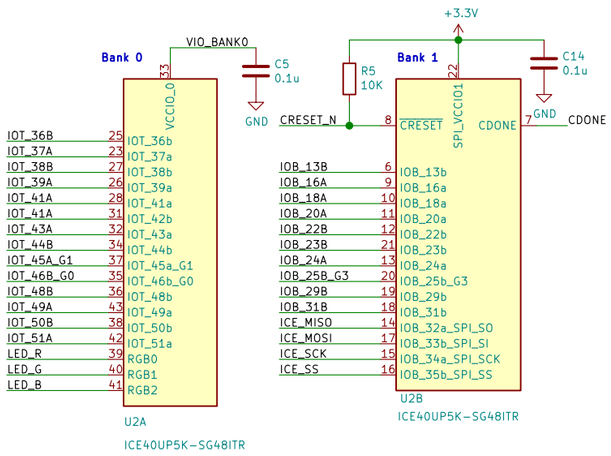
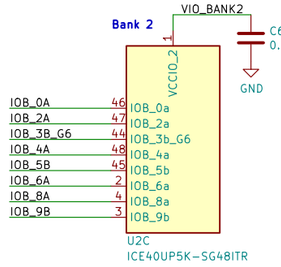
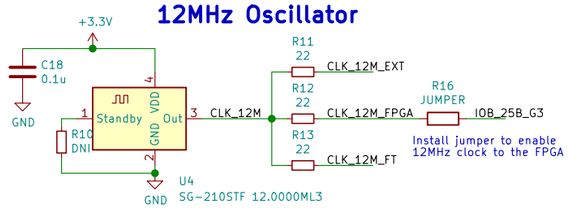
FPGA Banks

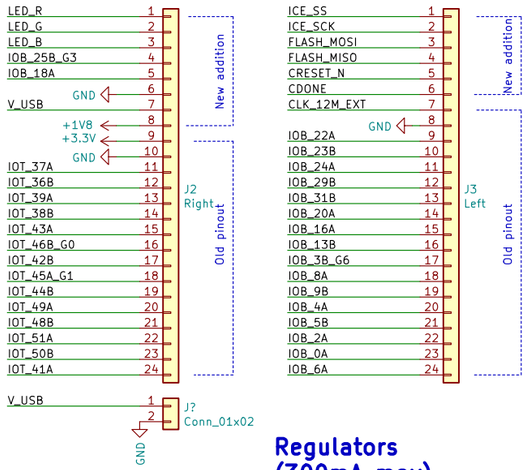




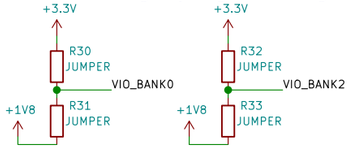
12MHz Oscillator



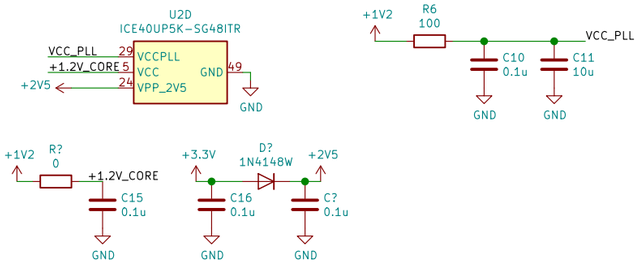
Board connections



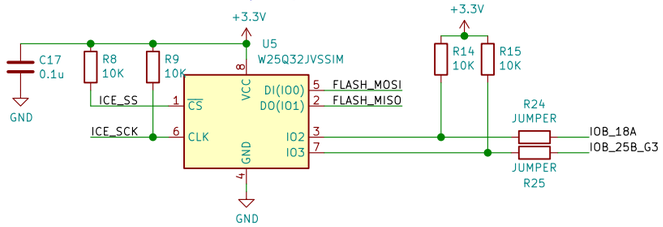
Bank voltage programming



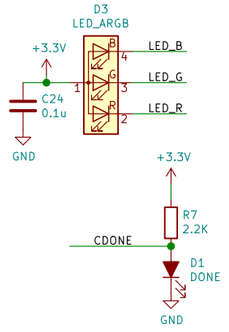
FPGA Power



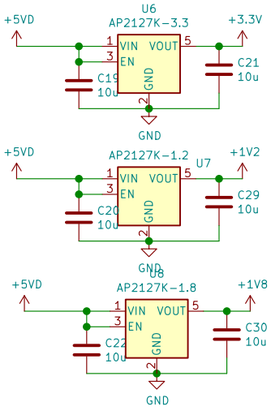
qSPI/DTR Flash



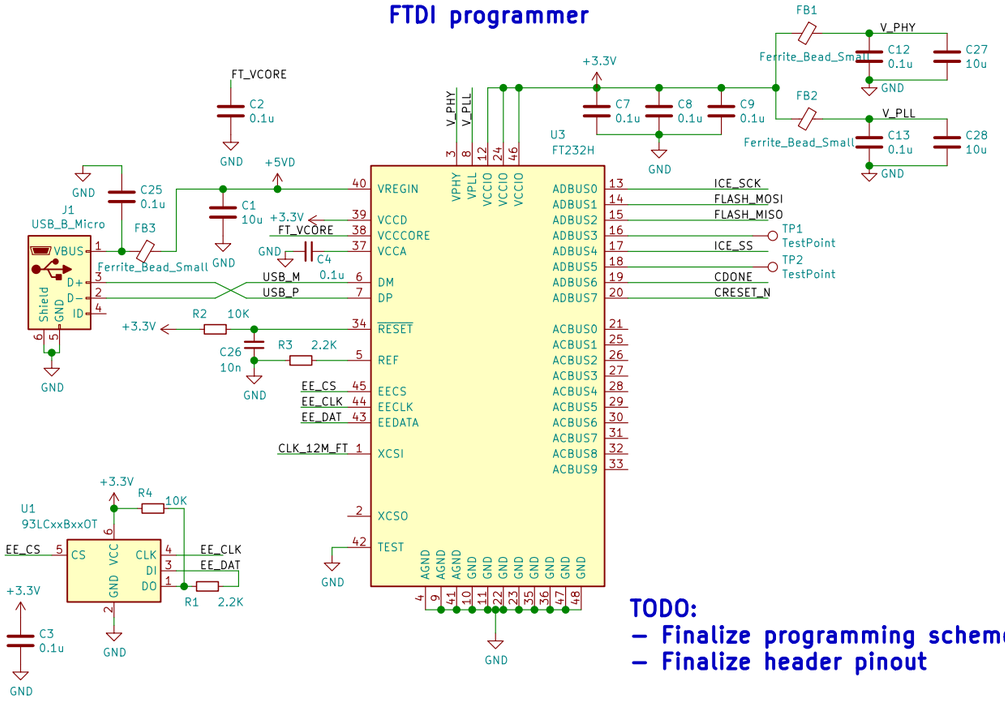
LED



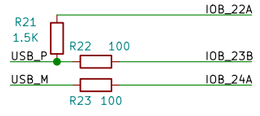
Regulators (300mA max)



FTDI programmer



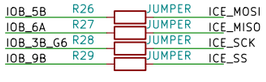
tinyFPGA Bootloader



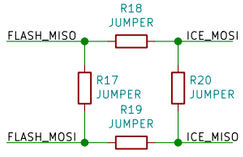
Keep the FTDI in reset to use the tinyFPGA bootloader. This requires the flash to be programmed with the bootloader!

Following jumpers allow the FPGA to talk to the FTDI after configuration using SPI/I2C/UART while not interfering with the memory bus.
This is very useful when you want to use the flash for say a RISCV processor in the FPGA and also the UART to talk to the processor. This would otherwise require an external translator...

NOTE: should be used in conjunction with the tinyFPGA bootloader to prevent bus conflicts.

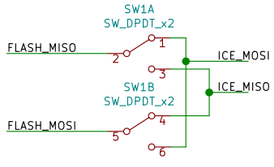


FPGA/Flash programming



This requires manual configuration, not a pleasant task!
Ideally, this would be auto-selected.

Alternate CRAM/Flash selection scheme



Switches are bidirectional

Switches are selected using the reset signal as follows:
Flash: Programming is done when reset is held low
CRAM: Programming is done when reset is held high

TODO:
- Finalize programming scheme
- Finalize header pinout

H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole

FID1 Fiducial
FID2 Fiducial
FID3 Fiducial
FID4 Fiducial
FID5 Fiducial
FID6 Fiducial

tinyVision.ai Inc.		
Sheet: /		
File: UPduino.sch		
Title: UPduino extended version		
Size: A3	Date:	**Rev: 3.0 v0.1**
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