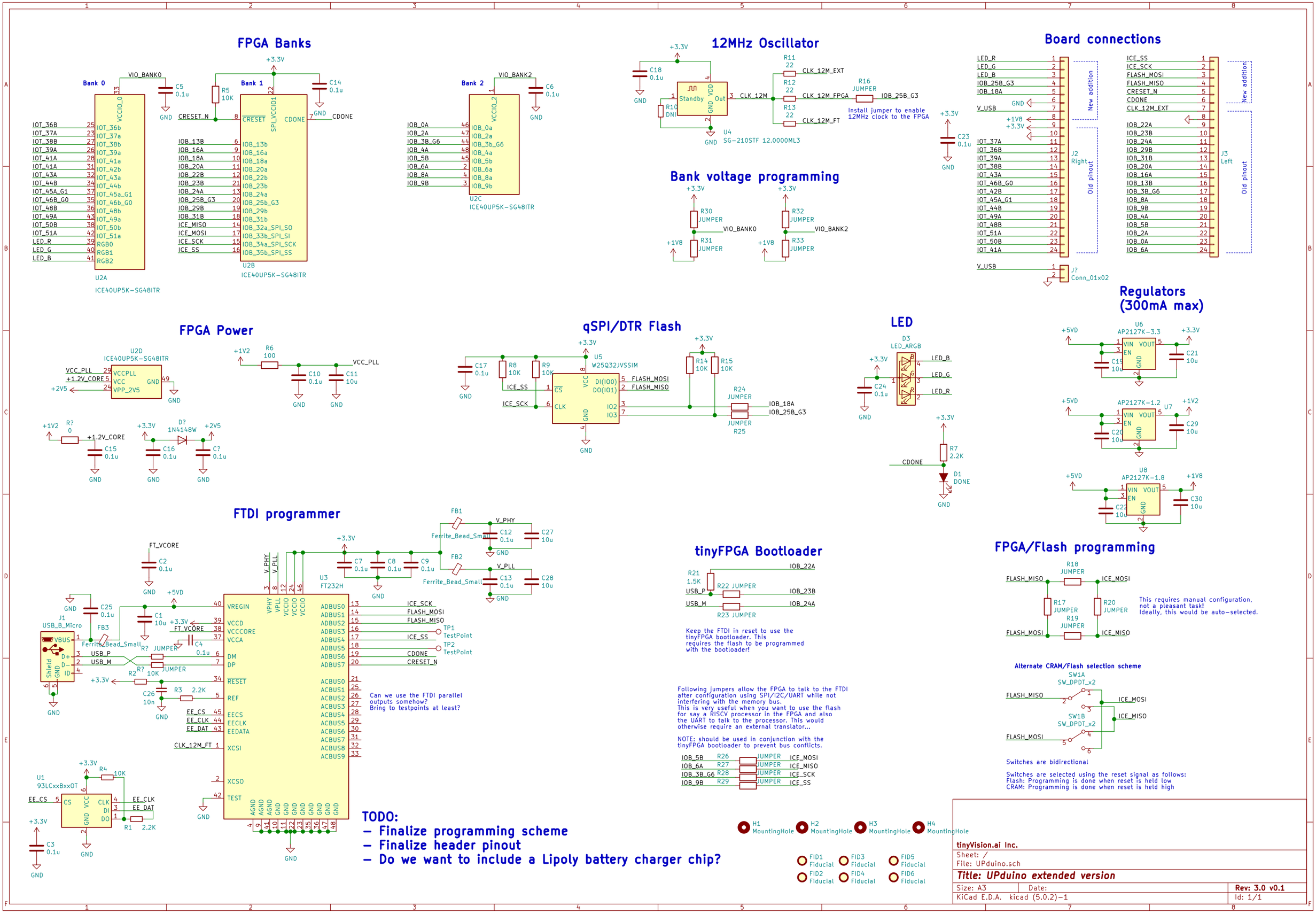
FPGA Banks
Bank 0
Bank 1
Bank 2
U2A
ICE40UP5K-SG48ITR
U2B
ICE40UP5K-SG48ITR
U2C
ICE40UP5K-SG48ITR
12MHz Oscillator
U4
SG-210STF 12.0000ML3
Install jumper to enable 12MHz clock to the FPGA
Bank voltage programming
Board connections
New addition
Old pinout
J2 Right
J3 Left
J? Conn_01x02
FPGA Power
U2D
ICE40UP5K-SG48ITR
qSPI/DTR Flash
U5
W25Q32JVSSIM
LED
D3
LED_ARGB
Regulators (300mA max)
U6
AP2127K-3.3
U7
AP2127K-1.2
U8
AP2127K-1.8
FTDI programmer
U3
FT232H
J1
USB_B_Micro
Can we use the FTDI parallel outputs somehow? Bring to testpoints at least?
U1
93LCxxBxxOT
tinyFPGA Bootloader
Keep the FTDI in reset to use the tinyFPGA bootloader. This requires the flash to be programmed with the bootloader!
Following jumpers allow the FPGA to talk to the FTDI after configuration using SPI/I2C/UART while not interfering with the memory bus.
This is very useful when you want to use the flash for say a RISCV processor in the FPGA and also the UART to talk to the processor. This would otherwise require an external translator...
NOTE: should be used in conjunction with the tinyFPGA bootloader to prevent bus conflicts.
FPGA/Flash programming
This requires manual configuration, not a pleasant task! Ideally, this would be auto-selected.
Alternate CRAM/Flash selection scheme
SW1A SW_DPDT_x2
SW1B SW_DPDT_x2
Switches are bidirectional
Switches are selected using the reset signal as follows:
Flash: Programming is done when reset is held low
CRAM: Programming is done when reset is held high
TODO:
– Finalize programming scheme
– Finalize header pinout
– Do we want to include a Lipoly battery charger chip?
tinyVision.ai Inc.
Sheet: /
File: UPduino.sch
Title: UPduino extended version
Size: A3
Date:
Rev: 3.0 v0.1
KiCad E.D.A. kicad (5.0.2)-1
Id: 1/1