8 General-purpose timers

8.1 Timer overview

The SPC1168 includes three 32-bit General Purpose Timers (GPT) with following features:

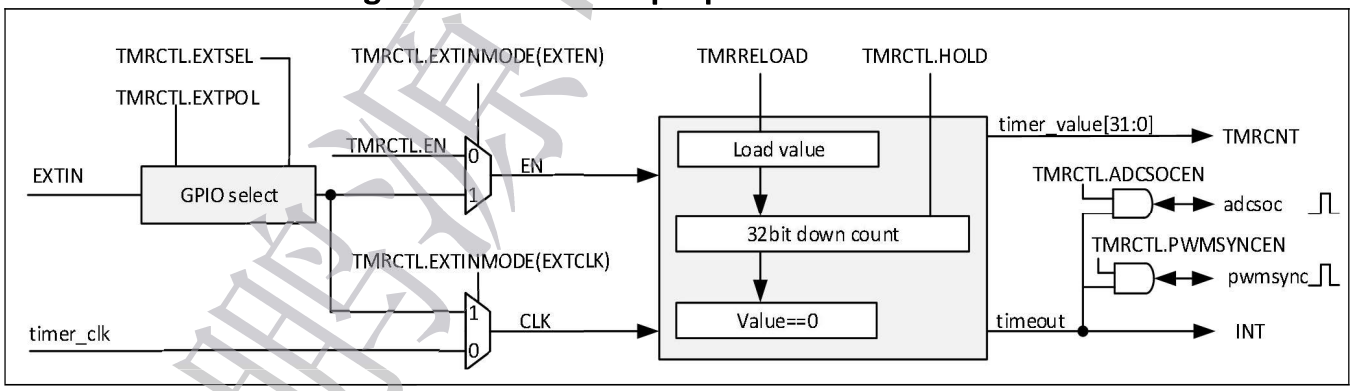
- Take clock from APB clock and timer clock
- 32-bit down-counter
- Generate interrupt upon counter reaches zero
- Generate ADCSOC event upon counter reaches zero
- Generate PWMSYNC event upon counter reaches zero
- Capture external input as timer enable
- Capture external input as timer clock

8.2 Functional description

Each GPT operates under periodic timer mode. As shown in Figure 8-1, when the timer is enabled, the counter loads the value from TMRRELOAD register and starts to count down until it reaches 0. Then the counter restarts from the reload value and decrease again. Upon the counter equals 0:

- An interrupt will be generated if it is enabled. The interrupt flag held until it is manually cleared
- An ADCSOC event will be generated if TMRCTL.ADCSOCEN is enabled
- A PWMSYNC event will be generated if TMRCTL.PWMSYNCEN is enabled

Figure 8-1: General-purpose timer structure



The low to high transition on external input (EXTIN) can be used as timer enable. It can also be used as external clock. The register TMRCTL.EXTSEL is used to select GPIO pin as the external input (EXTIN). Please see Table 8-3 and Table 8-4 for the details.

The timers are disabled by default after system reset.

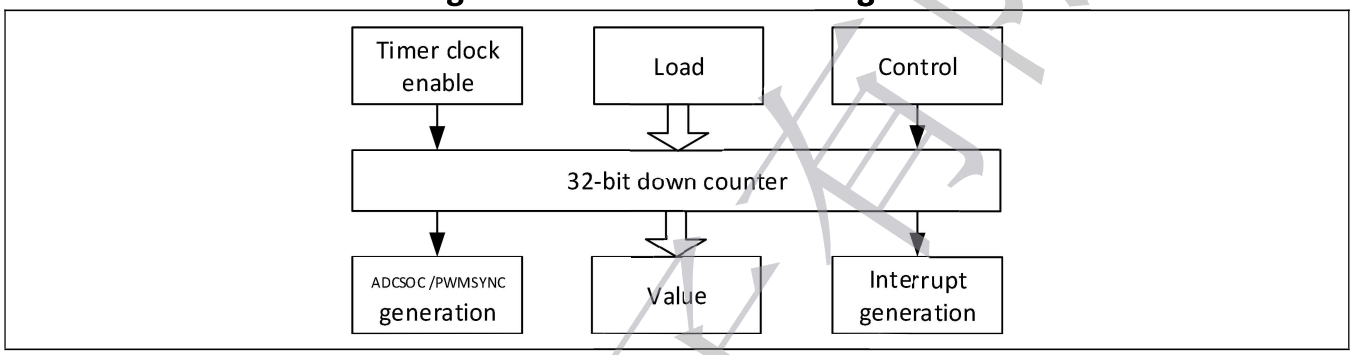
8.3 Initialization sequence

The following sequence of operations should be followed to start the timer.

- Disable the timer and clear timer interrupt
- Configure the timer reload value register (TMRRELOAD)
- Configure the timer control register (TMRCTL)
- Enable the timer to start the timer counter

A block diagram of the timer run mode is shown in Figure 8-2.

Figure 8- 2: GPT run flow diagram



8.4 Registers

8.4.1 TIMER register map

Table 8- 1: Timer Module Base Address

Peripheral Module	Base Address
TIMER0	0x4000 7000
TIMER1	0x4000 7020
TIMER2	0x4000 7040

Table 8- 2: Timer Register Map

Register	Offset	Description	Reset Value
TMRCTL	0x00	Timer Control Register	0x00000000
TMRCNT	0x04	Timer Counter Value Register	0x00000000
TMRRELOAD	0x08	Timer Reload Value Register	0x00000000
TMRIF	0x0C	Timer Interrupt Flag Register	0x00000000
TMRRAWIF	0x10	Timer Raw Interrupt Flag Register	0x00000000
TMRIE	0x14	Timer Interrupt Enable Register	0x00000000
TMRIFRC	0x18	Timer Interrupt Force Register	0x00000000
TMRIC	0x1C	Timer Interrupt Clear Register	0x00000000

8.4.2 TIMER registers

Table 8-3 through Table 8-18 provide the timer module related register details.

Table 8- 3: Timer Control Register (TMRCTL) Layout

TMRCTL (Timer Control Register) Offset: 0x0 Default: 0x00000000
Access: TIMER -> TMRCTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			EXTSEL				
7	6	5	4	3	2	1	0
EXTSEL	EXTPOL	EXTINMODE		PWMSYNCEN	ADCSOCEN	HOLD	EN

Table 8- 4: Timer Control Register (TMRCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12:7	EXTSEL	RW	0x0	External input source select (GPIO number)
6	EXTPOL	RW	0x0	External input polarity 0: Active low 1: Active high
5:4	EXTINMODE	RW	0x0	External input mode 00: Disable external input 01: Invalid 10: Take external input as timer clock 11: Take external input as timer enable
3	PWMSYNCEN	RW	0x0	PWMSYNC generation enable 0: Do not generate PWMSYNC 1: Generate PWMSYNC whenever TMRCNT counts down to 0
2	ADCSOCEN	RW	0x0	ADCSOC generation enable 0: Do not generate ADCSOC 1: Generate ADCSOC whenever TMRCNT counts down to 0
1	HOLD	RW	0x0	Hold counter value upon falling edge of TMRCTL.EN 0: Reset counter to 0 upon falling edge of TMRCTL.EN 1: Hold counter value upon falling edge of TMRCTL.EN
0	EN	RW	0x0	Timer enable 0: Disable Timer 1: Enable Timer

Table 8- 5: Timer Counter Value Register (TMRCNT) Layout

TMRCNT (Timer Counter Value Register) Offset: 0x4 Default: 0x00000000 Access: TIMER -> TMRCNT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 8- 6: Timer Counter Value Register (TMRCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Current value of timer counter.

Table 8- 7: Timer Reload Value Register (TMRRELOAD) Layout

TMRRELOAD (Timer Reload Value Register) Offset: 0x8 Default: 0x00000000 Access: TIMER -> TMRRELOAD.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 8- 8: Timer Reload Value Register (TMRRELOAD) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reload value. A Write to this register also sets the current TMRCNT value.

Table 8- 9: Timer Interrupt Flag Register (TMRIF) Layout

TMRIF (Timer Interrupt Flag Register) Offset: 0xC Default: 0x00000000 Access: TIMER -> TMRIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8- 10: Timer Interrupt Flag Register (TMRIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RO	0x0	Timer interrupt 0: Interrupt not occurred 1: Interrupt occurred and issued to CPU. No further interrupt will be issued until the flag is cleared

Table 8- 11: Timer Raw Interrupt Flag Register (TMRRAWIF) Layout

TMRRAWIF (Timer Raw Interrupt Flag Register) Offset: 0x10 Default: 0x00000000 Access: TIMER -> TMRRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8- 12: Timer Raw Interrupt Flag Register (TMRRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RO	0x0	Timer raw interrupt status. This bit is set whenever TMRCNT counts down to 0 and cleared only by writing a 1 to TMRIC 0: Interrupt not occurred 1: Interrupt occurred

Table 8- 13: Timer Interrupt Enable Register (TMRIE) Layout

TMRIE (Timer Interrupt Enable Register) Offset: 0x14 Default: 0x00000000 Access: TIMER -> TMRIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8- 14: Timer Interrupt Enable Register (TMRIE) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RW	0x0	Timer interrupt enable. This bit does not affect TMRRAWIF and PWMSYNC/ADCSOC generation 0: Do not issue interrupt to CPU 1: Issue interrupt whenever TMRRAWIF=1

Table 8- 15: Timer Interrupt Force Register (TMRIFRC) Layout

TMRIFRC (Timer Interrupt Force Register) Offset: 0x18 Default: 0x00000000 Access: TIMER -> TMRIFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8- 16: Timer Interrupt Force Register (TMRIFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	W1S	0x0	Timer interrupt software force 0: Write a 0 has no effect and always read back 0 1: Write a 1 forces the TMRRAWIF flag. This bit is self-cleared to 0.

Table 8- 17: Timer Interrupt Clear Register (TMRIC) Layout

TMRIC (Timer Interrupt Clear Register) Offset: 0x1C Default: 0x00000000 Access: TIMER -> TMRIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8- 18: Timer Interrupt Clear Register (TMRIC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	W1C	0x0	Timer interrupt clear 0: Write a 0 has no effect and always read back 0. 1: Write a 1 clears the TMRRAWIF and TMRIF flag. This bit is self-cleared to 0.