Computer Systems and Architecture Final Project

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The system performance of computers has vastly improved over the last 25 years and will continue to into the future. This paper describes how concepts such as RISC, pipelining, cache memory, and virtual memory have evolved to increase computer performance. Additionally, it will describe current technologies and trends in these areas.

RISC

The term "Reduced Instruction Set Computer (RISC)" was coined by David Patterson at the University of California at Berkeley in the 1980s. Patterson was primarily influenced by the principles behind the design of the IBM 801 supercomputer and wrote the first paper describing RISC. In short, Patterson advocated for a highly-optimized instruction set, shortened execution time, and one cycle per instruction.

RISC was conceptualized when researchers analyzed trace tapes with millions of recorded instructions. During the analysis, it was revealed that only a fraction of the microprogrammed instruction set was regularly utilized, while a majority of the instructions remained unused (Oklobdzija, 1999). This revelation drove a shift towards creating and using reduced instruction sets. At the time, RISC was an evolution and improvement upon CISC architecture. RISC became popular and gained momentum during the mid-1980s through the 1990s (Patterson, 2017).

Pipelining

RISC is ideal for a process known as "pipelining." Pipelining allows for a second instruction to be issued before the first instruction completes, allowing for increased performance and speed. The RISC pipeline consists of five steps: (1) instruction fetch, (2) instruction decode (read), (3) execute, (4) memory access, and (5) writeback. While these instructions may execute

concurrently, the two must be at different pipeline stages within the same clock cycle. Unlike RISC, pipelining in CISC processors is far more difficult due to: (1) variable length, (2) multiple operands, (3) complex addressing modes, and (4) complex instructions.

Several notable improvements to the pipelining concept have been made, such as Superscalar, Super-pipelining, and Very Long Instruction Word (VLIW). Below is a brief description of each technique:

- *Superscalar*: a technique that allows for more than one instruction to be issued per clock cycle by using instruction-level parallelism.
- *Super-pipelining*: a technique that breaks the pipeline stages into even smaller steps, performing multiple pipeline stages within one clock cycle.
- *VLIW:* a technique that issues multiple operations per instruction dictated and scheduled by the compiler.

Each of the mentioned processes was an evolution to the pipelining concept and has contributed to significant performance boosts that are present on modern-day machines. These techniques are even commonplace to be interwoven, producing an even more significant improvement.

Cache Memory

Cache Memory is a crucial part of modern computing. It is an expensive and fast type of Static RAM located between the microprocessor and the Computer's RAM. Its purpose is to store frequently accessed data used by the CPU. These caches are located in close proximity to or on the CPUs themselves. Historically, it was common for Cache Memory to only be used on supercomputers; however, the rise of home computing in the 1990s changed this (Carvalho, 2002).

Cache Memory became very relevant in the 1990s as main memory speeds began to lag behind processors. This disparity created bottlenecking, which is the result of a fast CPU/slow memory combination. In bottlenecking, the CPU waits on the RAM to deliver data and instructions, which is ultimately detrimental to performance. Cache Memory resolves this issue and accelerates the fetching of frequently used data. Modern Cache Memory is split into three layers; the following provides a brief description of each:

Level	Capacity/Speed	Priority
L1	Smallest capacity and fastest	First place the CPU will check for data
L2	Medium capacity and fast	Second place the CPU will check for data
L3	Largest capacity and slowest	Third place the CPU will check for data

Although Cache Memory does bridge the gap between DRAM and CPUs, it is predicted that there will be a point when existing DRAM speeds mask advances in CPU speeds, also referred to as the “memory wall” (Barua, 2021).

Virtual Memory

Virtual memory is a memory management technique that uses the computer hard disk to store unused data from the main memory to free up and optimize the use of RAM. This is ideal for systems with limited RAM and gives the “appearance” of a large main memory (Utilize Windows , 2010). A combination of hardware/software does the swapping of the data to and from the hard disk. This process is known as paging/swapping, and the storage space on the hard disk is referred to as a page file or a swap file.

In the days of limited RAM, Virtual Memory was critical. However, virtual memory can be avoided by upgrading the computer’s RAM, which is relatively cheap and performs better than the RAM of 25 years ago.

Current Trends and Technologies

During the 2000s, CISC-based processors dominated the computing market, the most prominent example being the Intel x86 instruction set. It had the advantage of mimicking RISC-like features with hardware and presented a superior circuit design over RISC processors (Patterson, 2017). In the PC market of the 2000s, processors like Intel Pentium became household names and synonymous with desktops and servers.

It took many decades for RISC to be re-adopted. The delay was mainly for two reasons: (1) RISC instructions were challenging to write for assembly programmers, and (2) they required more memory (RAM). However, RAM became faster and cheaper with technological advancements, opening the door to RISC architecture. Additionally, improvements to compilers made RISC instructions easier to write.

Perhaps the most significant contributor to the resurgence of RISC was the shift from the PC era to the Mobile Device era. Today, billions of RISC chips are manufactured and shipped every year. Nearly every Apple and Android device uses a RISC processor (Patterson, 2017).

RISC processors are utilized in mobile devices for several reasons: (1) they are easy to design, (2) cheaper to produce, (3) require fewer transistors, (4) are more power-efficient, and (4) have better heat dissipation. These factors combine to make RISC the ideal ISA for mobile devices.

The most notable family of modern RISC processors is the ARM (Advanced RISC Machine) architecture. ARM processors are predominantly used in mobile devices and are not compatible with Windows unless x86-to-ARM emulation is utilized (Pulapaka, 2021). However, a recent disruption to the computing industry occurred when Apple revealed their M1 MacBook and Tablets, implementing an ARM architecture (Apple Inc., 2021). This event symbolizes

another significant shift towards RISC-based processors. Apple's choice to walk away from a 14-year partnership with Intel and implement an ARM architecture was primarily due to their desire for increased power efficiency/performance and the freedom to create their own custom chips (Tracy, 2021).

Arguably the most important event in the world of ISAs was the announcement of the RISC-V architecture. RISC-V is an instruction set architecture (ISA) developed and promoted as a free and open-source project. The project seeks to learn from past design failures and create a brand new architecture from scratch to combat the proprietary nature of ISAs and provide a modern, modular architecture for developers to use. The creators of RISC-V developed it with the following considerations in mind: (1) Free and Open, (2) 64-bit Addresses, (3) Compressed Instructions, (4) Separate Privileged ISA, (4) Position Code, (5) IEEE 754-2008 and (6) Classically Virtualizable.

The release of RISC-V is the most significant evolution for ISAs since the creation of the original RISC architecture. The transition from proprietary ISAs to open-sourced provides enormous potential for the future of computing as we know it. The world of computer architecture is now accessible to anyone with the will to tackle it.

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