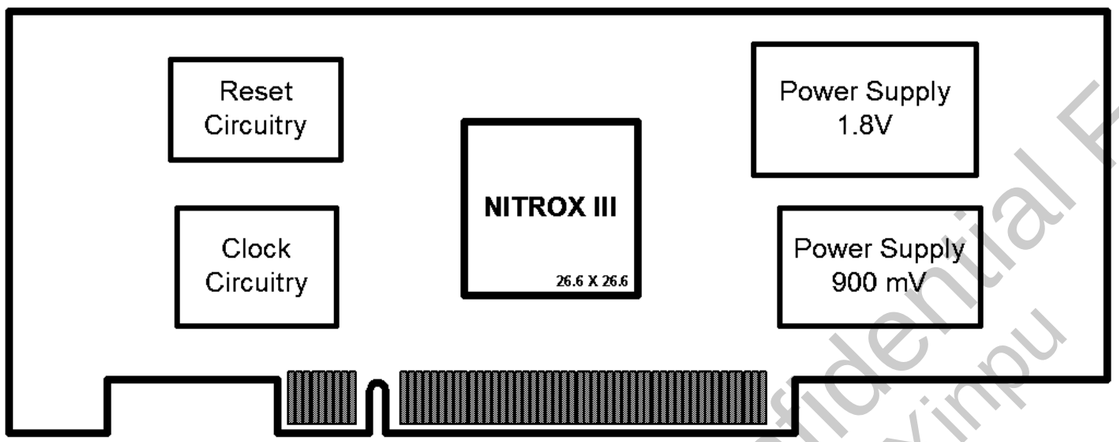

Assembly Note:

- DNI = Do Not Install

History of Changes

R1.0: Initial release

R1.1: Added FETs and LEDs D3, D4, D5

R1.2: Core clock frequency setting greater than 001 are reserved; thus not to be used.

R1.3: Changed C200 to 6pF for delayed output of U15 to about 500ms.
Corrected the delay comment.

R1.4: Placed the following NITROX III balls to GND: A20 and A24

R1.5: corrected the signal return path for PLL_E_VSS_18V,PLL_S_VSS_18V,PLL_Z_VSS_18V

R1.6: Changed the following resistors to 1K Ohm. R37, R38, R39.

R1.7: Fixed power sequencing for EXP_VDD_09.

R1.8: Fixed VCC for the EEPROM .

R1.9: Set ball CNN35XX.B23 to GND via R2

R1.10: Updated the CNN35XX symbol

R1.11: Updated the CNN35XX symbol. Removed R2. Removed R27. Updated the FREQ_SEL table

R1.12: Corrected the decoupling cap values for C206, C205, C248. Added two decoupling caps to EXP_VDD_09_FLT

CAVIUM NETWORKS	Rev A1.12	BLOCK DIAGRAM	DATE: Friday, February 24, 2012
	Project	Engineer: TM Engineering	PAGE: 1 of 9

Place components
close to the CPU

U1A

6 PEX_TX_00_P	AE9	EXP_RX_0_P	EXP_TX_0_P	AD8	C1 0402 X7R 100nF	PEX_RX_00_P 6
6 PEX_TX_00_N	AF9	EXP_RX_0_N	EXP_TX_0_N	AC8	C2 0402 X7R 100nF	PEX_RX_00_N 6
6 PEX_TX_01_P	AE11	EXP_RX_1_P	EXP_TX_1_P	AD10	C3 0402 X7R 100nF	PEX_RX_01_P 6
6 PEX_TX_01_N	AF11	EXP_RX_1_N	EXP_TX_1_N	AC10	C4 0402 X7R 100nF	PEX_RX_01_N 6
6 PEX_TX_02_P	AE13	EXP_RX_2_P	EXP_TX_2_P	AD12	C5 0402 X7R 100nF	PEX_RX_02_P 6
6 PEX_TX_02_N	AF13	EXP_RX_2_N	EXP_TX_2_N	AC12	C6 0402 X7R 100nF	PEX_RX_02_N 6
6 PEX_TX_03_P	AE15	EXP_RX_3_P	EXP_TX_3_P	AD14	C7 0402 X7R 100nF	PEX_RX_03_P 6
6 PEX_TX_03_N	AF15	EXP_RX_3_N	EXP_TX_3_N	AC14	C8 0402 X7R 100nF	PEX_RX_03_N 6
6 PEX_TX_04_P	AE17	EXP_RX_4_P	EXP_TX_4_P	AD16	C9 0402 X7R 100nF	PEX_RX_04_P 6
6 PEX_TX_04_N	AF17	EXP_RX_4_N	EXP_TX_4_N	AC16	C10 0402 X7R 100nF	PEX_RX_04_N 6
6 PEX_TX_05_P	AE19	EXP_RX_5_P	EXP_TX_5_P	AD18	C11 0402 X7R 100nF	PEX_RX_05_P 6
6 PEX_TX_05_N	AF19	EXP_RX_5_N	EXP_TX_5_N	AC18	C12 0402 X7R 100nF	PEX_RX_05_N 6
6 PEX_TX_06_P	AE21	EXP_RX_6_P	EXP_TX_6_P	AD20	C13 0402 X7R 100nF	PEX_RX_06_P 6
6 PEX_TX_06_N	AF21	EXP_RX_6_N	EXP_TX_6_N	AC20	C14 0402 X7R 100nF	PEX_RX_06_N 6
6 PEX_TX_07_P	AE23	EXP_RX_7_P	EXP_TX_7_P	AD22	C15 0402 X7R 100nF	PEX_RX_07_P 6
6 PEX_TX_07_N	AF23	EXP_RX_7_N	EXP_TX_7_N	AC22	C16 0402 X7R 100nF	PEX_RX_07_N 6
6 PEX_TX_08_P	AC25	EXP_RX_8_P	EXP_TX_8_P	AB24	C17 0402 X7R 100nF	PEX_RX_08_P 6
6 PEX_TX_08_N	AC26	EXP_RX_8_N	EXP_TX_8_N	AB23	C18 0402 X7R 100nF	PEX_RX_08_N 6
6 PEX_TX_09_P	AA25	EXP_RX_9_P	EXP_TX_9_P	Y24	C19 0402 X7R 100nF	PEX_RX_09_P 6
6 PEX_TX_09_N	AA26	EXP_RX_9_N	EXP_TX_9_N	Y23	C20 0402 X7R 100nF	PEX_RX_09_N 6
6 PEX_TX_10_P	W25	EXP_RX_10_P	EXP_TX_10_P	V24	C21 0402 X7R 100nF	PEX_RX_10_P 6
6 PEX_TX_10_N	W26	EXP_RX_10_N	EXP_TX_10_N	V23	C22 0402 X7R 100nF	PEX_RX_10_N 6
6 PEX_TX_11_P	U25	EXP_RX_11_P	EXP_TX_11_P	T24	C23 0402 X7R 100nF	PEX_RX_11_P 6
6 PEX_TX_11_N	U26	EXP_RX_11_N	EXP_TX_11_N	T23	C24 0402 X7R 100nF	PEX_RX_11_N 6
6 PEX_TX_12_P	R25	EXP_RX_12_P	EXP_TX_12_P	P24	C25 0402 X7R 100nF	PEX_RX_12_P 6
6 PEX_TX_12_N	R26	EXP_RX_12_N	EXP_TX_12_N	P23	C26 0402 X7R 100nF	PEX_RX_12_N 6
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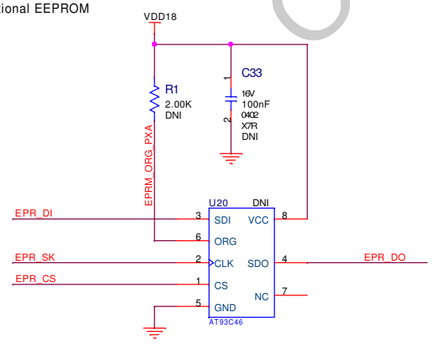
6 PEX_TX_14_N	L26	EXP_RX_14_N	EXP_TX_14_N	K23	C30 0402 X7R 100nF	PEX_RX_14_N 6
6 PEX_TX_15_P	J25	EXP_RX_15_P	EXP_TX_15_P	H24	C31 0402 X7R 100nF	PEX_RX_15_P 6
6 PEX_TX_15_N	J26	EXP_RX_15_N	EXP_TX_15_N	H23	C32 0402 X7R 100nF	PEX_RX_15_N 6

Length-match XMT to AC coupling
and AC coupling to RCV

5 PCIE_REFCLK__P	AF7	EXP_REF_CLK_P	
5 PCIE_REFCLK__N	AE7	EXP_REF_CLK_N	
EPR_DO	B25	EPR_DO	
EPR_DI	C22	EPR_DI	
EPR_SK	B20	EPR_SK	
EPR_CS	C21	EPR_CS	

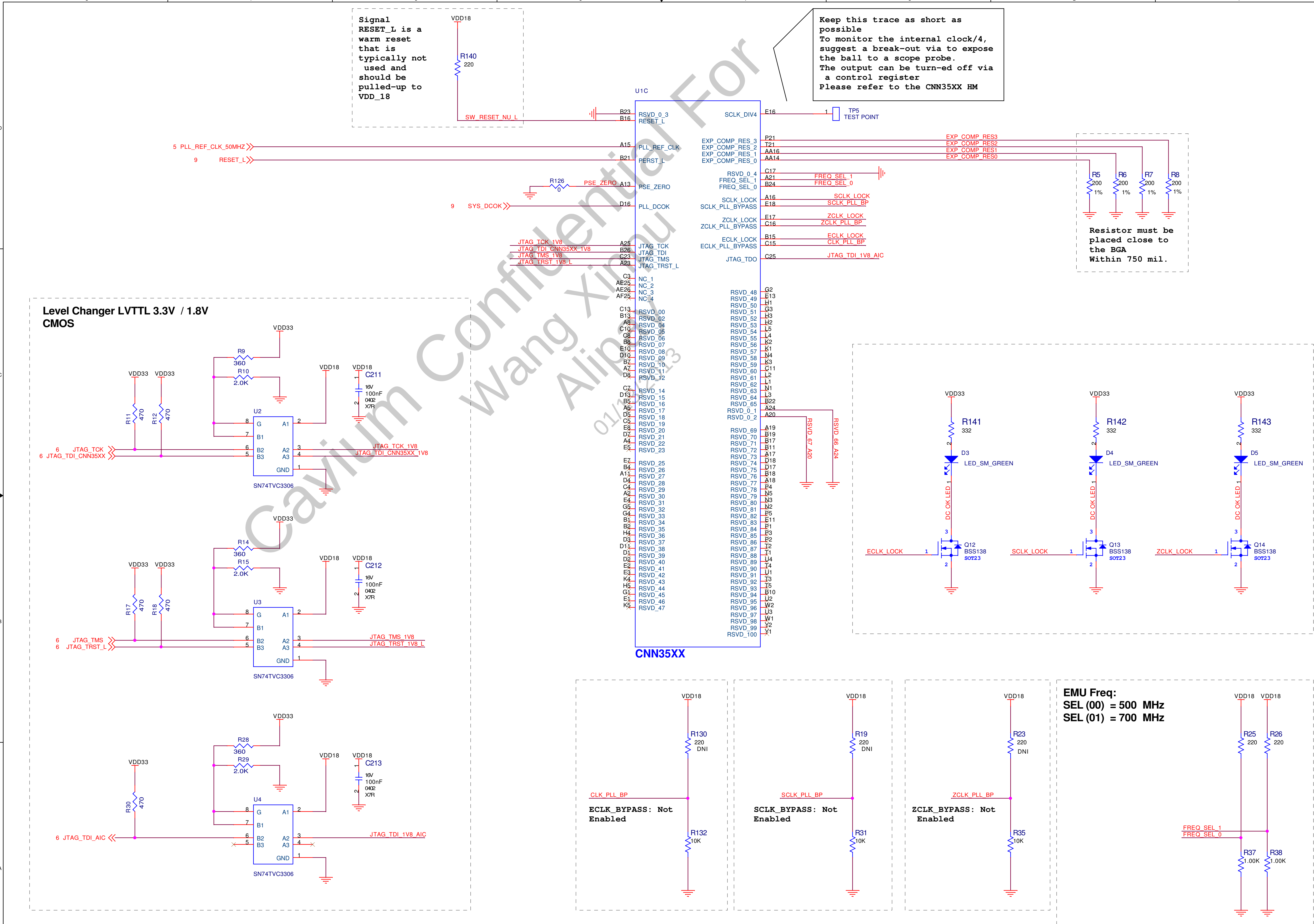
CNN35XX

Optional EEPROM



CAVIUM NETWORKS

Rev A1.12	**CNN35XX - PCIe LANES**	DATE: Friday, February 24, 2012
Project	Engineer: TM Engineering	PAGE: 2 of 9



CAVIUM NETWORKS	Rev A1.12	CNN35XX - MISC Circuits	DATE: Friday, February 24, 2012
	Project	Engineer: TM Engineering	PAGE: 3 of 9

CORE_VDD

EXP_VDD_VPTX

U5B

CNN35XX

VDD18

EXP_VDD_VPH

EXP_VDD_09_FLT

PLL_E_VDD_18V

PLL_E_VSS_18V

PLL_S_VDD_18V

PLL_S_VSS_18V

PLL_Z_VDD_18V

PLL_Z_VSS_18V

VDDQ

VDD_SENSE

VSS_SENSE

CNN35XX

U1D

Route as differential pair

CORE_VDD_SNS 7

CORE_VDD_SNS_RETRN 7

Place components close to the BGA
All traces are to be as short as possible

PLL_VDD_18V

PLL_E_VDD_18V — R134 100

C207 100nF — C210 22uF Tantalum

PLL_E_VSS_18V

PLL_VDD_18V

PLL_S_VDD_18V — R135 100

C206 100nF — C208 22uF Tantalum

PLL_S_VSS_18V

PLL_VDD_18V

PLL_Z_VDD_18V — R136 100

C205 100nF — C209 22uF Tantalum

PLL_Z_VSS_18V

EXP_VDD_09

EXP_VDD_09_FLT — L10 1500MA 120@100MHZ

C250 100nF — C251 100nF — C248 100nF — C249 10uF

EXP_VDD_VPTX Decoupling Caps

EXP_VDD_VPTX

C34 XTR 10uF 1206 — C35 XTR 10uF 1206 — C36 100nF — C37 1000nF — C38 100nF — C39 1000nF — C40 100nF — C41 1000nF — C42 100nF — C43 1000nF — C44 100nF — C45 1000nF — C46 100nF — C47 1000nF — C48 100nF — C49 1000nF — C50 100nF — C51 1000nF — C52 100nF — C53 1000nF — C54 100nF — C55 1000nF — C56 100nF — C57 1000nF

EXP_VDD_VPH Decoupling Caps

EXP_VDD_VPH

C73 XTR 10uF 1206 — C74 XTR 10uF 1206 — C75 100nF — C76 1000nF — C77 100nF — C78 1000nF — C79 100nF — C80 1000nF — C81 100nF — C82 1000nF — C83 100nF — C84 1000nF — C85 100nF — C86 1000nF — C87 100nF — C88 1000nF — C89 100nF — C90 1000nF — C91 100nF — C92 1000nF — C93 100nF — C94 1000nF — C95 100nF — C96 1000nF

VDD18 Decoupling Caps

VDD18

C112 XTR 10uF 1206 — C113 XTR 10uF 1206 — C114 100nF — C115 1000nF — C116 100nF — C117 1000nF — C118 100nF — C119 1000nF — C120 100nF — C121 1000nF — C122 100nF — C123 1000nF — C124 100nF — C125 1000nF — C126 100nF — C127 1000nF — C128 100nF

HS1

Heat Sink

CORE_VDD Decoupling Caps

CORE_VDD

C58 XTR 10uF 1206 — C59 100nF — C60 1000nF — C61 100nF — C62 1000nF — C63 100nF — C64 1000nF — C65 100nF — C66 1000nF — C67 100nF — C68 1000nF — C69 100nF — C70 1000nF — C71 100nF — C72 1000nF — C214 100nF

CORE_VDD

C97 XTR 10uF 1206 — C98 100nF — C99 1000nF — C100 100nF — C101 1000nF — C102 100nF — C103 1000nF — C104 100nF — C105 1000nF — C106 100nF — C107 1000nF — C108 100nF — C109 1000nF — C110 100nF — C111 1000nF — C215 100nF

CORE_VDD

C216 XTR 10uF 1206 — C217 100nF — C218 1000nF — C219 100nF — C220 1000nF — C221 100nF — C222 1000nF — C223 100nF — C224 1000nF — C225 100nF — C226 1000nF — C227 100nF — C228 1000nF — C229 100nF — C230 1000nF — C231 100nF

CORE_VDD

C232 XTR 10uF 1206 — C233 100nF — C234 1000nF — C235 100nF — C236 1000nF — C237 100nF — C238 1000nF — C239 100nF — C240 1000nF — C241 100nF — C242 1000nF — C243 100nF — C244 1000nF — C245 100nF — C246 1000nF — C247 100nF

CAVIUM NETWORKS

Rev A1.12

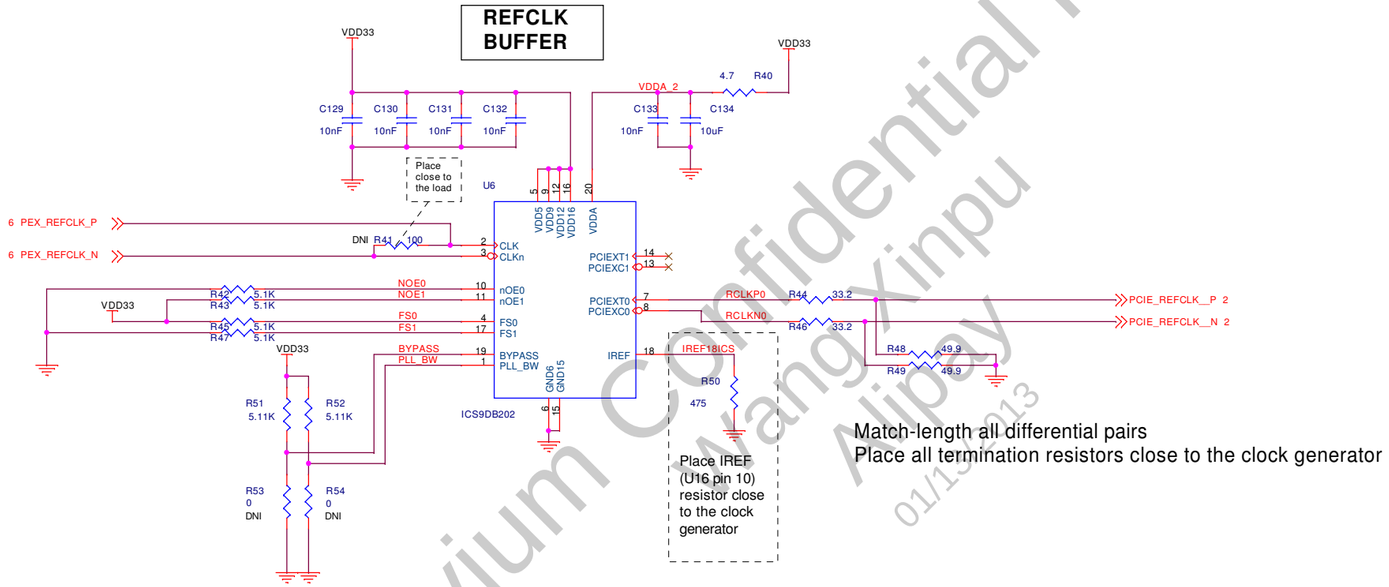
Project

CNN35XX - PWR - GND

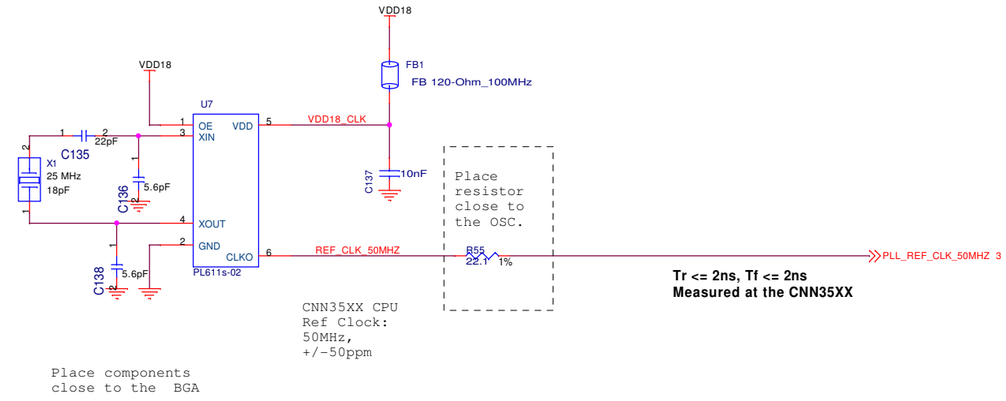
Engineer: TM Engineering

DATE: Friday, February 24, 2012

PCIe 100MHz Reference Clock Gen.

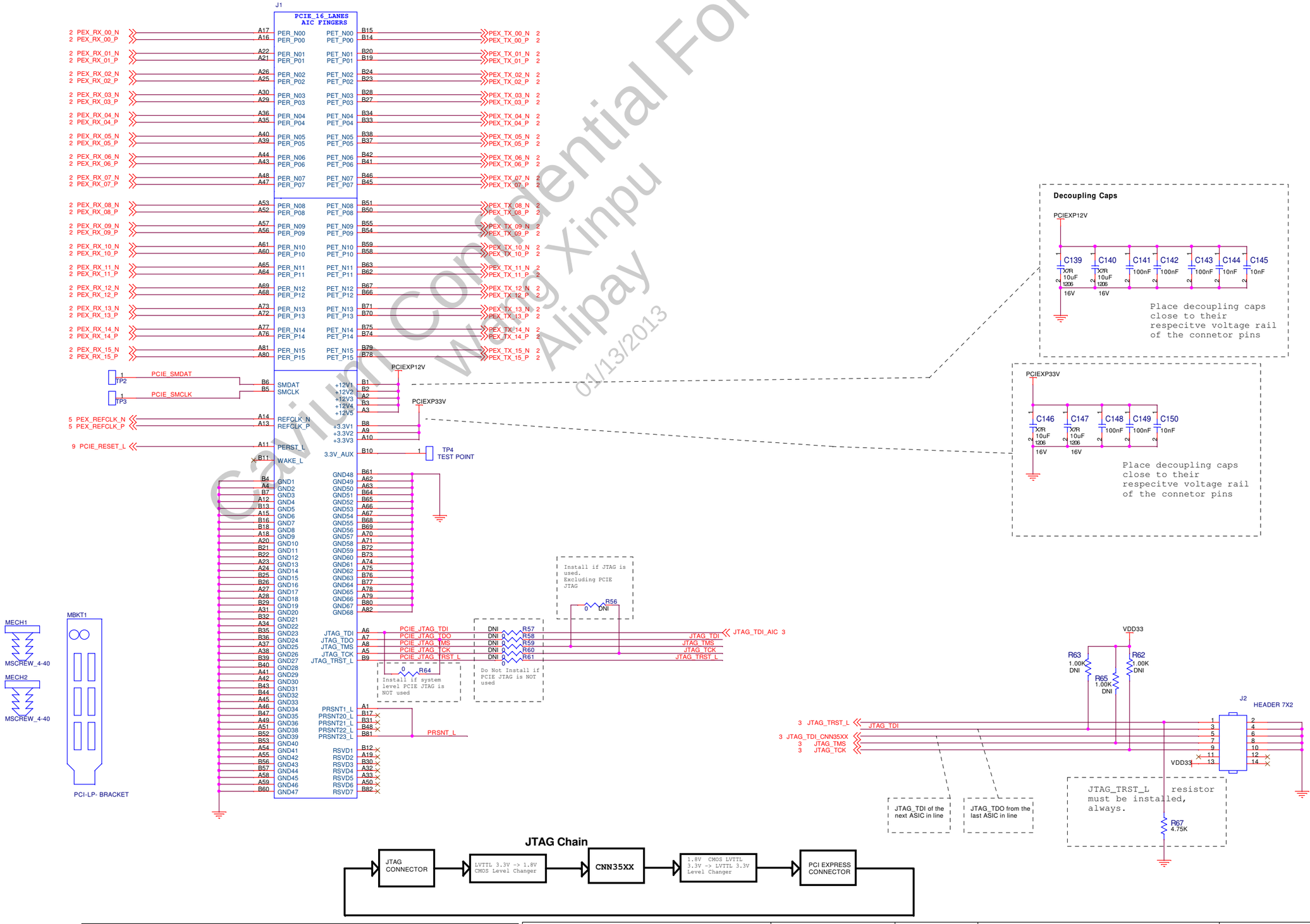


PLL REFERENCE CLOCK
50 MHz



CAVIUM NETWORKS

Rev	CLOCK GENERATION	DATE:
A1.12		Friday, February 24, 2012
Project	Engineer: TM Engineering	PAGE: 5 of 9



CAVIUM NETWORKS

Rev A1.12	PCIe AIC CONNECTOR	DATE: Friday, February 24, 2012	
Project	Engineer: TM Engineering	PAGE: 6 of 9	

VDD50
C151 2.2uF
R68 10
CV_VCC
VDD33
C156 2.2uF
C157 100nF
R69 15K
AGND_VDD
U8
PGND
VCC
PVCC
9 CV_PGOOD
PGOOD
BOOT
F_osc = 500KHz
DNI
0
R71
CV_FSEL
100K
R72
DNI
FSEL
UGATE
AGND_VDD
8 PWR_RAILS_PGOOD
R74 33E
PGOOD
EN
PHASE
SN_CV_RTN
R77 4.42K
CV_RTN
RTN
LGATE
R80 3.4K
CV_SS
10ms
C165 0.33uF
SREF
OCSET
AGND_VDD AGND_VDD AGND_VDD
GND
Vo
FB
ISL95870
R81 0
AGND_VDD
SHORT GROUNDS
LOCATE UNDER PART CENTER
Refer to the ISL95870 data sheet for layout instructions
PCIEXP12V
L1
0.15UH
CV_TFET12V
C152 150uF
C153 22UF
C154 22UF
C155 10nF
CV_BOOT
C158 0.22uF
Q1
FDMS3602S
R70 0
CV_TGR
R73 0
CV_TG
CV_LX_PHASE
CV_BGR
R78 0
CV_BG
CV_OCSET
CV_VO
CV_FB
R82 Rtop 4.7K
Rbot
R85 5.8K
AGND_VDD
Vout = 0.5V
* [(R_top / R_bot) +1]
L2
0.36uH
R76 19.6K
R75 4.42K
C163 0.056UF
C164 2.2nF
R79 4.42K
C162 100nF
C159 47uF
C160 470uF
C161 470uF
CORE_VDD
900mV
Run as differential Pairs
SN_CV_P1V
SN_CV_RTN
Run as differential Pairs
Place components at load for remote sensing!
R83 0
R84 0
CORE_VDD_SNS 4
CORE_VDD_SNS_RETRN 4
Route as differential pair

VDD33
L3
4.7uH
P33VF_EXP_VDD_09
C167 10uF
C166 1uF
R86 10.0K
PWR_RAILS_PGOOD
U9
VIN_1
VIN_2
VOUT_1
VOUT_2
SENSE/ADJ
ENABLE
PAD_GND
GND
PG
ISL80101
Approx 2.5ms delay
EXP_VDD_09_SS
C170 10nF
EXP_VDD_09_ADJ
Rtop
R87 4.7K 1%
R88 5.8K 1%
Rbot
C168 1uF
C169 10uF
EXP_VDD_09
900mV
EXP_VDD_09
900mV Rail
CV_PGOOD
Vout = 0.5V
* [(R_top / R2_bot) +1]

CAVIUM NETWORKS

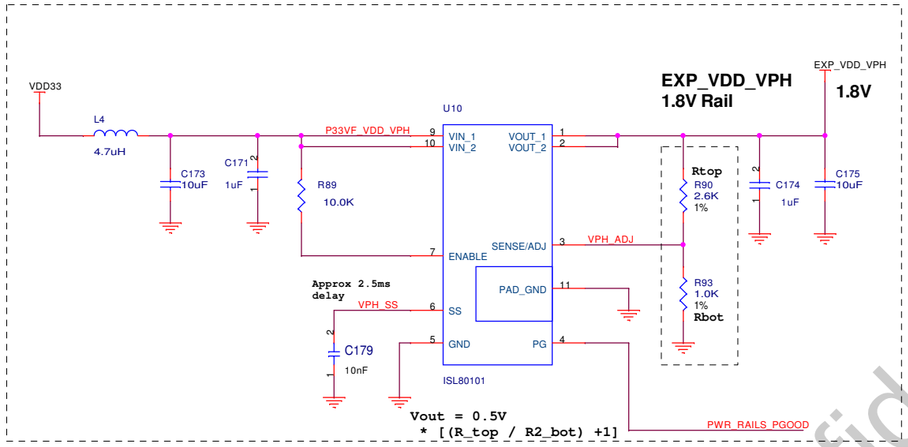
Rev A1.12

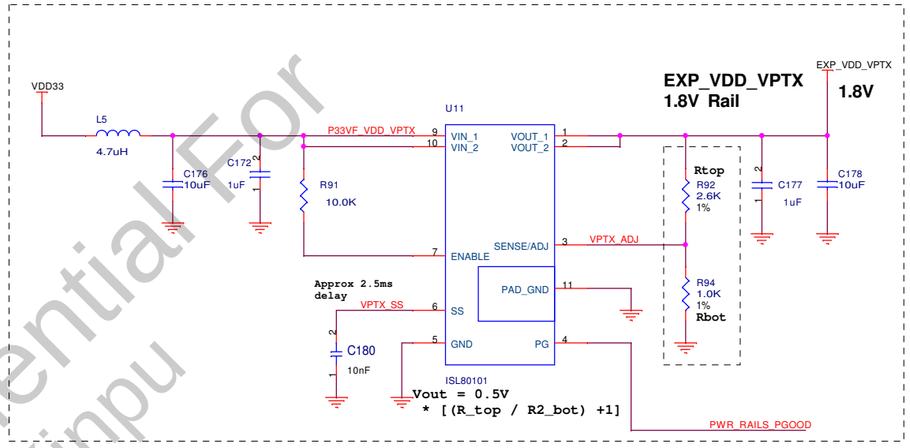
Project

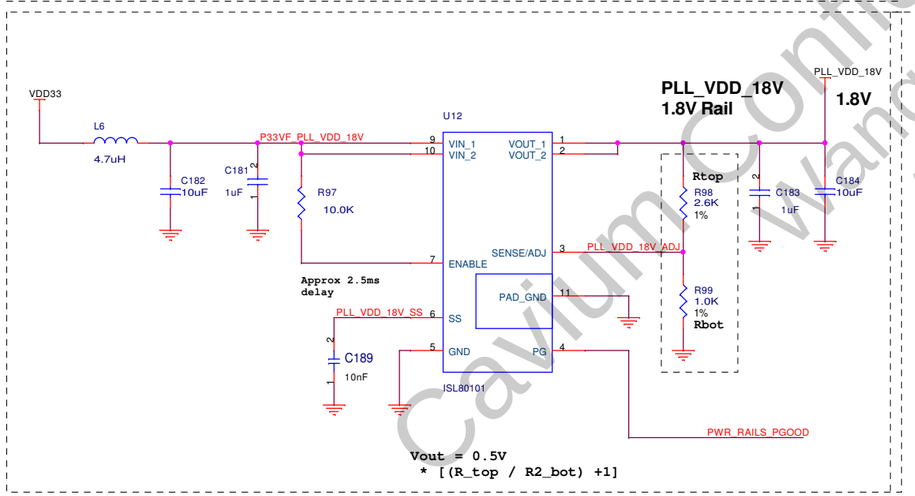
POWER SUPPLIES

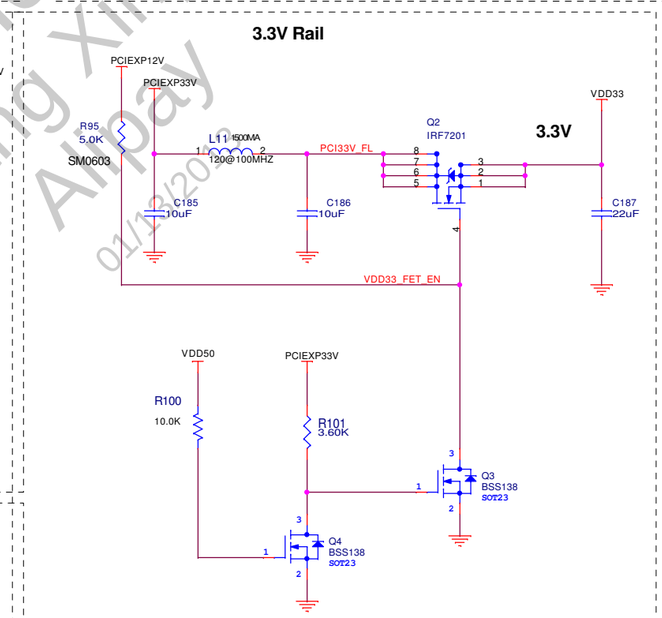
Engineer: TM Engineering

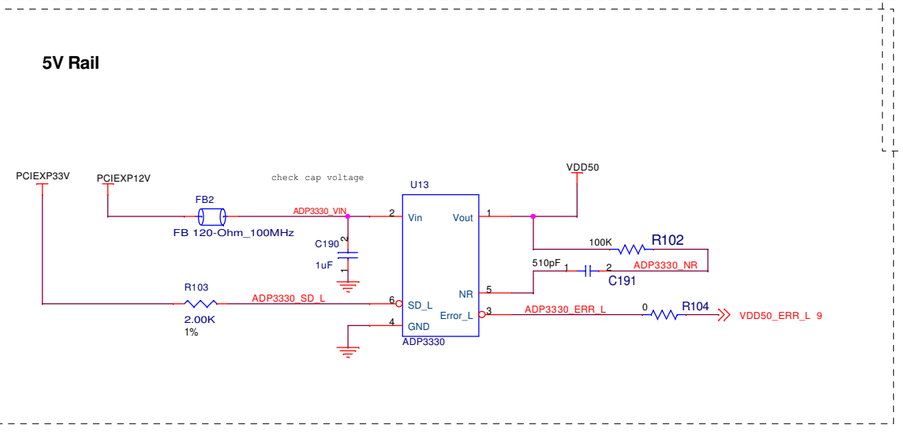
DATE: Friday, February 24, 2012

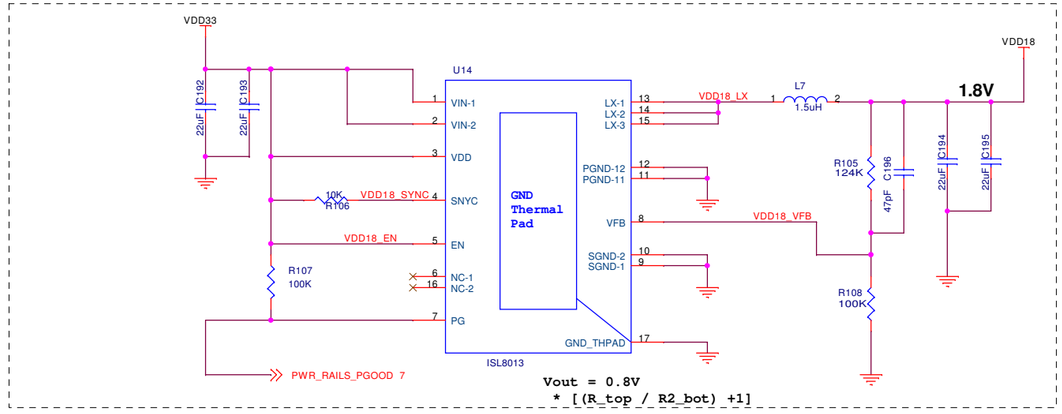












CAVIUM NETWORKS

Rev A1.12

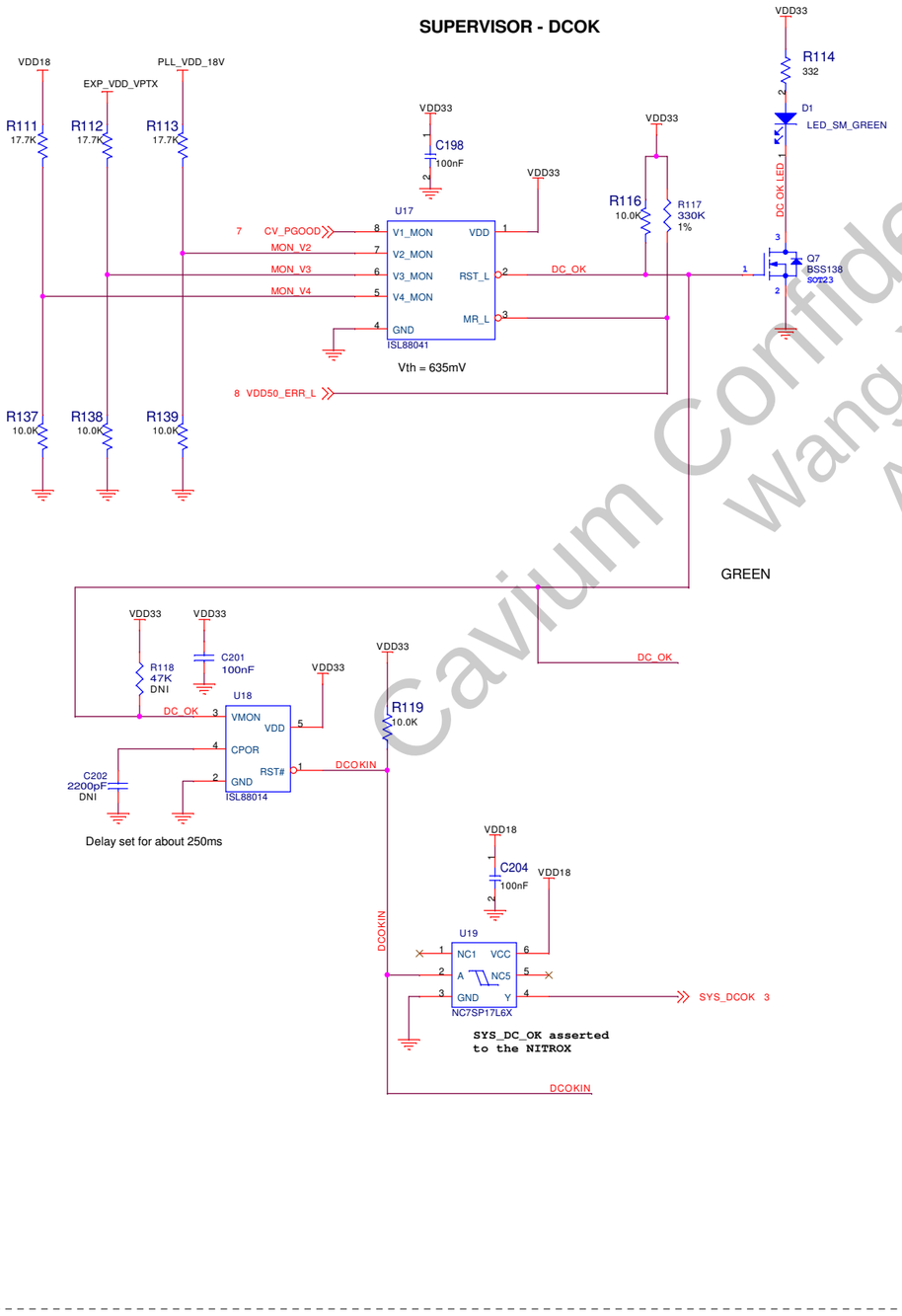
Project

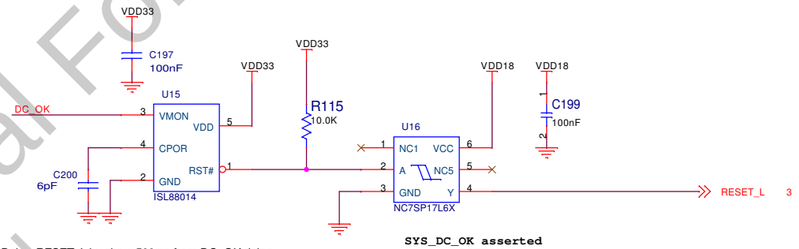
POWER SUPPLIES

Engineer: TM Engineering

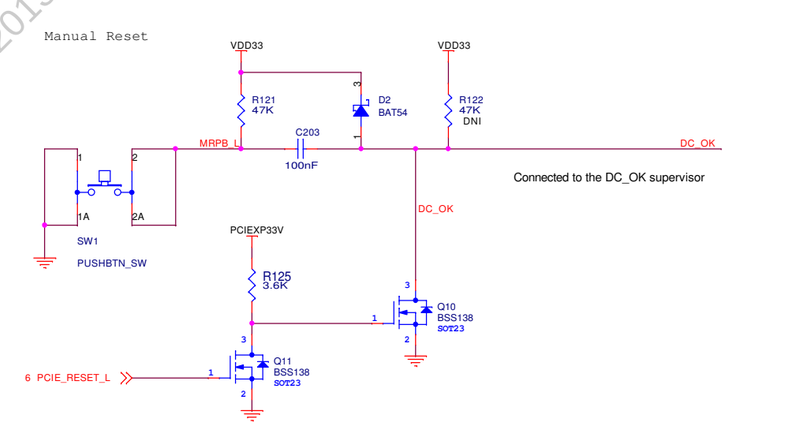
DATE: Friday, February 24, 2012

SUPERVISOR - DCOK





Manual / Power-UP Reset



CAVIUM NETWORKS

Rev	RESET - PWR SEQUENCING	DATE:
A1.12		Friday, February 24, 2012
Project	Engineer: TM Engineering	PAGE: 9 of 9