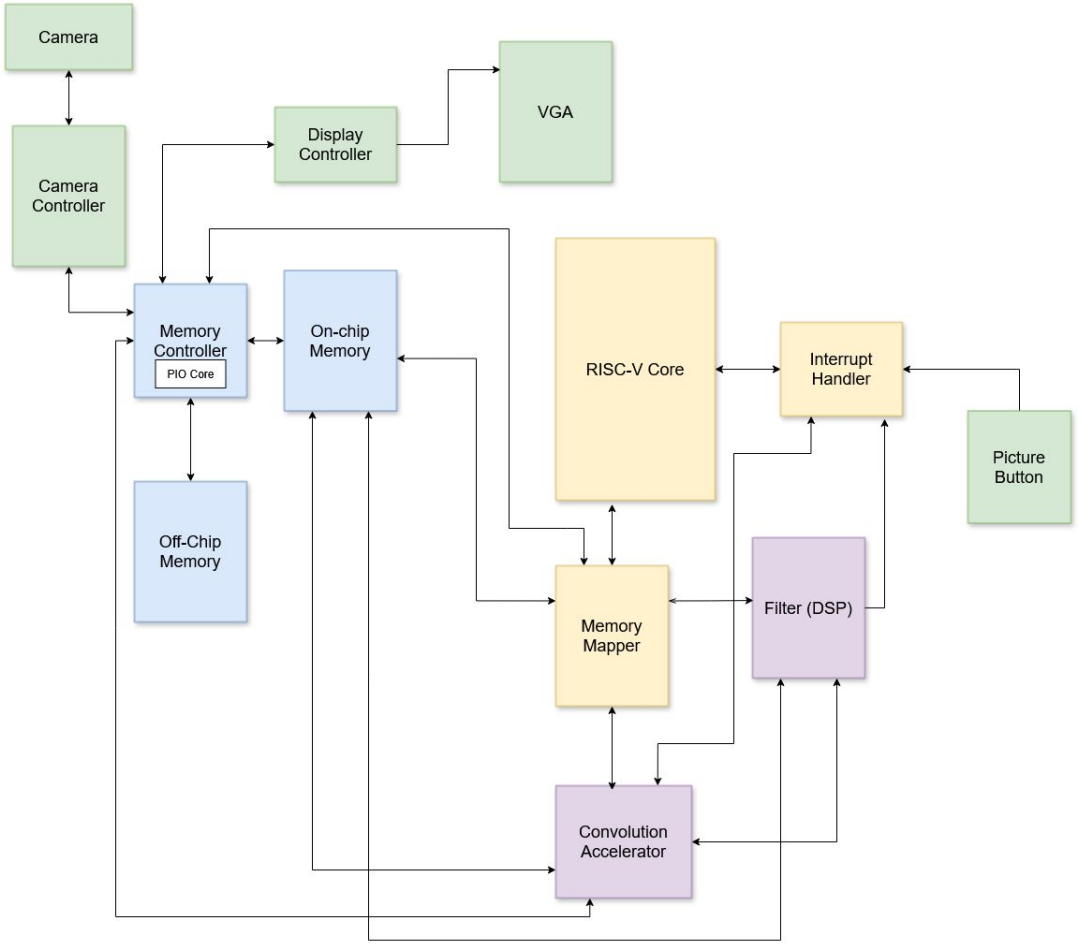
Face Filter Architectural Review

Block Diagram



Processor Implementation

- RISC-V
  - ISA: RV32I
    - CSRs for Interrupts

- Interrupts

  I/O, Picture Button (Interrupt Service Routine stored at predefined memory space)

- Memory Controller
  - SDRAM and On-Chip Memory

Algorithms to Accelerate

- Convolution
- Normalization
- ReLU function
- Filter

Accelerator Implementation

Communication with Processor

- Control, status registers in memory map

MAC array based implementation of convolution operations

- Timing control and mapping FSM/Assembly to finish all layers

ReLU and Normalization

- based on MUX or adders/shifters

Filter module

- Bitwise operation of the selected area of the image

External Interfaces

- Camera (D5M)
- Display Monitor (VGA)

Verification of Original Plan

Deviations

- Taking a still frame to apply the face filter to instead of video
  - Reduced the amount of extensions/special features for the processor (no out-of-order/superscalar)
  - Implementing interrupts in the processor to support communication with external modules

Thank You