Face Filter Project Overview

ECE 554 Team Project

Team Introduction

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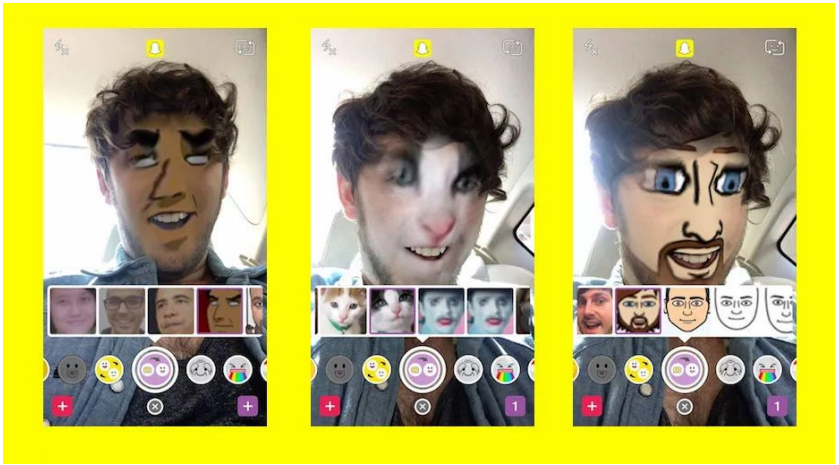
Motivation

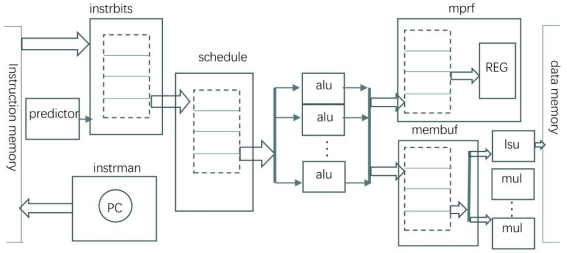
Image processing and AI technologies have always attracted attention across various fields, hardware accelerators dedicated to convolution operations are of major research interests. In this project, we wish to provide better solutions for convolution acceleration and combine it with signal processing to build a real world application.



Approach

- RISC-V CPU - major control and instruction execution (SSRV or SCR1)
- Convolution Accelerator - facial recognition
- DSP Unit - apply the face filter real-time
- VGA Interface - display the image
- On-board Memory - store instructions, CNN parameters and image data
- Software development - train the AI model, complete the main program

Anticipated Challenges



Out-of-Order Processor Design Resource Usage:

Out-of-Order one built on baseline RISC-V Processor), but SSRV need more resources than what DE1 can offer (Logic Element Resources, Memory Adjustments to Open-Source RISC-V)

Memory Bandwidth:

Data transfer overhead largely decreases efficiency in convolution calculations.

Convolution result and VGA:

Large image puts pressure on the CNN model and small CNN models have trouble interfacing with VGA (1280*960)

Design trade-offs:

Memory-mapping the accelerator VS integrating it into execution pipeline has an impact on ISA design

Parallelism VS serial execution of convolution operations determines hardware size and mapping algorithms

Risk Management

1. Use high-level synthesis tools and pre-built IP cores to simplify design.

2. Optimize the AI model (such as MobileNetV1) and hardware design to fit within resource constraints to solve the limited FPGA resources.

3. Use pipelining and parallelism to maximize throughput to solve the real-time performance constraints.

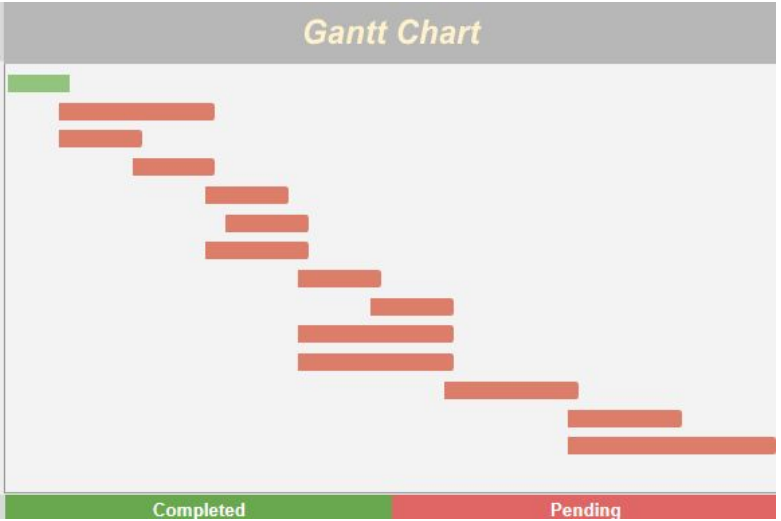
4. Research general designs of convolution accelerators and explore trade-offs

Milestones and Evaluation

- Finish model selection and training in python
- Develop convolution accelerator
- Develop digital signal processing unit
- Interface with VGA
- Finish CPU design and software design

Gantt Chart

Task	Start Date	End Date	Progress
Project Proposal	2/20/2025	2/25/2025	100%
Create Facial Recognition Model	2/25/2025	3/11/2025	0%
Architectural Review	2/25/2025	3/4/2025	0%
Microarchitectural Review	3/4/2025	3/11/2025	0%
Interface Design	3/11/2025	3/18/2025	0%
Interface Testing	3/13/2025	3/20/2025	0%
Basic Building Blocks Implementation	3/11/2025	3/20/2025	0%
Accelerator Design	3/20/2025	3/27/2025	0%
Accelerator Testing	3/27/2025	4/3/2025	0%
Filter Model Design	3/20/2025	4/3/2025	0%
Processor/Accelerator Implementation & Basic Software Support	3/20/2025	4/3/2025	0%
Complete System Implementation/Final Touches and Debugging	4/3/2025	4/15/2025	0%
Demo Poster	4/15/2025	4/25/2025	0%
Final Report	4/15/2025	5/4/2025	0%
Overall Status	**2/20/2025**	**5/4/2025**	**6.67%**



Team Responsibilities

Han Lyu - AI model training, accelerator design, DSP unit design

Allie Bacholl - CPU Design and Testing, Peripheral Interfaces

Tianqi Shen - CPU Design and Accelerator Design

Jingyu Liu- Testing and AI design, software design

Thank you!