Face Filter Microarchitectural Review

Accelerator Overview

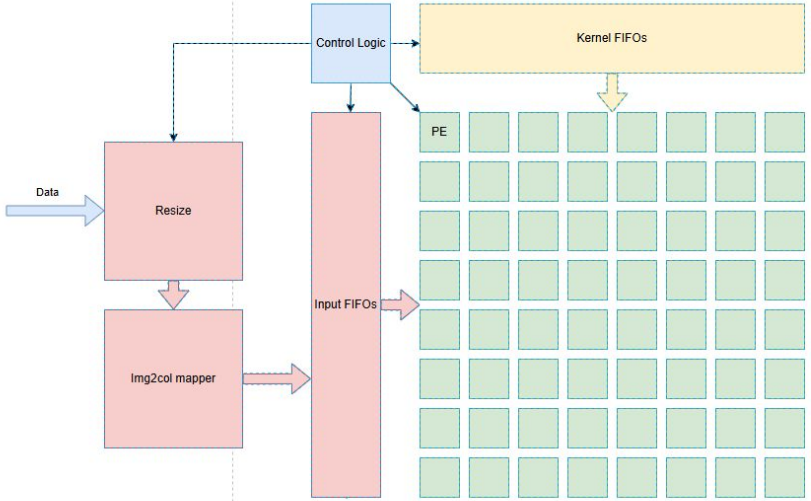
Systolic Array

Control Logic

Resize Unit (for CNN)

Img2col mapper

FIFOs

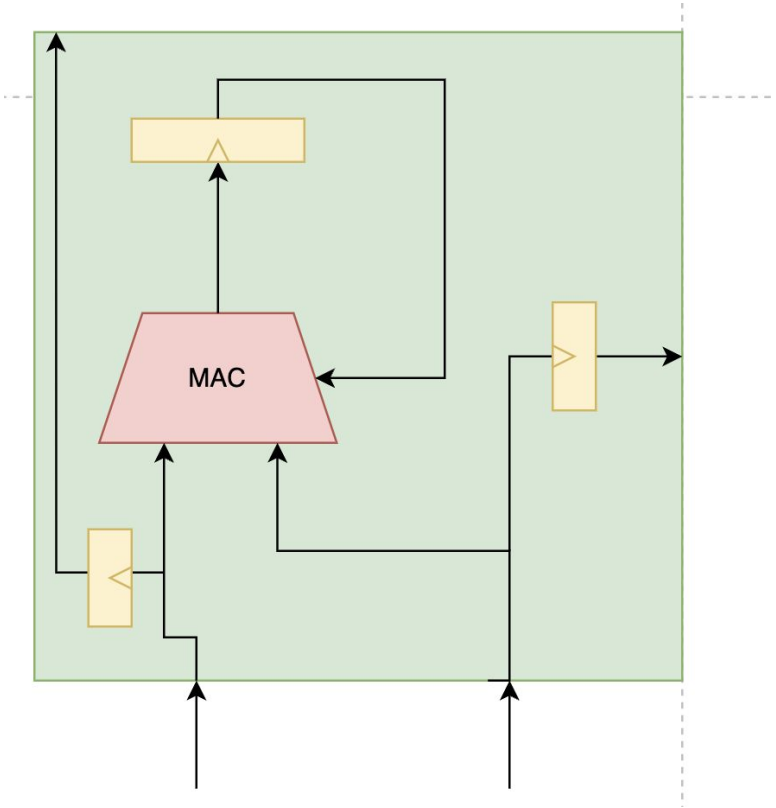


PE Internal Structure

MAC unit

Registers (clk, rst, clr and enable)

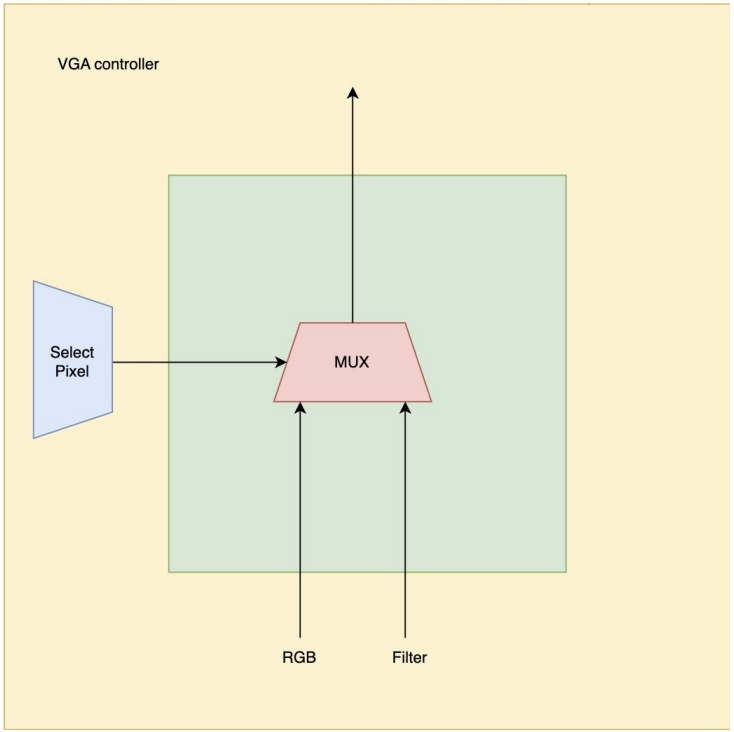
Adder



Overlaying Unit

Insert inside VGA controller

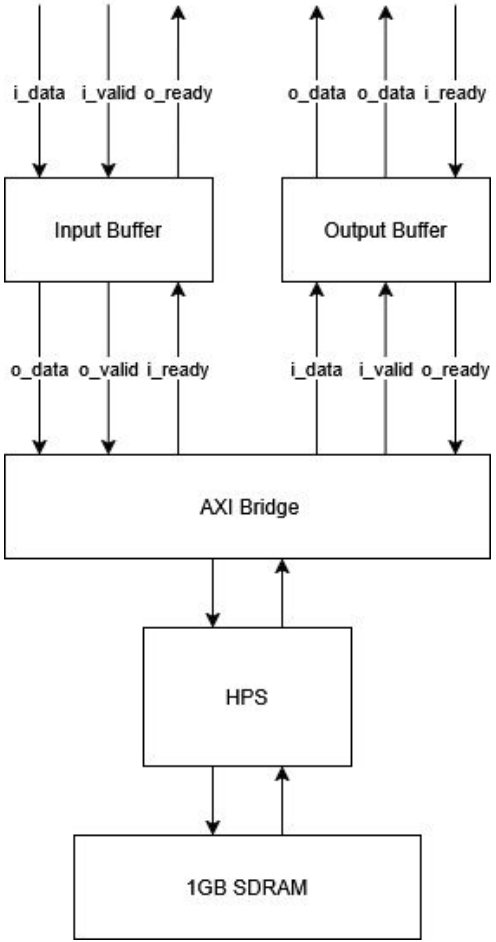
Replace RGB with the filter of certain locations



Memory Overview

AXI4-Lite (1GB DDR3)

- Kernel Values
- Frame from Camera
- Output from Accelerator
- Output from Overlay



shows how a read transaction uses the read address and read data channels.

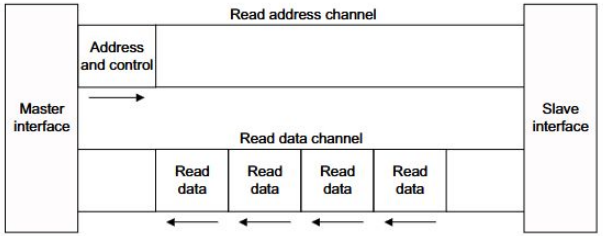


Figure A1-1 Channel architecture of reads

shows how a write transaction uses the write address, write data, and write response channels.

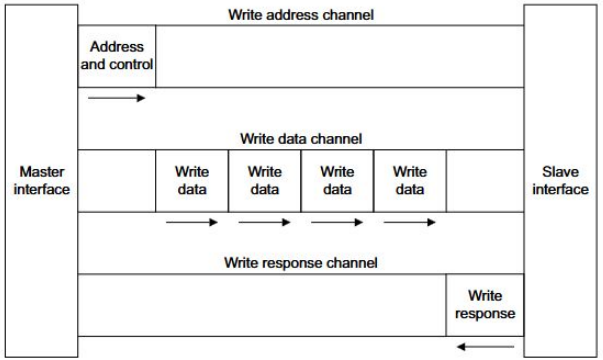
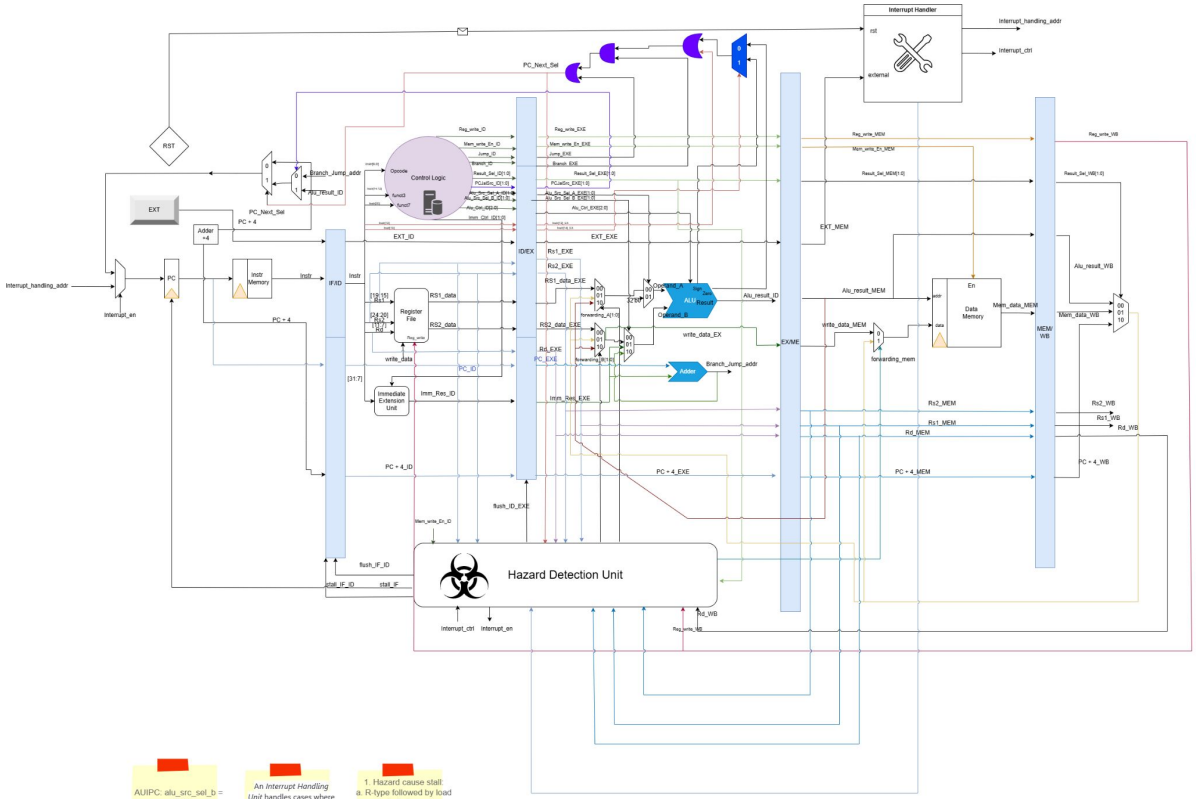


Figure A1-2 Channel architecture of writes

Processor Design: RISC-V 32I (excluding OS instructions)



AUIPC: alu_src_sel_b = 1'b1
LUI: using 32'b0 in operand A

An Interrupt Handling Unit handles cases where an external signal (INT or RST) overwrites the pipeline, or when executing a multicycle instruction.

1. Hazard cause stall:
a. R-type followed by load instr, i.e.
ADD $2, $4, $5
LW $7, $2, 5

2. Branch/Jump Resolution currently in exe stage