Introduction to FPGA Simulation and Debug

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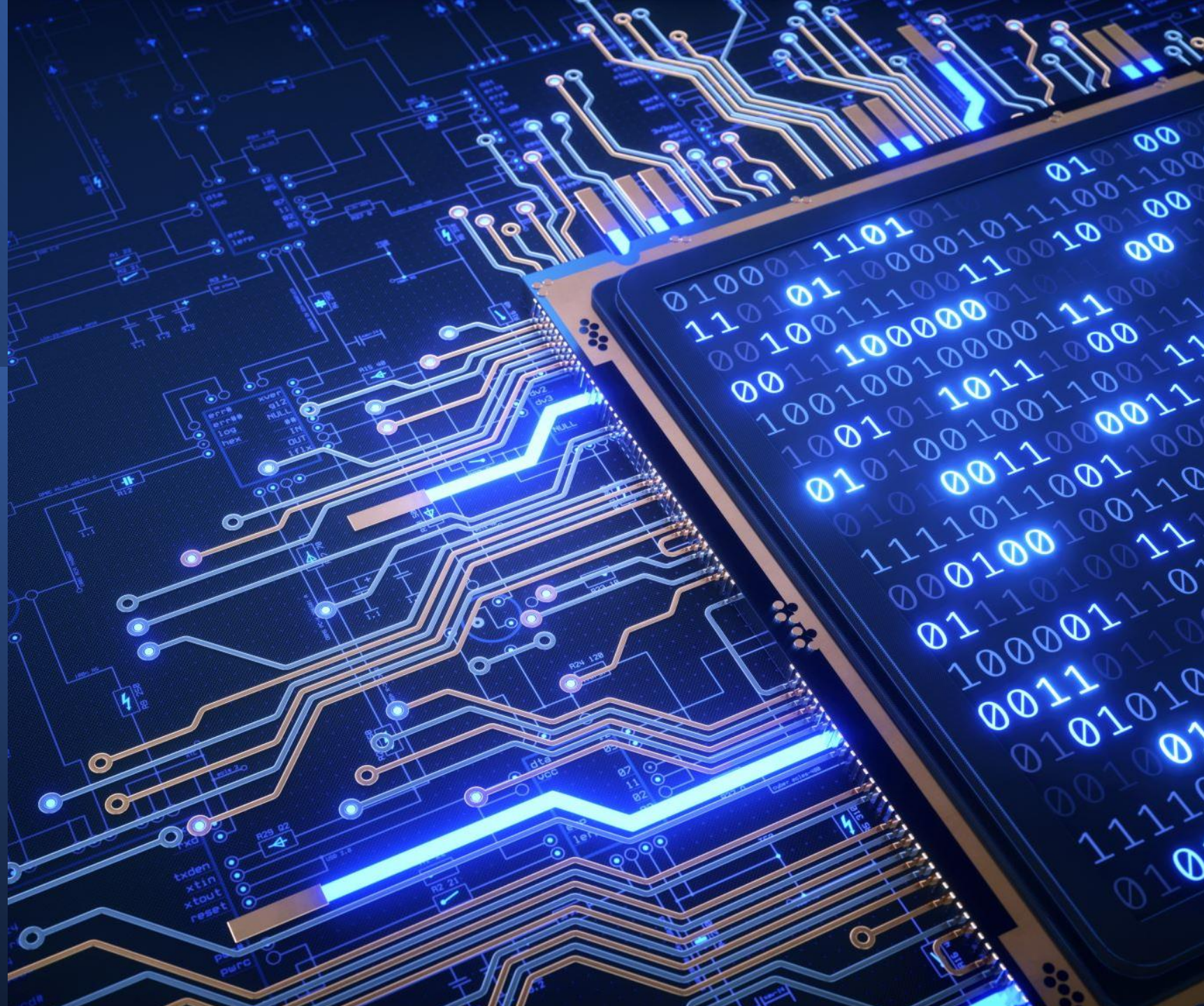
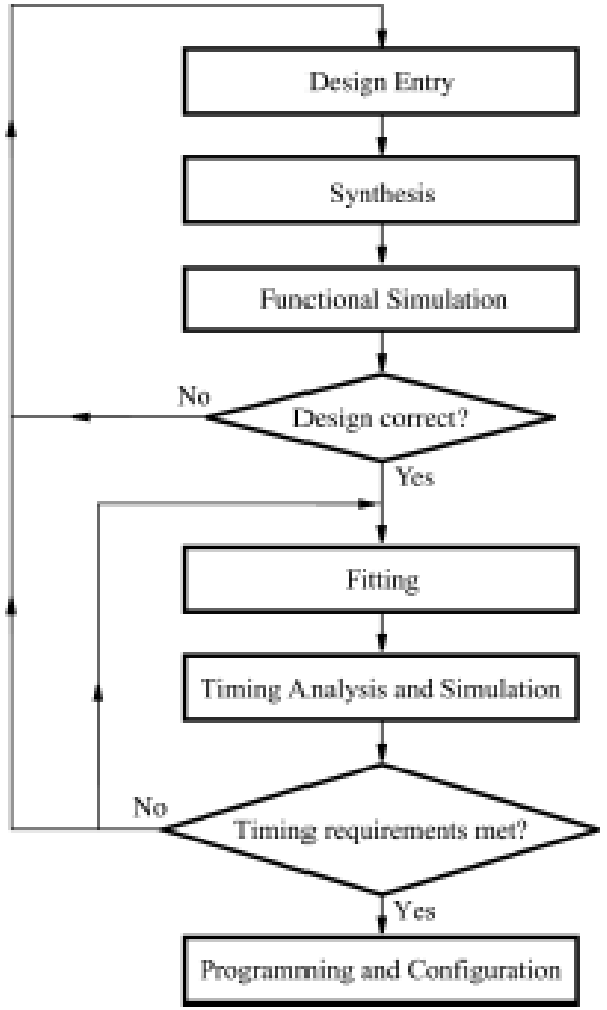


FPGA Design Flow

- Design Entry – HDL coding
- Synthesis – the design is mapped into a circuit that consists of the logic elements (LEs) provided in the FPGA.
- Functional Simulation – Test if the design is functionally correct.
- Fitting – Placement & Routing.
- Timing Analysis – propagation delays along the various paths in the fitted circuit are analyzed.
- Timing Simulation – The fitted circuit is tested to verify both its functional correctness and timing.
- Programming and Configuration – The designed circuit is implemented in a physical FPGA chip by programming the configuration switches that configure the LEs and establish the required wiring connections.



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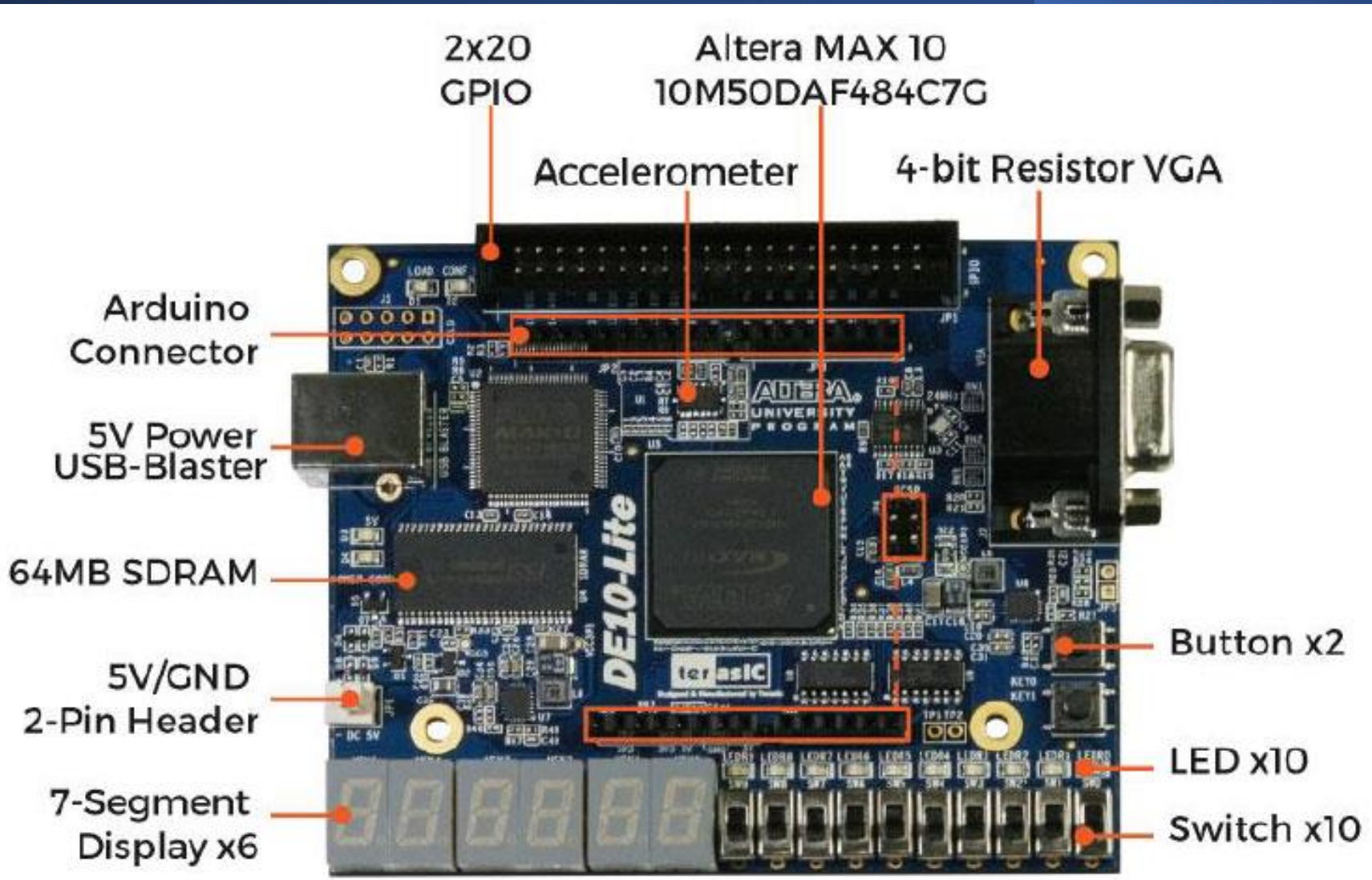
DE-Lite Max 10 series



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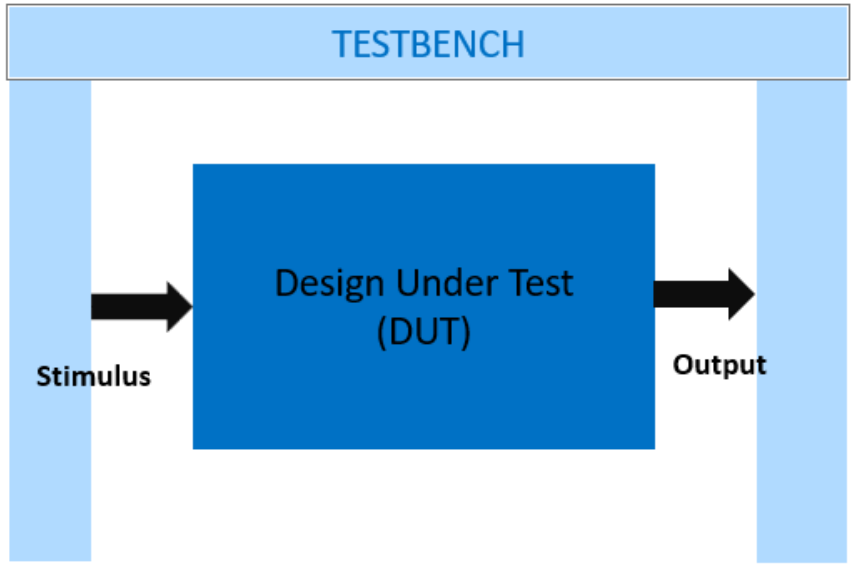
Why Simulation?

- Advantages:
  - Cost-effective: reduce development costs as it eliminates the need for physical hardware prototypes.
  - Early error detection: provide early bug detection before the design is implemented on the hardware.
  - High visibility of all signals in the design.
  - Faster time-to-market: provides early detection of design issues which reduces the overall development time.
- Disadvantages:
  - Hardware testing & performance: e.g. interacting with external peripherals and sensors.
  - Can take a long time to run – Software-based.

Testbench

- A test bench or testing workbench is an environment used to verify the correctness or soundness of a design or model.



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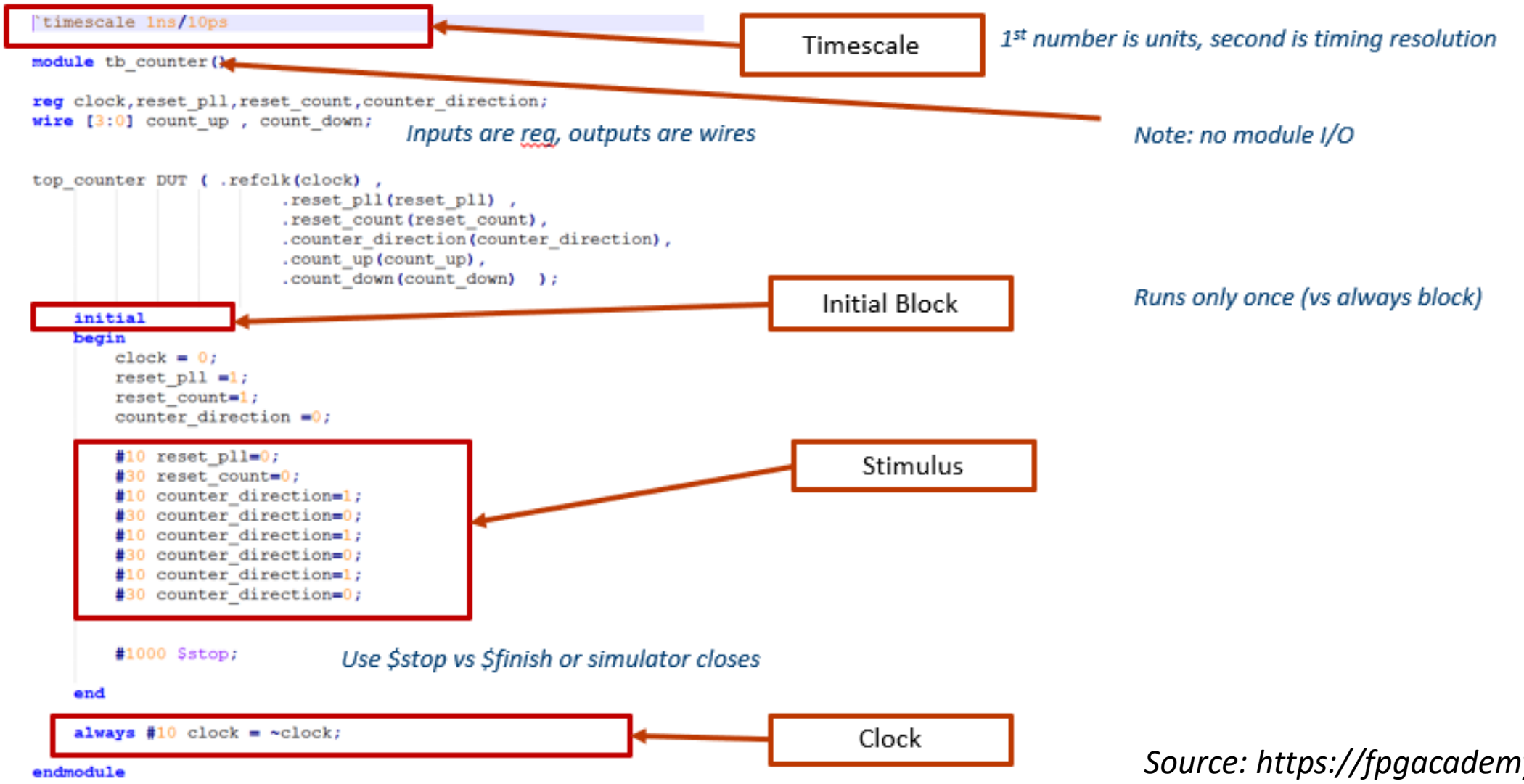
Verilog Testbench



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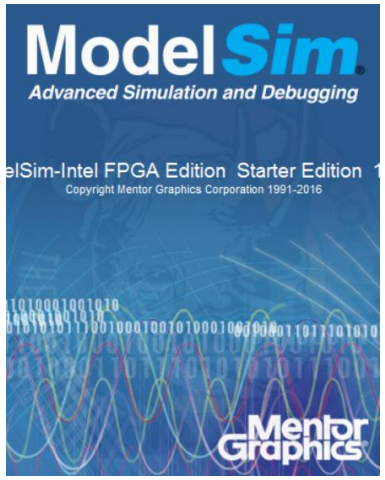
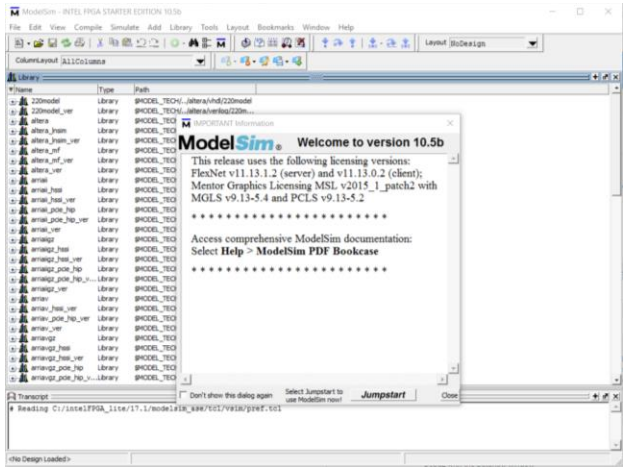
Mentor ModelSim Overview

- ModelSim is a multi-language HDL (Verilog/VHDL) simulation environment. It can be used independently or Intel Quartus can create startup scripts and link designs to ModelSim.
  - Intel Quartus has a license to distribute Modelsim-Altera with Quartus.





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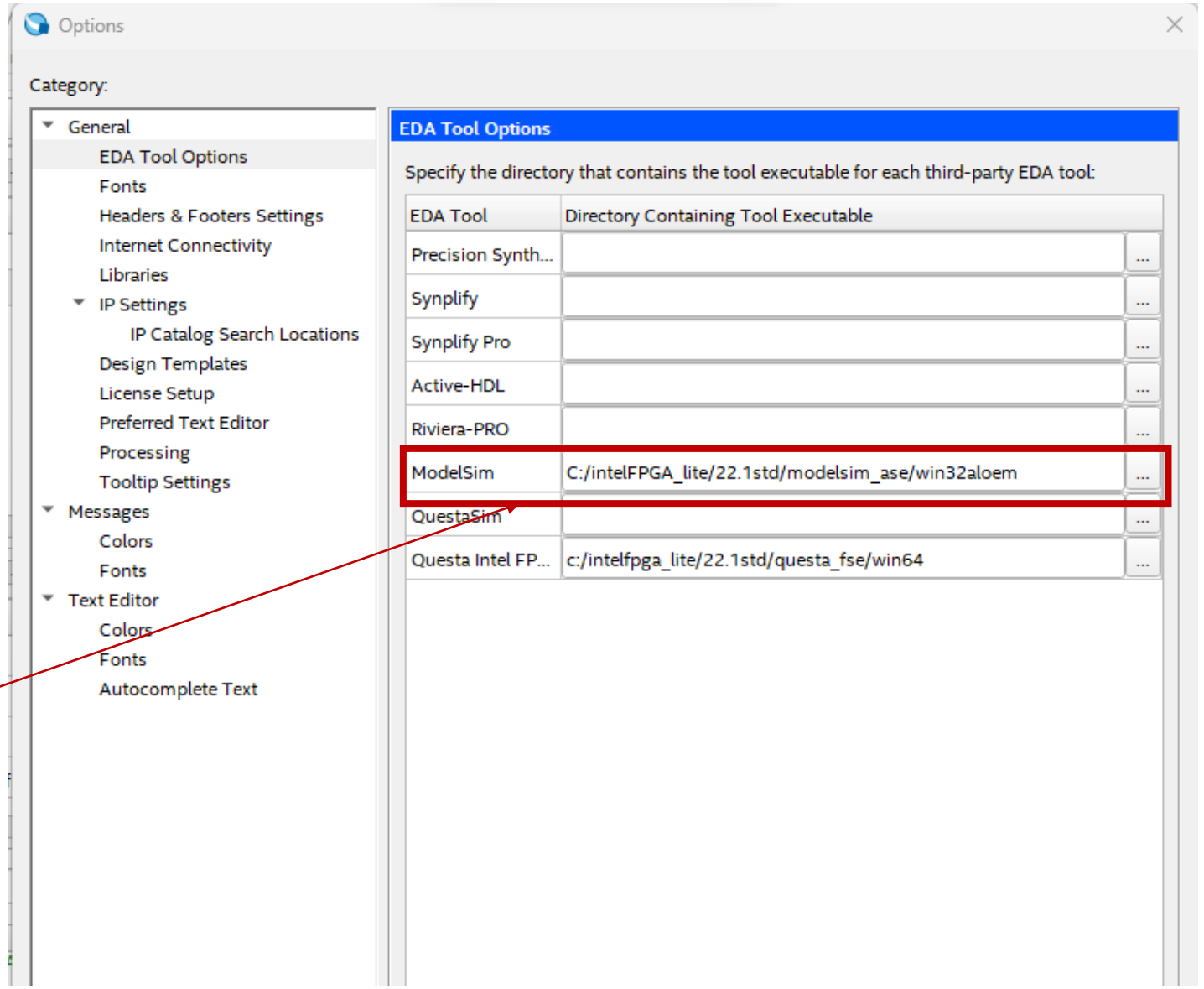
Modelsim setup - 1

- Go to Tools Options EDA Tool Options. In ModelSim-Altera, enter the executable pathway.

This path might be different for your own installation!



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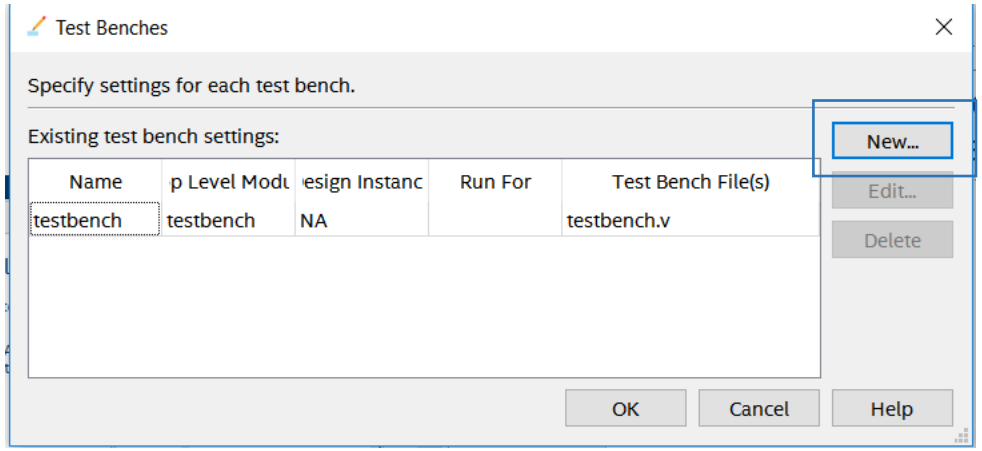
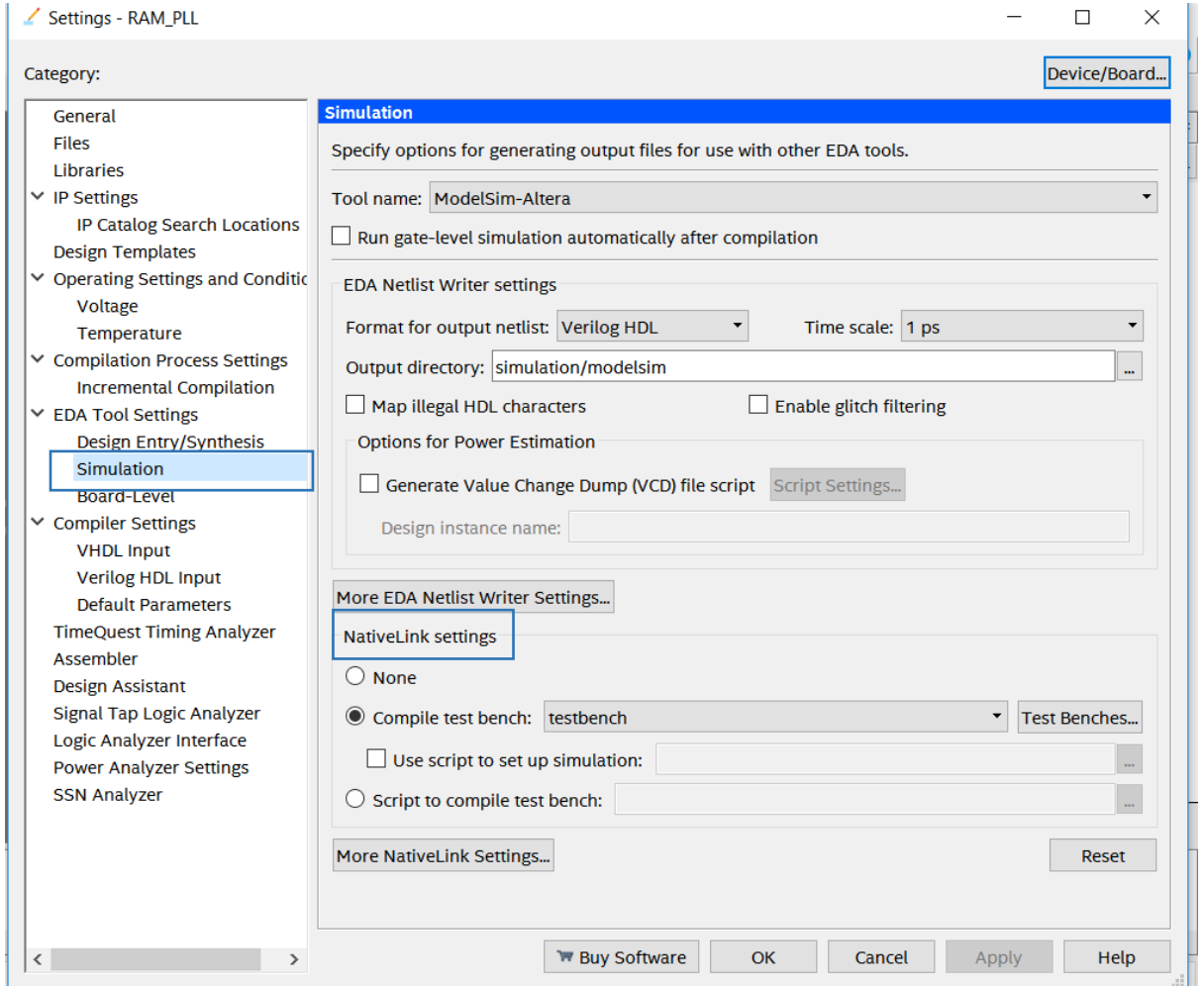
Setting up ModelSim from Intel Quartus

- Assignments → Settings→ EDA Tools Settings → Simulation
- In NativeLink Settings → Test Benches → NEW
- Add New testbench → OK





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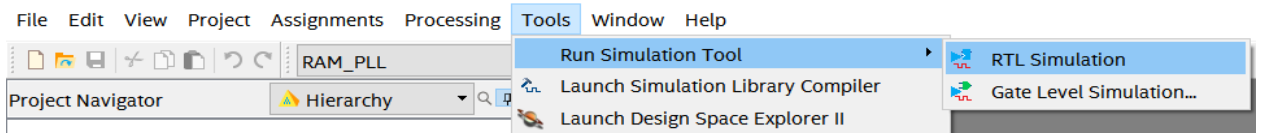
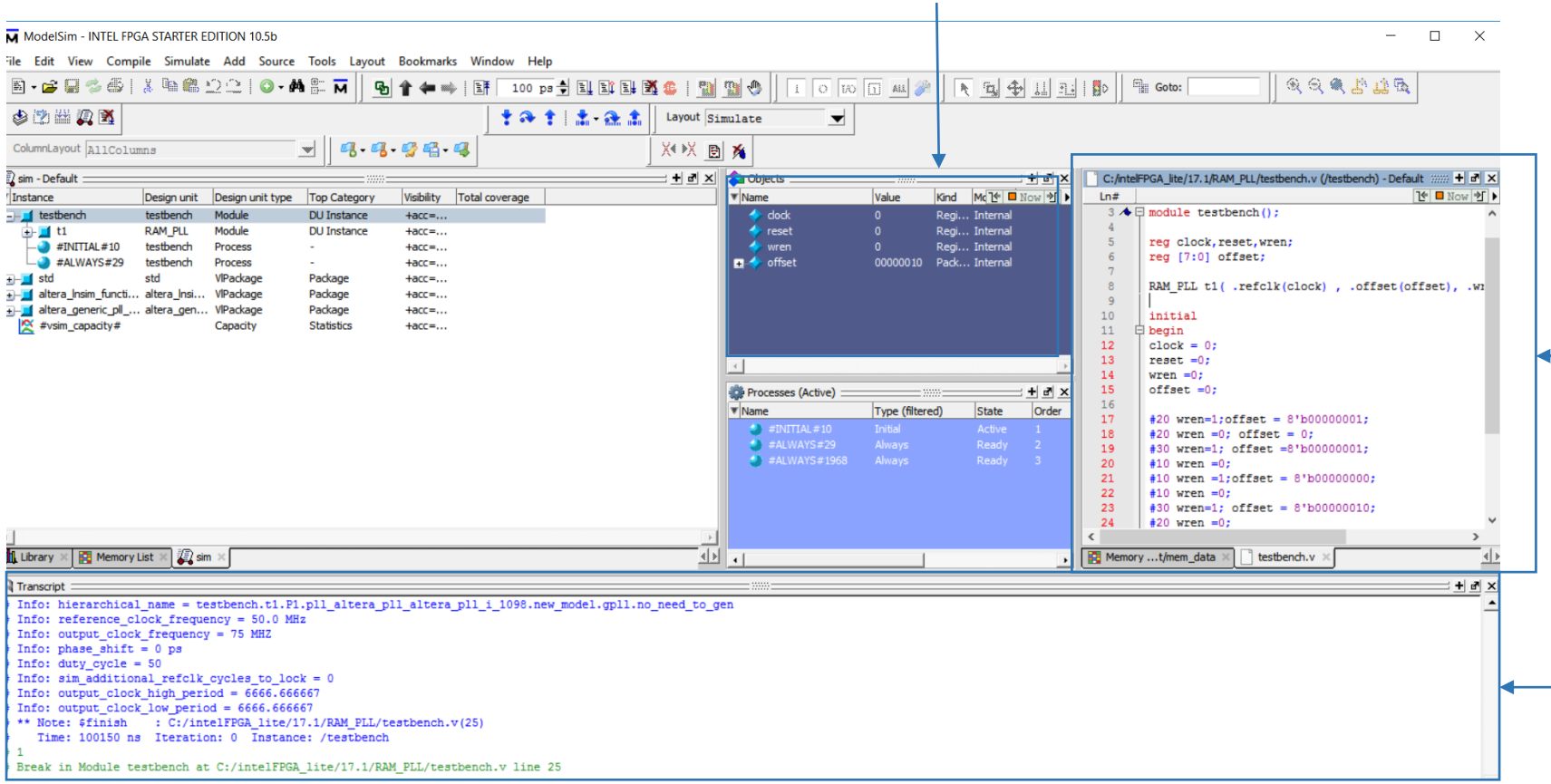
ModelSim GUI

Launching ModelSim from Quartus Tools →Run Simulation Tool → RTL Simulation



Simulation Objects



Testbench File

Command Transcript Window

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Example

- Implement the Majority Function logic circuit as defined by the following expression.

$$f(x_1, x_2, x_3) = x_1 x_2 + x_1 x_3 + x_2 x_3$$