INTRODUCTION

The S6B0107 (TQFP type: S6B2107) is an LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the S6B0108 (64 channel segment driver – TQFP type: S6B2108). The S6B0107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the S6B0108 (64 channel segment driver).
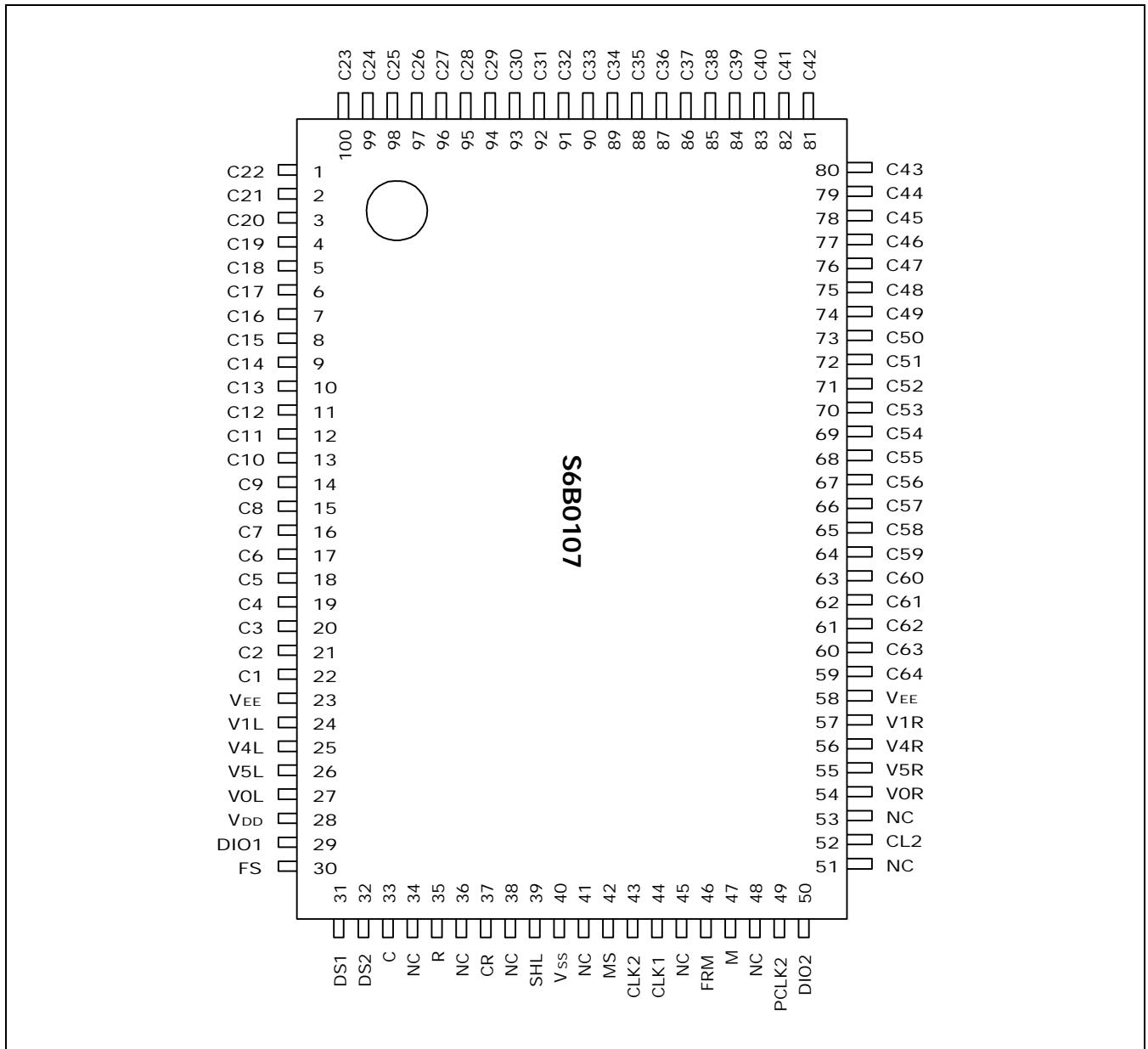
FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: + 5V ± 10%
- LCD driving voltage: 8V - 17V (V_{DD}-V_{EE})
- Interface
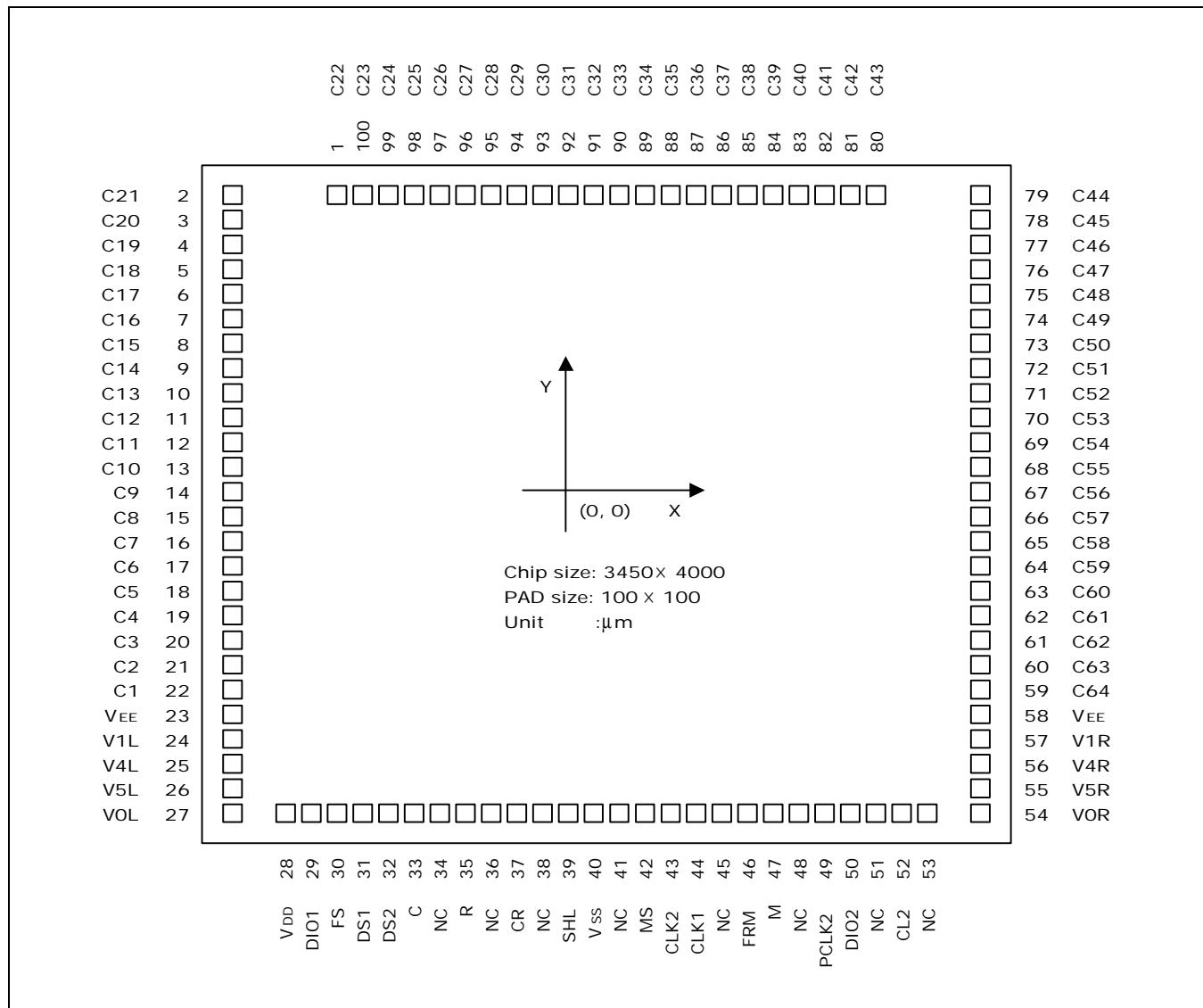
Driver		Controller
COMMON	SEGMENT	
Other S6B0107	S6B0108	MPU

- High voltage CMOS process
- 100QFP / 100TQFP or bare chip available

BLOCK DIAGRAM

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PIN CONFIGURATION

100 QFP

Top pins (100 → 81): C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42

Left pins (1 → 30):

Pin	Signal
1	C22
2	C21
3	C20
4	C19
5	C18
6	C17
7	C16
8	C15
9	C14
10	C13
11	C12
12	C11
13	C10
14	C9
15	C8
16	C7
17	C6
18	C5
19	C4
20	C3
21	C2
22	C1
23	V_{EE}
24	V1L
25	V4L
26	V5L
27	V0L
28	V_{DD}
29	DIO1
30	FS

Bottom pins (31 → 50): DS1, DS2, C, NC, R, NC, CR, NC, SHL, V_{SS}, NC, MS, CLK2, CLK1, NC, FRM, M, NC, PCLK2, DIO2

Right pins (80 → 51):

Pin	Signal
80	C43
79	C44
78	C45
77	C46
76	C47
75	C48
74	C49
73	C50
72	C51
71	C52
70	C53
69	C54
68	C55
67	C56
66	C57
65	C58
64	C59
63	C60
62	C61
61	C62
60	C63
59	C64
58	V_{EE}
57	V1R
56	V4R
55	V5R
54	V0R
53	NC
52	CL2
51	NC

S6B0107

PAD DIAGRAM (CHIP LAYOUT FOR THE 100QFP)

Top pads (left to right): C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43

Top pin numbers: 1 100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80

Left side pads:

Signal	Pin
C21	2
C20	3
C19	4
C18	5
C17	6
C16	7
C15	8
C14	9
C13	10
C12	11
C11	12
C10	13
C9	14
C8	15
C7	16
C6	17
C5	18
C4	19
C3	20
C2	21
C1	22
V_{EE}	23
V1L	24
V4L	25
V5L	26
VOL	27

Right side pads:

Pin	Signal
79	C44
78	C45
77	C46
76	C47
75	C48
74	C49
73	C50
72	C51
71	C52
70	C53
69	C54
68	C55
67	C56
66	C57
65	C58
64	C59
63	C60
62	C61
61	C62
60	C63
59	C64
58	V_{EE}
57	V1R
56	V4R
55	V5R
54	VOR

Y
(O, O)   X

Chip size: 3450 × 4000
PAD size: 100 × 100
Unit   : μm

Bottom pin numbers: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53

Bottom pads: V_{DD} DIO1 FS DS1 DS2 C NC R NC CR NC SHL V_{SS} NC MS CLK2 CLK1 NC FRM M NC PCLK2 DIO2 NC CL2 NC

There is the mark S6B0107 on the center of the chip.

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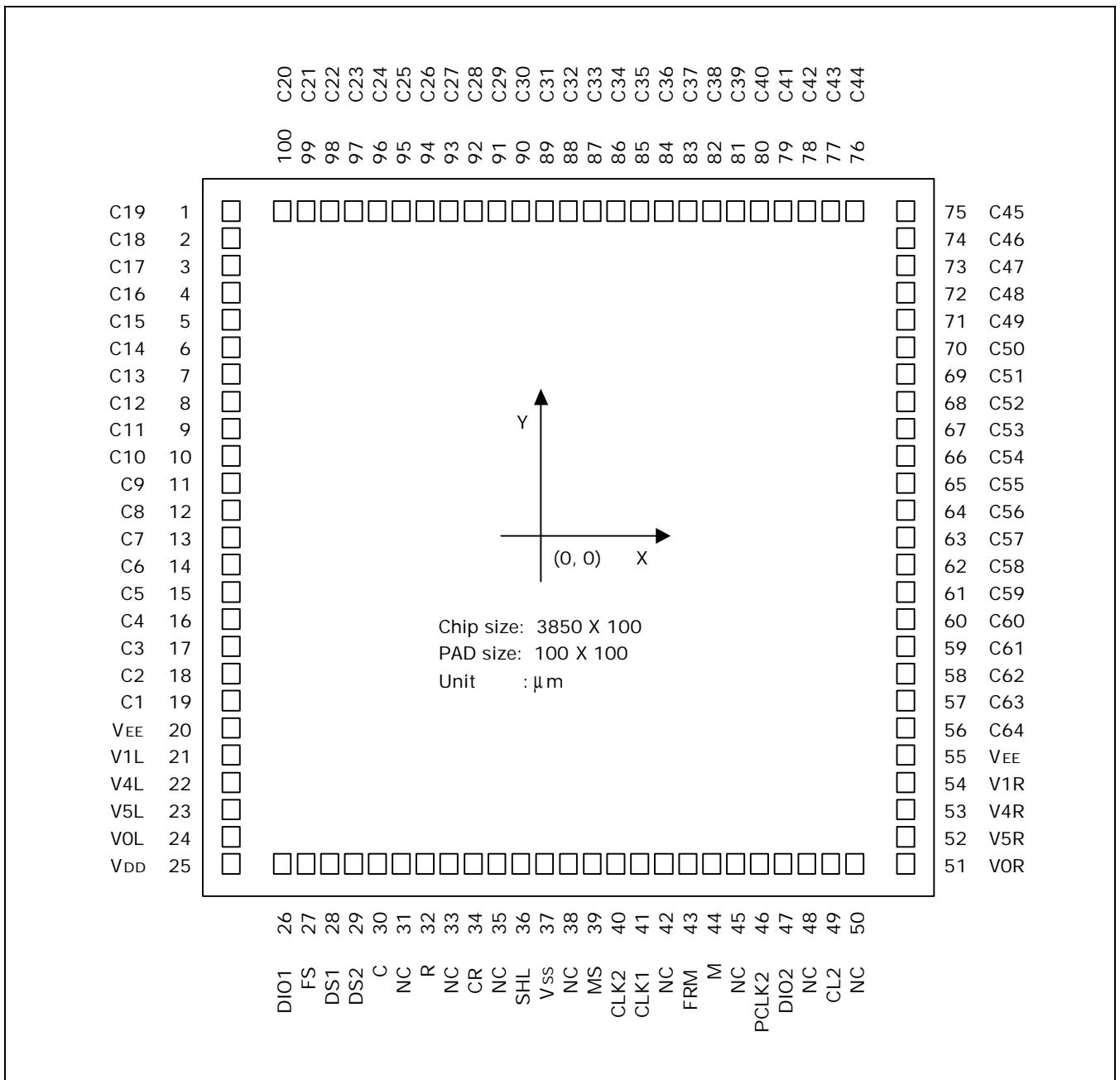
PAD CENTER COORDINATES (100QFP)

Pad Number	Pad Name	Coordinate		Pad Number	Pad Name	Coordinate		Pad Number	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	C22	-1314.5	1775.4	32	DS2	-677.6	-1775	71	C52	1500.9	630
2	C21	-1499.9	1630	34	C	-527.6	-1775	72	C51	1500.9	755
3	C20	-1499.9	1505	35	R	-377.6	-1775	73	C50	1500.9	880
4	C19	-1499.9	1380	37	CR	-227.6	-1775	74	C49	1500.9	1005
5	C18	-1499.9	1255	39	SHL	-77.6	-1775	75	C48	1500.9	1130
6	C17	-1499.9	1130	40	VSS	113.8	-1775	76	C47	1500.9	1255
7	C16	-1499.9	1005	42	MS	308.7	-1775	77	C46	1500.9	1380
8	C15	-1499.9	880	43	CLK2	458.7	-1775	78	C45	1500.9	1505
9	C14	-1499.9	755	44	CLK1	608.7	-1775	79	C44	1500.9	1630
10	C13	-1499.9	630	46	FRM	758.7	-1775	80	C43	1310.5	1775.4
11	C12	-1499.9	505	47	M	908.7	-1775	81	C42	1185.5	1775.4
12	C11	-1499.9	380	49	PCLK2	1058.7	-1775	82	C41	1060.5	1775.4
13	C10	-1499.9	255	50	DIO2	1208.7	-1775	83	C40	935.5	1775.4
14	C9	-1499.9	130	52	CL2	1358.7	-1775	84	C39	810.5	1775.4
15	C8	-1499.9	5	54	V0R	1500.9	-1495	85	C38	685.5	1775.4
16	C7	-1499.9	-120	55	V5R	1500.9	-1370	86	C37	560.5	1775.4
17	C6	-1499.9	-245	56	V4R	1500.9	-1245	87	C36	435.5	1775.4
18	C5	-1499.9	-370	57	V1R	1500.9	-1120	88	C35	310.5	1775.4
19	C4	-1499.9	-495	58	VEE	1500.9	-995	89	C34	185.5	1775.4
20	C3	-1499.9	-620	59	C64	1500.9	-870	90	C33	60.5	1775.4
21	C2	-1499.9	-745	60	C63	1500.9	-745	91	C32	-64.5	1775.4
22	C1	-1499.9	-870	61	C62	1500.9	-620	92	C31	-189.5	1775.4
23	VEE	-1499.9	-995	62	C61	1500.9	-495	93	C30	-314.5	1775.4
24	V1L	-1499.9	-1120	63	C60	1500.9	-370	94	C29	-439.5	1775.4
25	V4L	-1499.9	-1245	64	C59	1500.9	-245	95	C28	-564.5	1775.4
26	V5L	-1499.9	-1370	65	C58	1500.9	-120	96	C27	-689.5	1775.4
27	V0L	-1499.9	-1495	66	C57	1500.9	5	97	C26	-814.5	1775.4
28	VDD	-1345.6	-1775	67	C56	1500.9	130	98	C25	-939.5	1775.4
29	DIO1	-1127.6	-1775	68	C55	1500.9	255	99	C24	-1064.5	1775.4
30	FS	-977.6	-1775	69	C54	1500.9	380	100	C23	-1189.5	1775.4
31	DS1	-827.6	-1775	70	C53	1500.9	505				

100 TQFP (S6B2107)

Top pins (left to right): C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 V$_{EE}$ V1R V4R V5R V0R

Top pin numbers: 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51

Left side pins:
Pin	Number
C44	76
C43	77
C42	78
C41	79
C40	80
C39	81
C38	82
C37	83
C36	84
C35	85
C34	86
C33	87
C32	88
C31	89
C30	90
C29	91
C28	92
C27	93
C26	94
C25	95
C24	96
C23	97
C22	98
C21	99
C20	100

S6B2107

(100 TQFP)

Right side pins:
Number	Pin
50	NC
49	CL2
48	NC
47	DIO2
46	PCLK2
45	NC
44	M
43	FRM
42	NC
41	CLK1
40	CLK2
39	MS
38	NC
37	VSS
36	SHL
35	NC
34	CR
33	NC
32	R
31	NC
30	C
29	DS2
28	DS1
27	FS
26	DIO1

Bottom pin numbers: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

Bottom pins (left to right): C19 C18 C17 C16 C15 C14 C13 C12 C11 C10 C9 C8 C7 C6 C5 C4 C3 C2 C1 V$_{EE}$ V1L V4L V5L V0L V$_{DD}$

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PAD DIAGRAM (CHIP LAYOUT FOR THE 100-TQFP)

Chip size: 3850 X 100
PAD size: 100 X 100
Unit : μm

There is the mark S6B2107 on the center of the chip.

PAD CENTER COORDINATES (100-TQFP)
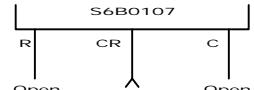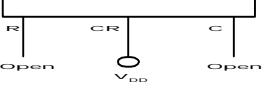
Pad Number	Pad Name	Coordinate		Pad Number	Pad Name	Coordinate		Pad Number	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	C19	-1697	1534	35	NC			69	C51	1697	784
2	C18	-1697	1409	36	SHL	-195	-1821	70	C50	1697	909
3	C17	-1697	1284	37	VSS	0	-1821	71	C49	1697	1034
4	C16	-1697	1159	38	NC			72	C48	1697	1159
5	C15	-1697	1034	39	MS	195	-1821	73	C47	1697	1284
6	C14	-1697	909	40	CLK2	345	-1821	74	C46	1697	1409
7	C13	-1697	784	41	CLK1	495	-1821	75	C45	1697	1534
8	C12	-1697	659	42	NC			76	C44	1500	1822
9	C11	-1697	534	43	FRM	645	-1821	77	C43	1375	1822
10	C10	-1697	409	44	M	795	-1821	78	C42	1250	1822
11	C9	-1697	284	45	NC			79	C41	1125	1822
12	C8	-1697	159	46	PCLK2	945	-1821	80	C40	1000	1822
13	C7	-1697	34	47	DIO2	1095	-1821	81	C39	875	1822
14	C6	-1697	-91	48	NC			82	C38	750	1822
15	C5	-1697	-216	49	CL2	1245	-1821	83	C37	625	1822
16	C4	-1697	-341	50	NC			84	C36	500	1822
17	C3	-1697	-466	51	V0R	1697	-1466	85	C35	375	1822
18	C2	-1697	-591	52	V5R	1697	-1341	86	C34	250	1822
19	C1	-1697	-716	53	V4R	1697	-1216	87	C33	125	1822
20	VEE	-1697	-841	54	V1R	1697	-1091	88	C32	0	1822
21	V1L	-1697	-966	55	VEE	1697	-966	89	C31	-125	1822
22	V4L	-1697	-1091	56	C64	1697	-841	90	C30	-250	1822
23	V5L	-1697	-1216	57	C63	1697	-716	91	C29	-375	1822
24	V0L	-1697	-1341	58	C62	1697	-591	92	C28	-500	1822
25	VDD	-1697	-1466	59	C61	1697	466	93	C27	-625	1822
26	DIO1	-1245	-1821	60	C60	1697	-341	94	C26	-750	1822
27	FS	-1095	-1821	61	C59	1697	-216	95	C25	-875	1822
28	DS1	-945	-1821	62	C58	1697	-91	96	C24	-1000	1822
29	DS2	-795	-1821	63	C57	1697	34	97	C23	-1125	1822
30	C	-645	-1821	64	C56	1697	159	98	C22	-1250	1822
31	NC			65	C55	1697	284	99	C21	-1375	1822
32	R	-495	-1821	66	C54	1697	409	100	C20	-1500	1822
33	NC			67	C53	1697	534				
34	CR	-345	-1821	68	C52	1697	659				

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PIN DESCRIPTION

Table 1. Pin Description

Pin Number QFP (TQFP)	Symbol	I/O	Description
28(25) 40(37) 23(20), 58(55)	V_{DD} V_{SS} V_{EE}	Power	For internal logic circuit (+5V ± 10%) GND (= 0 V) For LCD driver circuit
27(24), 54(51) 24(21), 57(54) 25(22), 56(53) 26(23), 55(52)	VOL, VOR V1L, V1R V4L, V4R V5L, V5R	Power	Bias supply voltage terminals to drive LCD. <table><tr><td>Slelect Level</td><td>Non-Select Level</td></tr><tr><td>VOL (R), V5L (R)</td><td>V1L (R), V4L (R)</td></tr></table> VOL and VOR (V1L & V1R, V4L & V4R, V5L & V5R) should be connected by the same voltage.
42(39)	MS	Input	Selection of master/slave mode - Master mode (MS = 1) DIO1, DIO2, CL2 and M is output state. - Slave mode (MS = 0) SHL = 1 → DIO1 is input state (DIO2 is output state) SHL = 0 → DIO2 is input state (DIO1 is output state) CL2 and M are input state.
39(36)	SHL	Input	Selection of data shift direction. <table><tr><td>SHL</td><td>Data Shift Direction</td></tr><tr><td>H</td><td>DIO1 → C1 ...... C64 → DIO2</td></tr><tr><td>L</td><td>DIO2 → C64 ...... C1 → DIO1</td></tr></table>
49(46)	PCLK2	Input	Selection of shift clock (CL2) phase. <table><tr><td>PCLK2</td><td>Shift Clock (CL2) Phase</td></tr><tr><td>H</td><td>Data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>Data shift at the falling edge of CL2</td></tr></table>
30(27)	FS	Input	Selection of oscillation frequency. - Master mode When the frame frequency is 70 Hz, the oscillation frequency should be fosc = 430kHz at FS = 1(V_{DD}) fosc = 215kHz at FS = 0(V_{SS}) - Slave mode Connect to V_{DD}.

Table 1. Pin Description (Continued)

Pin Number QFP (TQFP)	Symbol	I/O	Description
31(28) 32(29)	DS1 DS2	Input	Selection of display duty. - Master mode <table><tr><td>DS1</td><td>DS2</td><td>Duty</td></tr><tr><td>L</td><td>L</td><td>1/48</td></tr><tr><td>L</td><td>H</td><td>1/64</td></tr><tr><td>H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>H</td><td>1/128</td></tr></table> - Slave mode Connect to V_{DD}
33(30) 35(32) 37(34)	C R CR		RC Oscillator - Master mode: Use these terminals as shown below. - Slave mode: Stop the oscillator as shown below.
44(41) 43(40)	CLK1 CLK2	Output	Operating clock output for the S6B0108 - Master mode: connection to CLK1 and CLK2 of the S6B0108 - Slave mode: open
46(43)	FRM	Output	Synchronous frame signal. - Master mode: connection to FRM of the S6B0108 - Slave mode: open
47(44)	M	Input/ Output	Alternating signal input for LCD driving. - Master mode: output state Connection to M of the S6B0108 - Slave mode: input state Connection to the controller
52(49)	CL2	Input / Output	Data shift clock - Master mode: output state Connection to CL of the S6B0108 - Slave mode: input state Connection to shift clock terminal of the controller.

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29(26) 50(47)	DIO1 DIO2	Input/ Output	Data input/output pin of internal shift register.			
			MS	DS2	DIO1	DIO2
			H	H	Output	Output
				L	Output	Output
			L	H	Input	Output
				L	Output	Input

Table 1. Pin Description (Continued)

Pin Number QFP (TQFP)	Symbol	I/O	Description
22-1(19-1) 100-59(100-56)	C1-C64	Output	Common signal output for LCD driving.
34(31), 36(33) 38(35), 41(38) 45(42), 48(45) 51(48), 53(50)	NC		No connection

For the C1-C64 row, the Description contains the following sub-table:

Data	M	Out
L	L	V_1
L	H	V_4
H	L	V_5
H	H	V_0

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	V_{DD}-19.0 to V_{DD}+0.3	V	(4)
Driver supply voltage	V_B	-0.3 to V_{DD}+0.3	V	(1), (2)
	V_{LCD}	V_{EE}-0.3 to V_{DD}+0.3	V	(3), (4)
Operating temperature	T_{OPR}	-30 to +85	°C	-
Storage temperature	T_{STG}	-55 to +125	°C	-

NOTES:

1. Based on V_{SS} = 0V

2. Applies to input terminals and I/O terminals at high impedance. (Except V0L(R), V1L(R), V4L(R) and V5L(R))

3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).

4. Voltage level: $V_{DD} \geq$ V0L = V0R $\geq$ V1L = V1R $\geq$ V4L = V4R $\geq$ V5L = V5R $\geq V_{EE}$.

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ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD} = +5V ± 10%, V_{SS} = 0V, $|V_{DD}\text{-}V_{EE}|$ =8 - 17V, TA = -30 - +85°C)
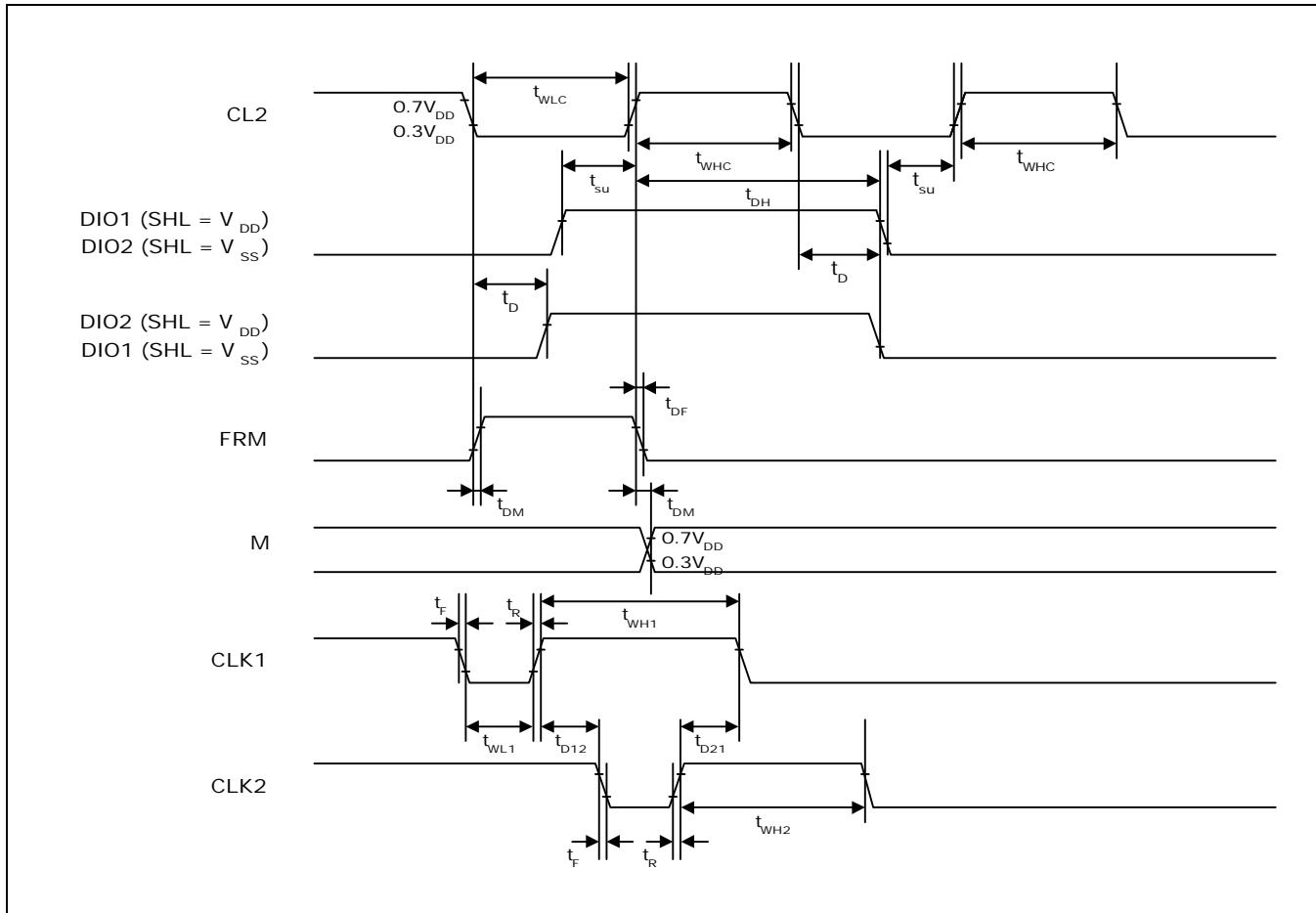
| Characteristic		Symbol	Condition	Min	Typ	Max	Unit	Note
Input Voltage	High	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V	(1)
	Low	V_{IL}		V_{SS}	-	$0.3V_{DD}$		
Output voltage	High	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-	-	V	(2)
	Low	V_{OL}	I_{OL} = 0.4mA	-	-	0.4		
Input leakage current		I_{LKG}	V_{IN} = V_{DD}-V_{SS}	-1.0	-	1.0	µA	(1)
OSC frequency		f_{OSC}	Rf = 47kΩ ± 2% Cf = 20pf ± 5%	315	450	585	kHz	
On resistance (VDIV-Ci)		R_{ON}	V_{DD}-V_{EE} = 17V Load current = ± 150µA	-	-	1.5	KΩ	
Operating current		I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	(3)
		I_{DD2}	Slave mode 1/128 Duty	-	-	200	µA	(4)
Supply current		I_{EE}	Master mode 1/128 Duty	-	-	100		(5)
Operating		f_{op1}	Master mode External clock	50	-	600	kHz	
Frequency		f_{op2}	Slave mode	0.5	-	1500		

NOTES:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the
   input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
3. This value is specified at about the current flowing through V_{SS}. Internal oscillation circuit: Rf = 47kΩ, Cf = 20pF. Each
   terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about the current flowing through V_{SS}. Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is
   connected to V_{DD}, and MS is connected to V_{SS}. CL2, M, DIO1 is external clock.
5. This value is specified at about the current flowing through V_{EE}. Don't connect to V_{LCD} (V1-V5).
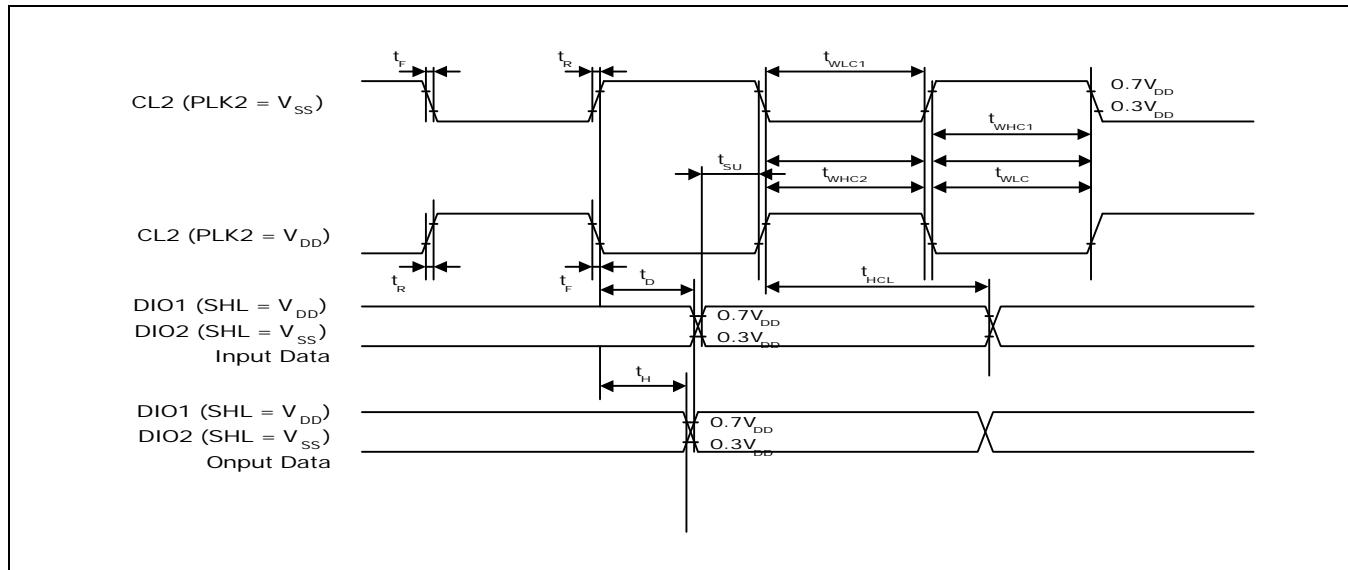
AC CHARACTERISTICS (V_{DD} = 5V $\pm$ 10%, TA = -30°C - +85°C)

Master Mode (MS = V_{DD}, PCLK2 = V_{DD}, Cf = 20pF, Rf = 47kΩ)

CL2

$0.7V_{DD}$
$0.3V_{DD}$

t_{WLC}

t_{WHC}

t_{WHC}

t_{su}

t_{su}

t_{DH}

DIO1 (SHL = V_{DD})
DIO2 (SHL = V_{SS})

t_D

t_D

DIO2 (SHL = V_{DD})
DIO1 (SHL = V_{SS})

t_{DF}

FRM

t_{DM}

t_{DM}

M

$0.7V_{DD}$
$0.3V_{DD}$

t_F

t_R

t_{WH1}

CLK1

t_{WL1}

t_{D12}

t_{D21}

CLK2

t_F

t_R

t_{WH2}

14
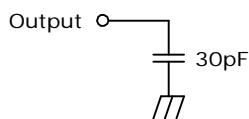
Master Mode

Characteristic	Symbol	Min	Typ	Max	Unit
Data setup time	^{t}SU	20	-	-	μs
Data hold time	^{t}DH	40	-	-	
Data delay time	^{t}D	5	-	-	
FRM delay time	^{t}DF	-2	-	2	
M delay time	^{t}DM	-2	-	2	
CL2 low level width	^{t}WLC	35	-	-	
CL2 high level width	^{t}WHC	35	-	-	
CLK1 low level width	^{t}WL1	700	-	-	ns
CLK2 low level width	^{t}WL2	700	-	-	
CLK1 high level width	^{t}WH1	2100	-	-	
CLK2 high level width	^{t}WH2	2100	-	-	
CLK1-CLK2 phase difference	^{t}D12	700	-	-	
CLK2-CLK1 phase difference	^{t}D21	700	-	-	
CLK1, CLK2 rise/fall time	^{t}R/^{t}F	-	-	150	

Slave Mode (MS = V$_{SS}$)

Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width	t$_{WLC1}$	450	-	-	ns	PCLK2 = V$_{SS}$
CL2 high level width	t$_{WHC1}$	150	-	-	ns	PCLK2 = V$_{SS}$
CL2 low level width	t$_{WLC2}$	150	-	-	ns	PCLK2 = V$_{DD}$
CL2 high level width	t$_{WHL}$	450	-	-	ns	PCLK2 = V$_{DD}$
Data setup time	t$_{SU}$	100	-	-	ns	
Data hold time	t$_{DH}$	100	-	-	ns	
Data delay time	t$_{D}$	-	-	200	ns	(NOTE)
Output data hold time	t$_{H}$	10	-	-	ns	
CL2 rise/fall time	t$_{R}$/t$_{F}$	-	-	30	ns	

NOTE: Connect load CL = 30pF

Output o———
        |
       ═══ 30pF
        |
       /7/7

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FUNCTIONAL DESCRIPTION
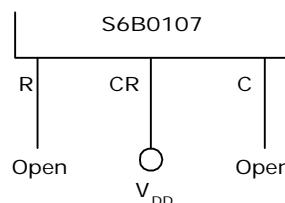
RC Oscillator

The RC Oscillator generates CL2, M, FRM of the S6B0107, and CLK1 and CLK2 of the S6B0108 by the oscillation resister R and capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.

Internal Oscillation   External Clock

Slave Mode: In the slave mode, stop the oscillator as shown below.

Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode
- When M/S is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.
- When M/S is "L", it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)
To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	f_{OSC} = 430kHz
L	f_{OSC} = 215kHz

In the slave mode, it is connected to V_{DD}.

Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	DUTY
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

Phase Selection

It is a circuit to shift data on synchronization or rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

Data Shift Direction Selection

When M/S is connected to V_{DD}, DIO1 and DIO2 terminal is only output.
When M/S is connected to V_{SS}, it depends on the SHL.
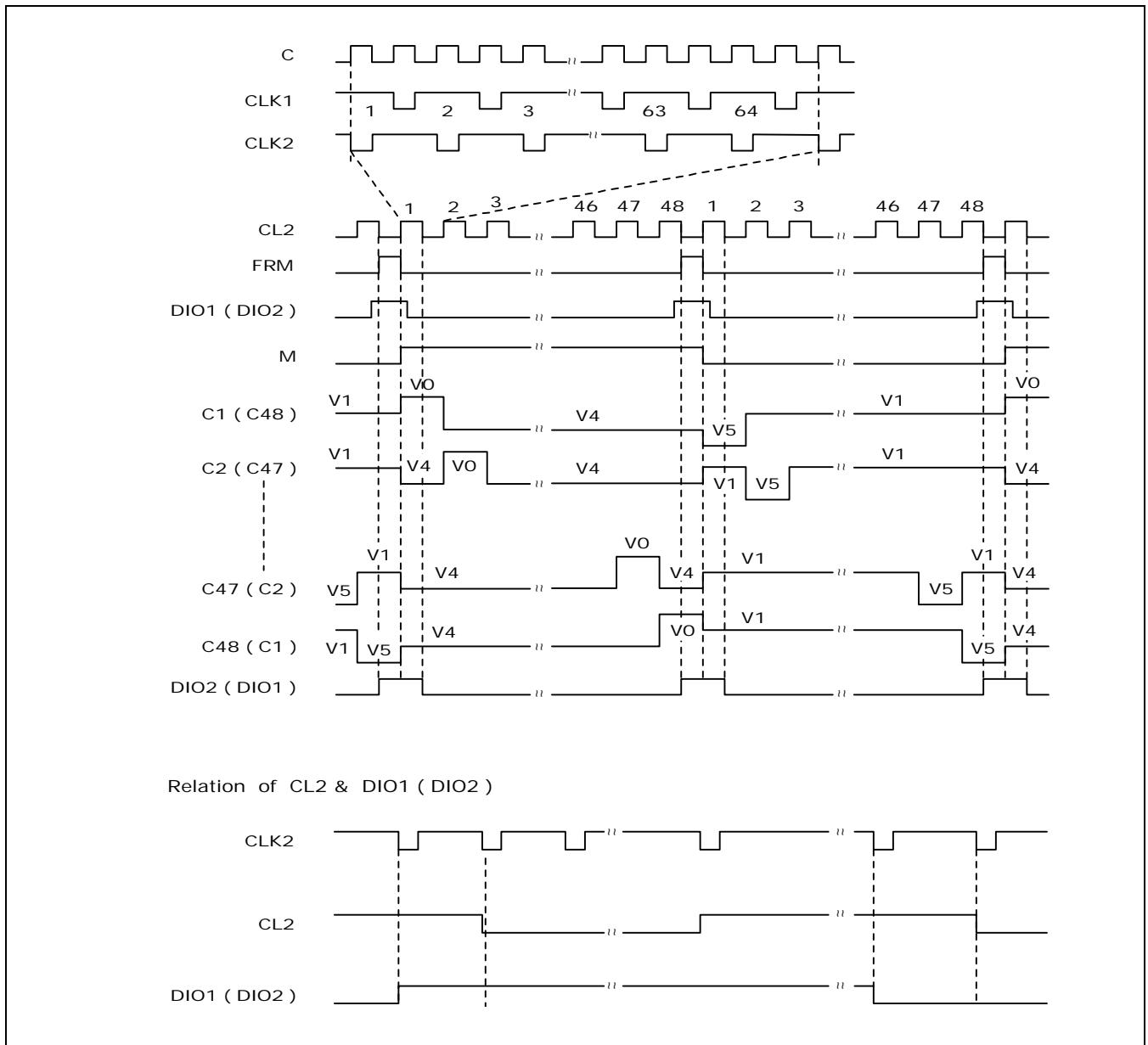
| MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 $\rightarrow$ C64
	L	Output	Output	C64 $\rightarrow$ C1
L	H	Input	Output	DIO1 $\rightarrow$ C1 $\rightarrow$ C64 $\rightarrow$ DIO2
	L	Output	Input	DIO2 $\rightarrow$ C64 $\rightarrow$ C1 $\rightarrow$ DIO1

TIMING DIAGRAM
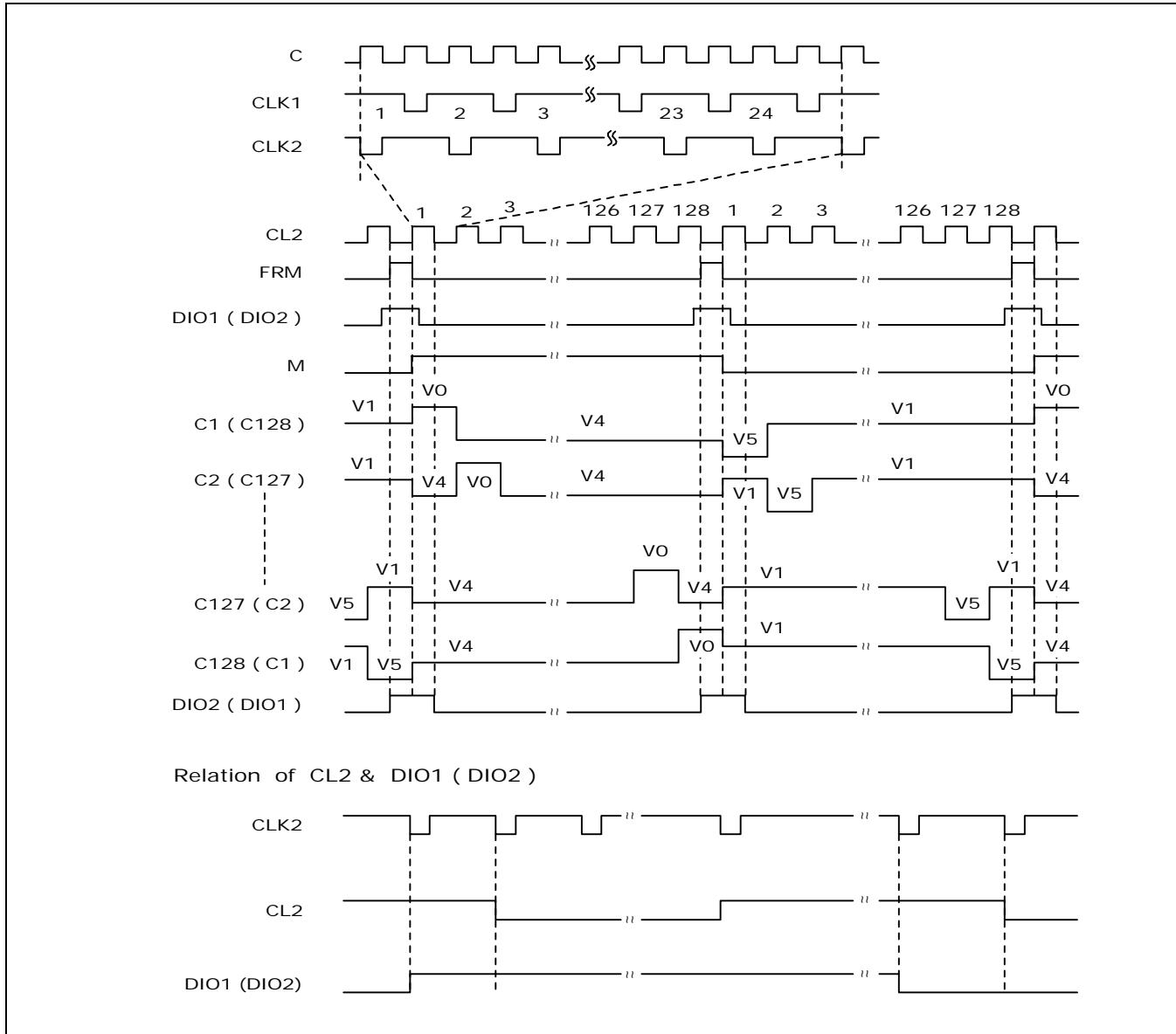
1/48 DUTY TIMING (MASTER MODE)

Condition: DS1 = L, DS2 = L, SHL = H(L), PCLK2 = H
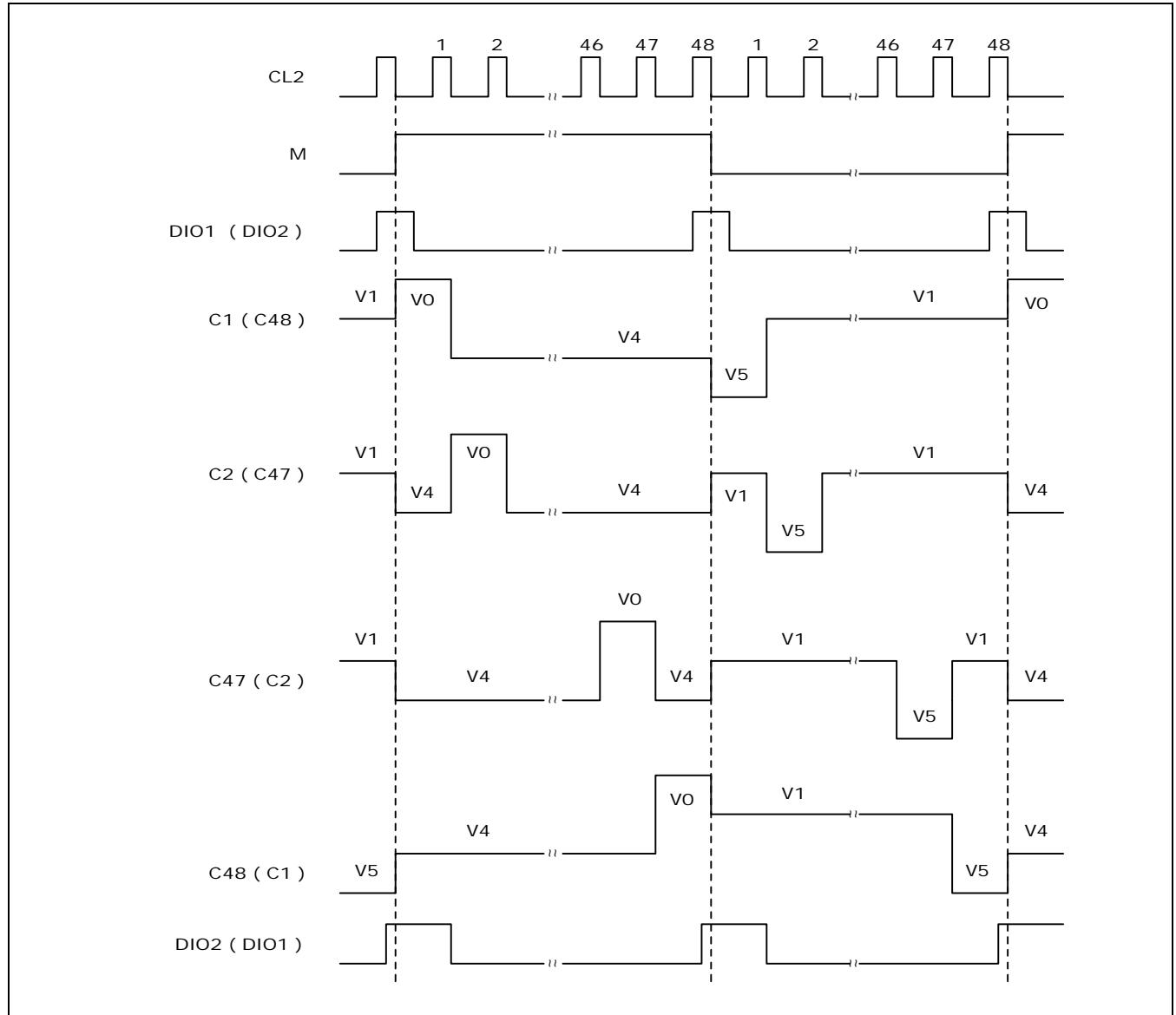
1/128 DUTY TIMING (MASTER MODE)

Condition: DS1 = H, DS2 = H, SHL = H(L), PCLK2 = H
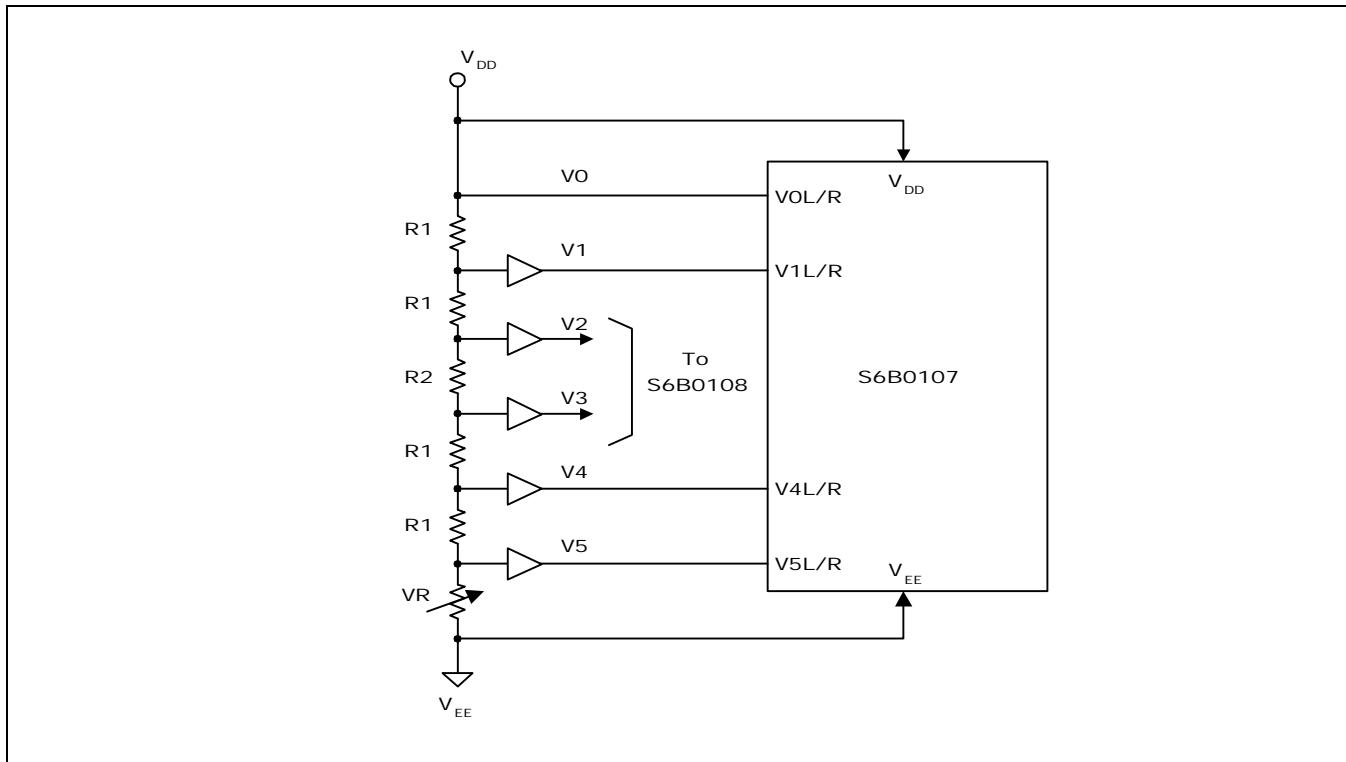
1/48 DUTY TIMING (SLAVE MODE)

Condition: PCLK2 = L, SHL = H(L)

POWER DRIVER CIRCUIT

Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2 = 4R1
1/64	1/9	R2 = 5R1
1/96	1/11	R2 = 7R1
1/128	1/12	R2 = 8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.

$R1/(4R1 + R2) = 1/8$

$R1 + 3k\Omega$, $R2 = 12k\Omega$

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APPLICATION CIRCUIT

1/128 duty Segment driver (S6B0108) interface circuit