Github url: https://github.com/Almo-o/Computer-Organization-and-Assembly/tree/main

1. Q = 0, Q' = 1

2. Characteristics of each flip flop

SR flip flop:
Inputs: S (set) and R (reset)
Outputs: Q (current state) and Q' (complement Q)

Characteristic Table:

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

D flip flop:
Single input D
Outputs: Q (current state) and Q' (complement Q)

Characteristic Table:

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

JK flip flop:
Inputs: J and K

Outputs: Q (current state) and Q’ (complement Q)

Characteristic Table:

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

T flip flop:
Single input T:
Outputs: Q (current state) and Q’ (complement Q)

Characteristic Table:

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

3. Excitation tables

Sr flip flop

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

D flip flop

Q(t)	Q(t+10	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip flop

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip flop

Q(t)	Q(t+10	T
0	0	0
0	1	1
1	0	1
1	1	0

4. 5 latches
5. 32 states

6.design a two-bit up/down counter using the input direction such that when direction = 0, the system decrements (00 -> 11 -> 10 -> 01 -> 00) and when direction = 1, the system increments (00 -> 01 -> 10 -> 11 -> 00)

State table

Current state (Q1,Q0)	Input (direction)	Next State
00	0	11
00	1	01
01	0	00
01	1	10
10	0	01
10	1	11
11	0	10
11	1	00

K-map
Q1’

	00	01	11	10
0	1	0	1	0
1	0	1	0	1

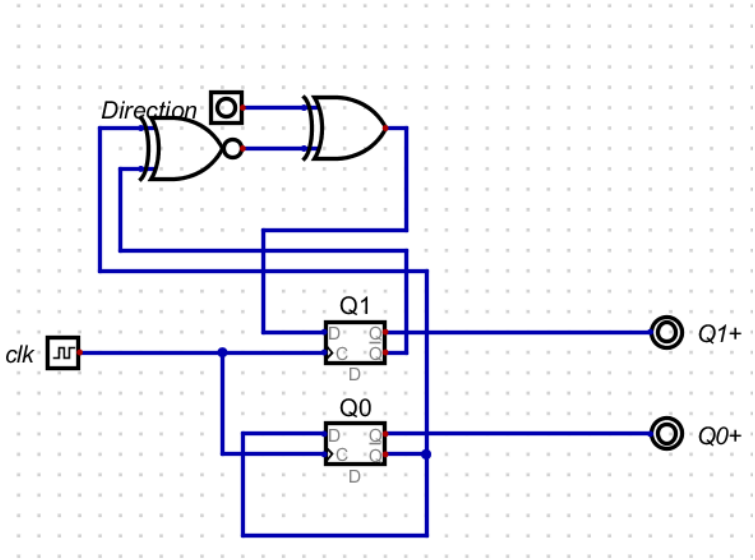
Boolean expression:
= (Q1 XNOR Q0) XOR Direction

K-map
Q0’

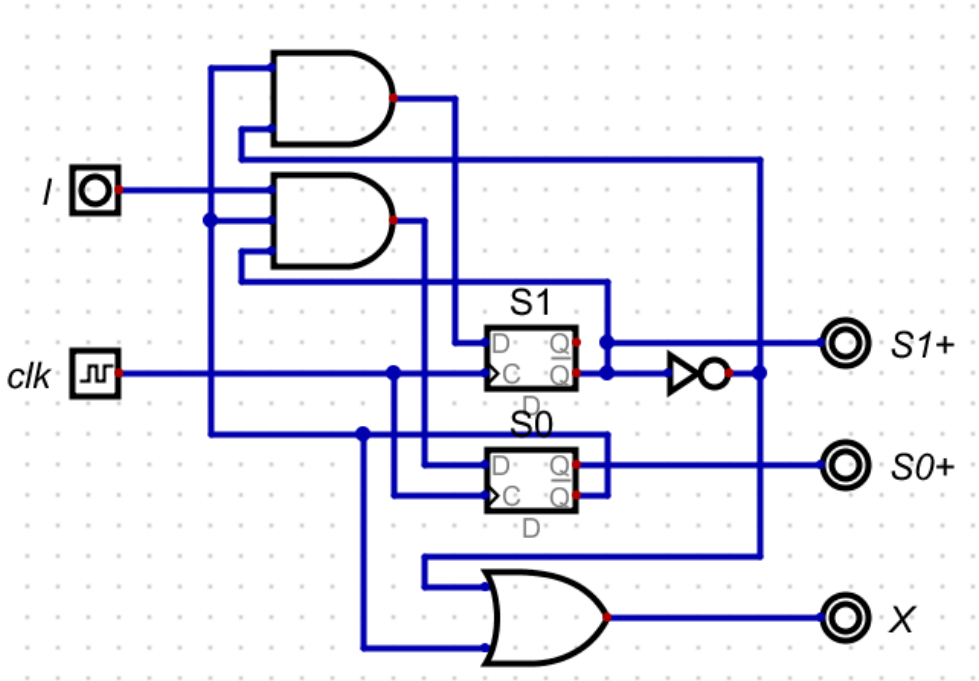
	00	01	11	10
0	1	0	0	1
1	1	0	0	1

Boolean expression : relies only on Q0 being 0
= -Q0

Circuit for Two-bit-up/down–counter



7. The three Boolean expressions below represent the next state bits, S1' and S0', and the output bit, X, based on the current state, S1 and S0, and the input I. Draw the logic circuit for the state machine including the latches and output circuitry. Label all signals.



8.

State Truth Table

Current state (S1,S0)	Input (direction)	Next State
00	0	01
00	1	10
01	0	11
01	1	10
10	0	11
10	1	00
11	0	10
11	1	01

Output table

Current State	Output
00	1
01	1
10	0
11	1

8.b)

Current state (S1,S0)	Input (direction)	Next State
00	0	01
00	1	00
01	0	01
01	1	10
10	0	00
10	1	01

Output table

Current State	Output
00	0
01	1
10	1

9. Design a state machine to detect the bit pattern "110" in a stream of bits