Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I^2C	USB	Packages
							Dedicated 16-Bit Timers	UART(1)/LIN/J2602	MCCP(4)	SCCP(3)	CLC	SPI(2)/I^2S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.

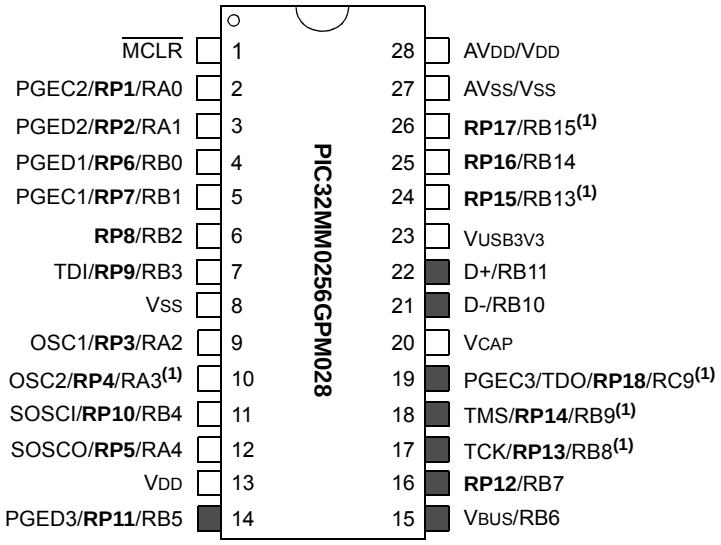
2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.

3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

Pin Diagrams

28-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

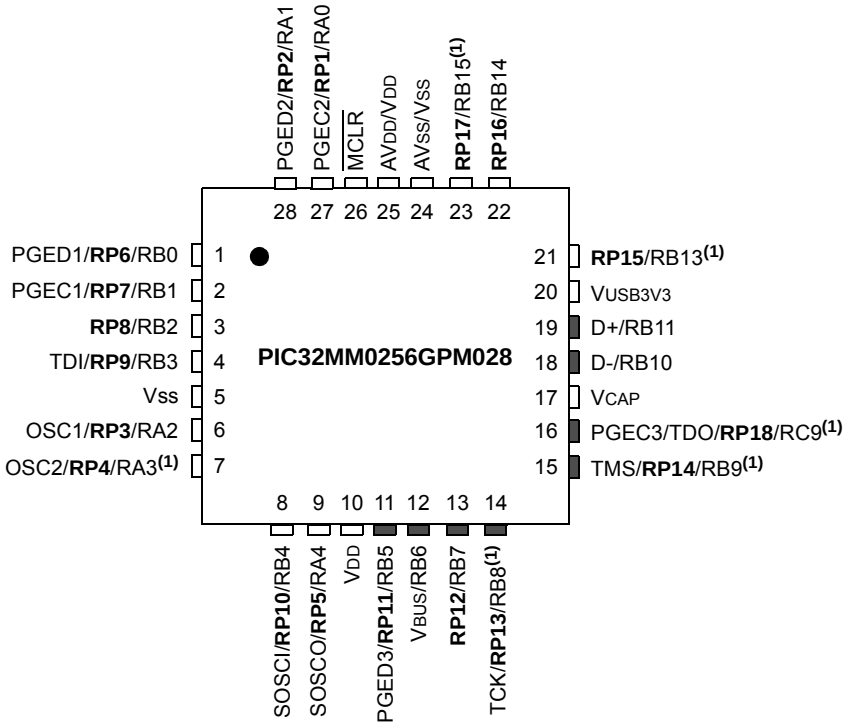
TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SSOP DEVICES

Pin	Function	Pin	Function
1	MCLR	15	VBUS/RB6
2	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0	16	**RP12**/SDA3/SDI3/OCM3F/RB7
3	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	17	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)
4	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	18	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
5	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	19	PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1)
6	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	20	VCAP
7	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	21	D-/RB10
8	VSS	22	D+/RB11
9	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	23	VUSB3V3
10	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	24	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1)
11	SOSCI/AN7/**RP10**/OCM3C/RB4	25	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	26	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
13	VDD	27	AVSS/VSS
14	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	28	AVDD/VDD

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

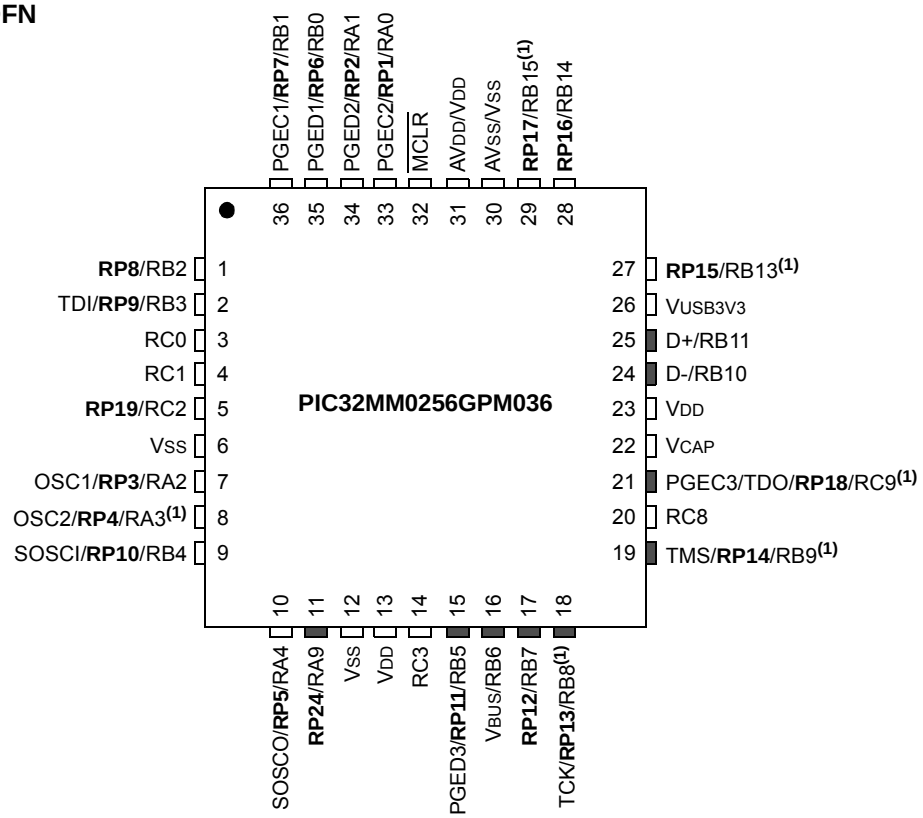
TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	15	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	16	PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1)
3	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	17	VCAP
4	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	18	D-/RB10
5	VSS	19	D+/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	VUSB3V3
7	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	21	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1)
8	SOSCI/AN7/**RP10**/OCM3C/RB4	22	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
9	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	23	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
10	VDD	24	AVSS/VSS
11	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	25	AVDD/VDD
12	VBUS/RB6	26	MCLR
13	**RP12**/SDA3/SDI3/OCM3F/RB7	27	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	28	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

36-Pin QFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

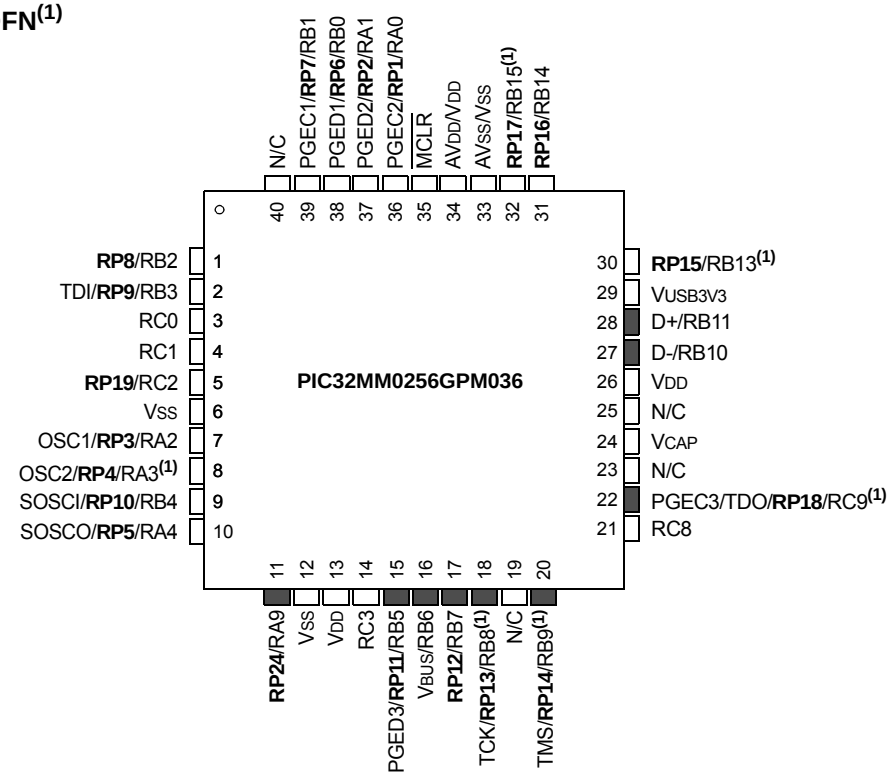
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN QFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	19	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	20	AN14/LVDIN/C2INC/RC8
3	AN12/C2IND/T2CK/T2G/RC0	21	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/SDO3/RC9(1)
4	AN13/T3CK/T3G/RC1	22	VCAP
5	**RP19**/OCM2A/RC2	23	VDD
6	VSS	24	D-/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	D+/RB11
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	26	VUSB3V3
9	SOSCI/AN7/**RP10**/OCM3C/RB4	27	AN8/**RP15**/SCL3/SCK3/RB13(1)
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	28	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
11	**RP24**/OCM3A/RA9	29	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
12	VSS	30	AVSS/VSS
13	VDD	31	AVDD/VDD
14	RC3	32	MCLR
15	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	33	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	VBUS/RB6	34	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP12**/SDA3/SDI3/OCM3F/RB7	35	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

40-Pin UQFN(1)



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

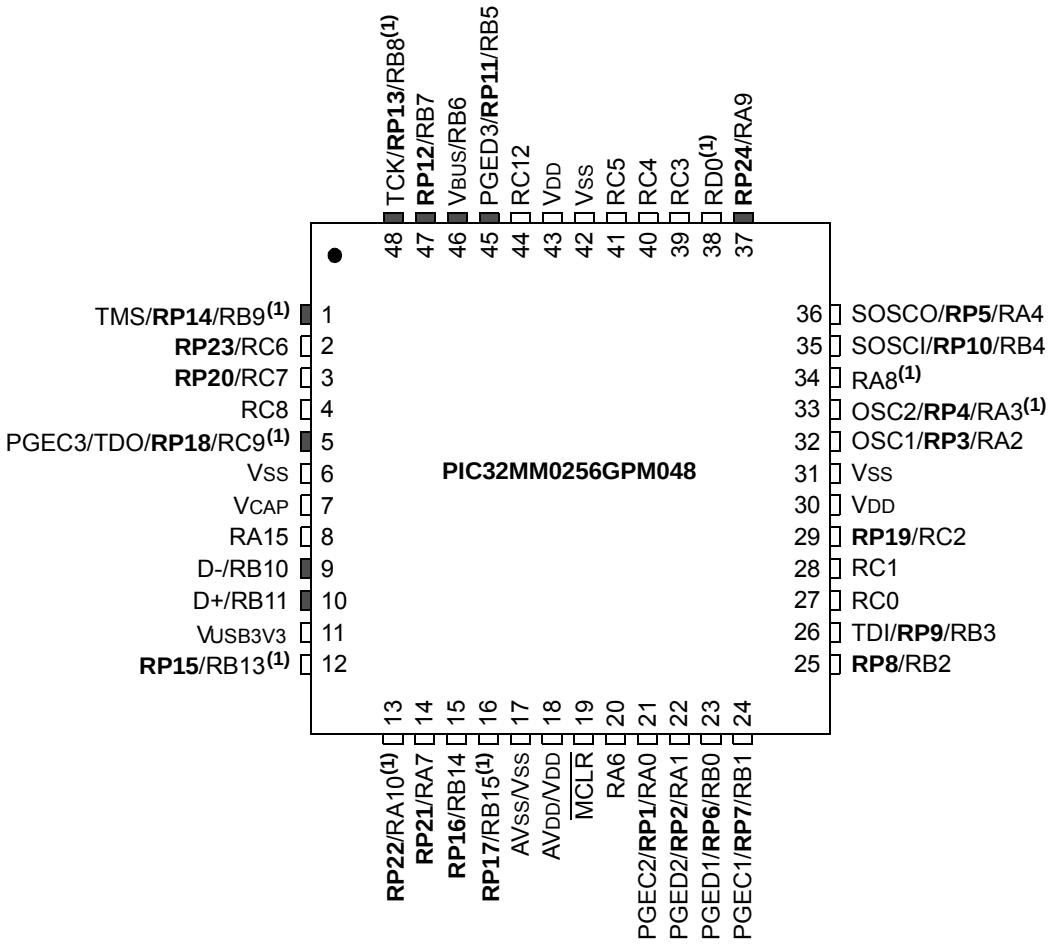
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	21	AN14/LVDIN/C2INC/RC8
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	22	PGEC3/TDO/**RP18**/ASCL1(2)/SDO3/USBOEN/RC9(1)
3	AN12/C2IND/T2CK/T2G/RC0	23	N/C
4	AN13/T3CK/T3G/RC1	24	VCAP
5	**RP19**/OCM2A/RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	D-/RB10
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	28	D+/RB11
9	SOSCI/AN7/**RP10**/OCM3C/RB4	29	VUSB3V3
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	30	AN8/**RP15**/SCL3/SCK3/RB13(1)
11	**RP24**/OCM3A/RA9	31	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	VSS	32	AN10/C3INA/REFCLKO/**RP17**/U1RX/$\overline{SS1}$/FSYNC1/OCM2B/INT0/RB15(1)
13	VDD	33	AVSS/VSS
14	RC3	34	AVDD/VDD
15	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{SS3}$/FSYNC3/OCM3E/RB5	35	$\overline{MCLR}$
16	VBUS/RB6	36	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP12**/SDA3/SDI3/OCM3F/RB7	37	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP13**/SCL1/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	38	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1
20	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/OCM1B/INT2/RB9(1)	40	N/C

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

48-Pin UQFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

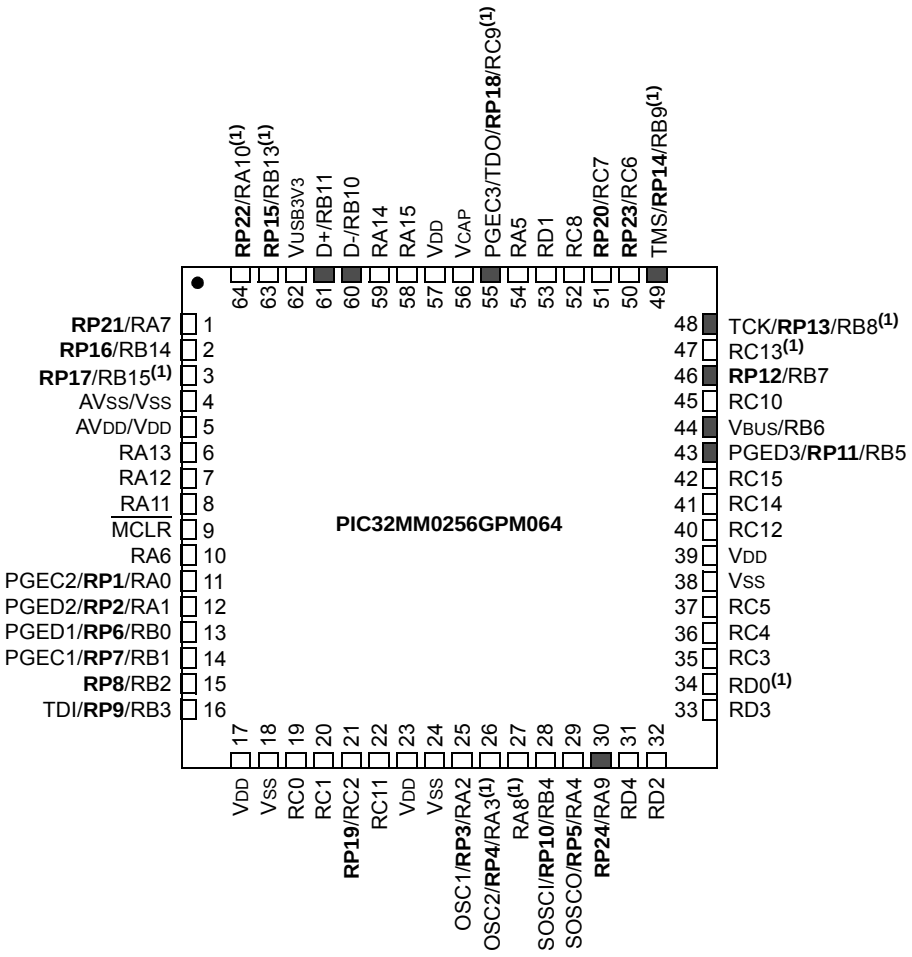
TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 48-PIN UQFN/TQFP DEVICES

Pin	Function	Pin	Function
1	TMS/**RP14**/SDA1/OCM1B/INT2/RB9(1)	25	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2
2	**RP23**/RC6	26	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3
3	**RP20**/RC7	27	AN12/C2IND/T2CK/T2G/RC0
4	AN14/LVDIN/C2INC/RC8	28	AN13/T3CK/T3G/RC1
5	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)	29	**RP19**/OCM2A/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	RTCC/RA15	32	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2
9	D-/RB10	33	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)
10	D+/RB11	34	SDO3/RA8(1)
11	VUSB3V3	35	SOSCI/AN7/**RP10**/OCM3C/RB4
12	AN8/**RP15**/SCL3/RB13(1)	36	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4
13	**RP22**/SCK3/RA10(1)	37	**RP24**/OCM3A/RA9
14	**RP21**/SDI3/RA7	38	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
15	CVREF/AN9/C3INB/**RP16**/VBUSON/SDI1/OCM3B/INT1/RB14	39	OCM2B/RC3
16	AN10/C3INA/REFCLKO/**RP17**/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)	40	OCM1E/INT3/RC4
17	AVSS/VSS	41	AN15/OCM1D/RC5
18	AVDD/VDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	AN19/U1RX/RA6	44	U1TX/RC12
21	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	45	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{\text{SS3}}$/FSYNC3/OCM3E/RB5
22	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	46	VBUS/RB6
23	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	47	**RP12**/SDA3/OCM3F/RB7
24	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	48	TCK/**RP13**/SCL1/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

64-Pin QFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN QFN/TQFP DEVICES

Pin	Function	Pin	Function
1	**RP21**/SDI3/RA7	33	OCM3B/RD3
2	CVREF/AN9/C3INB/**RP16**/VBUSON/RB14	34	REFCLKI/T1CK/T1G/U1RTS/U1BCLK/SDO1/RD0(1)
3	AN10/C3INA/REFCLKO/**RP17**/RB15(1)	35	OCM2B/RC3
4	AVSS	36	OCM1E/INT3/RC4
5	AVDD	37	AN15/OCM1D/RC5
6	AN16/U1CTS/RA13	38	VSS
7	AN17/OCM1A/RA12	39	VDD
8	AN18/RA11	40	U1TX/RC12
9	MCLR	41	OCM3D/RC14
10	AN19/U1RX/RA6	42	OCM3E/RC15
11	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	43	PGED3/**RP11**/ASDA1(2)/USBID/RB5
12	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	44	VBUS/RB6
13	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	45	OCM3F/RC10
14	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	46	**RP12**/SDA3/RB7
15	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	47	SCK1/RC13(1)
16	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	48	TCK/**RP13**/SCL1/RB8(1)
17	VDD	49	TMS/**RP14**/SDA1/INT2/RB9(1)
18	VSS	50	**RP23**/RC6
19	AN12/C2IND/T2CK/T2G/RC0	51	**RP20**/RC7
20	AN13/T3CK/T3G/RC1	52	AN14/LVDIN/C2INC/RC8
21	**RP19**/OCM2A/RC2	53	OCM1B/RD1
22	SS3/FSYNC3/RC11	54	OCM3A/RA5
23	VDD	55	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)
24	VSS	56	VCAP
25	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	57	VDD
26	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)	58	RTCC/RA15
27	SDO3/RA8(1)	59	OCM3C/RA14
28	SOSCI/AN7/**RP10**/RB4	60	D-/RB10
29	SOSCO/SCLKI/**RP5**/PWRLCLK/RA4	61	D+/RB11
30	**RP24**/RA9	62	VUSB3V3
31	SDI1/INT1/RD4	63	AN8/**RP15**/SCL3/RB13(1)
32	SS1/FSYNC1/INT0/RD2	64	**RP22**/SCK3/RA10(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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