Communication Interfaces

- Two UART modules (15 Mbps):
  - Supports LIN/J2602 protocols and IrDA®
- Two 4-Wire SPI modules (15 Mbps)
- Two I^2C modules (up to 1 Mbaud) with SMBus Support

Input/Output

- Constant-Current Source (10 µA nominal)
- Sink/Source up to 12mA/15mA, respectively; Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable, Open-Drain Pull-ups and Pull-Downs
- External Interrupts on All I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- The 6x6x0.5 mm UQFN Package is Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Five Program and Three Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

Device	Pins	Program Memory Bytes	RAM (Bytes)	General Purpose I/O (GPIO)	Remappable Peripherals								12-Bit ADC		PGA	Analog Comparator	DAC Output	Constant-Current Source	Packages
					Timers(1)	Input Capture	Output Compare	UART	SPI	PWM(2)	External Interrupts(3)	Reference Clock	I^2C	Analog Inputs	S&H Circuits					
dsPIC33EP16GS502	28	16K	2K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	SOIC, QFN-S, UQFN
dsPIC33EP32GS502	28	32K	4K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	
dsPIC33EP64GS502	28	64K	8K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	
dsPIC33EP16GS504	44	16K	2K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	QFN, TQFP
dsPIC33EP32GS504	44	32K	4K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP64GS504	44	64K	8K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP16GS505	48	16K	2K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	TQFP
dsPIC33EP32GS505	48	32K	4K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP64GS505	48	64K	8K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP16GS506	64	16K	2K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	TQFP
dsPIC33EP32GS506	64	32K	4K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	
dsPIC33EP64GS506	64	64K	8K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	

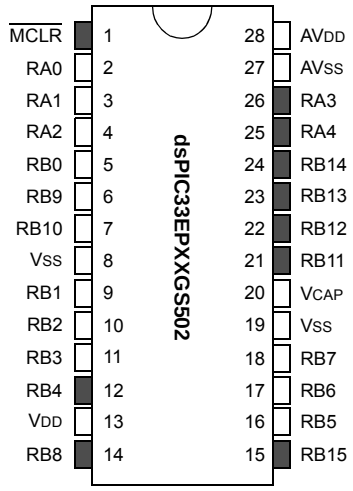
Note 1: The external clock for Timer1, Timer2 and Timer3 is remappable.

2: PWM4 and PWM5 are remappable on all devices except the 64-pin devices.

3: External interrupts, INT0 and INT4, are not remappable.

Pin Diagrams

28-Pin SOIC

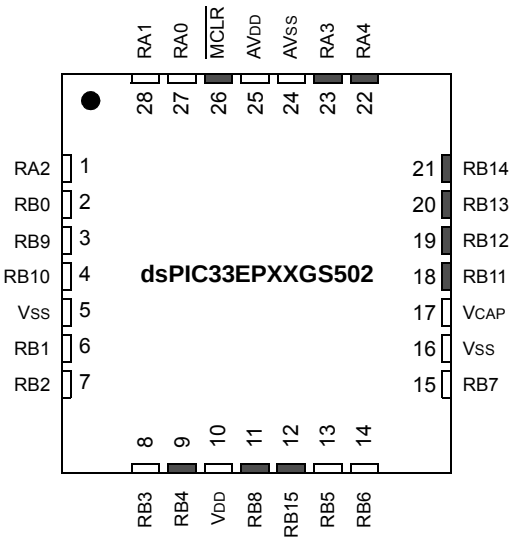


Pin	Pin Function	Pin	Pin Function
1	MCLR	15	PGEC3/SCL2/**RP47**/RB15
2	AN0/PGA1P1/CMP1A/RA0	16	TDO/AN19/PGA2N2/**RP37**/RB5
3	AN1/PGA1P2/PGA2P1/CMP1B/RA1	17	PGED1/TDI/AN20/SCL1/**RP38**/RB6
4	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	18	PGEC1/AN21/SDA1/**RP39**/RB7
5	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0	19	VSS
6	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9	20	VCAP
7	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10	21	TMS/PWM3H/**RP43**/RB11
8	Vss	22	TCK/PWM3L/**RP44**/RB12
9	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1	23	PWM2H/**RP45**/RB13
10	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2	24	PWM2L/**RP46**/RB14
11	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3	25	PWM1H/RA4
12	PGEC2/ADTRG31/EXTREF1/RP36/RB4	26	PWM1L/RA3
13	VDD	27	AVSS
14	PGED3/SDA2/FLT31/RP40/RB8	28	AVDD

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

Pin Diagrams (Continued)

28-Pin QFN-S, UQFN

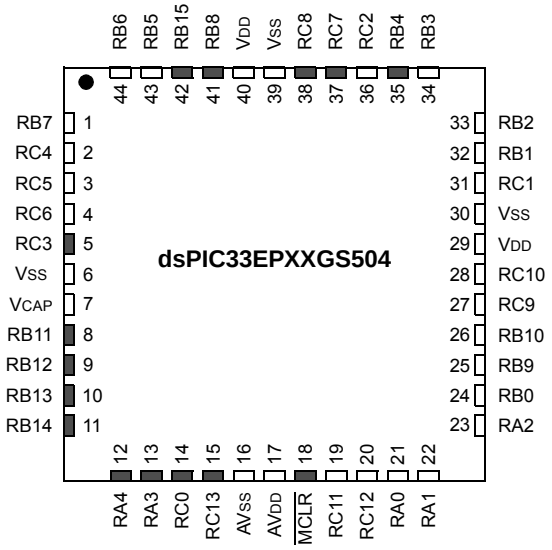


Pin	Pin Function	Pin	Pin Function
1	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	15	PGEC1/AN21/SDA1/**RP39**/RB7
2	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0	16	VSS
3	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9	17	VCAP
4	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10	18	TMS/PWM3H/**RP43**/RB11
5	Vss	19	TCK/PWM3L/**RP44**/RB12
6	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1	20	PWM2H/**RP45**/RB13
7	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2	21	PWM2L/**RP46**/RB14
8	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3	22	PWM1H/RA4
9	PGEC2/ADTRG31/EXTREF1/RP36/RB4	23	PWM1L/RA3
10	VDD	24	AVSS
11	PGED3/SDA2/FLT31/RP40/RB8	25	AVDD
12	PGEC3/SCL2/**RP47**/RB15	26	MCLR
13	TDO/AN19/PGA2N2/**RP37**/RB5	27	AN0/PGA1P1/CMP1A/RA0
14	PGED1/TDI/AN20/SCL1/**RP38**/RB6	28	AN1/PGA1P2/PGA2P1/CMP1B/RA1

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

Pin Diagrams (Continued)

44-Pin QFN

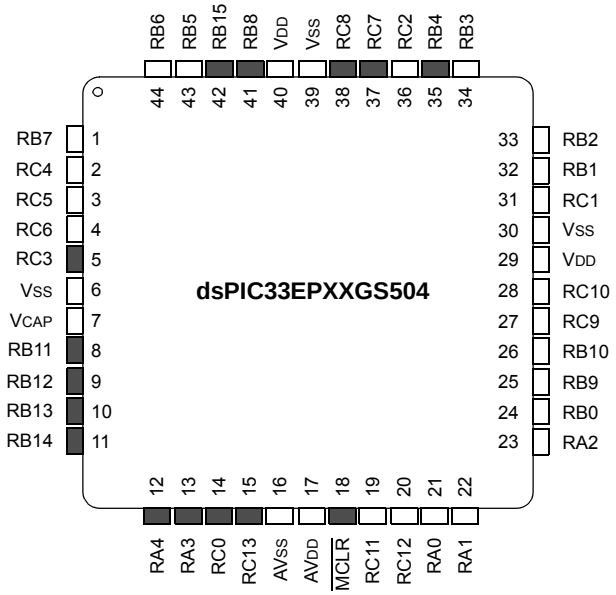


Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/**RP39**/RB7	23	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2
2	AN1ALT/**RP52**/RC4	24	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0
3	AN0ALT/**RP53**/RC5	25	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9
4	AN17/**RP54**/RC6	26	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10
5	**RP51**/RC3	27	AN11/PGA1N3/**RP57**/RC9
6	VSS	28	AN10/PGA1P4/EXTREF2/**RP58**/RC10
7	VCAP	29	VDD
8	TMS/PWM3H/**RP43**/RB11	30	VSS
9	TCK/PWM3L/**RP44**/RB12	31	AN8/PGA2P4/CMP4C/**RP49**/RC1
10	PWM2H/**RP45**/RB13	32	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1
11	PWM2L/**RP46**/RB14	33	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2
12	PWM1H/RA4	34	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3
13	PWM1L/RA3	35	PGEC2/ADTRG31/**RP36**/RB4
14	FLT12/**RP48**/RC0	36	AN9/CMP4D/EXTREF1/**RP50** /RC2
15	FLT11/**RP61**/RC13	37	ASDA1/**RP55**/RC7
16	AVSS	38	ASCL1/**RP56**/RC8
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	AN12/ISRC1/**RP59**/RC11	41	PGED3/SDA2/FLT31/**RP40**/RB8
20	AN14/PGA2N3/**RP60**/RC12	42	PGEC3/SCL2/**RP47**/RB15
21	AN0/PGA1P1/CMP1A/RA0	43	TDO/AN19/PGA2N2/**RP37**/RB5
22	AN1/PGA1P2/PGA2P1/CMP1B/RA1	44	PGED1/TDI/AN20/SCL1/**RP38**/RB6

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

Pin Diagrams (Continued)

44-Pin TQFP

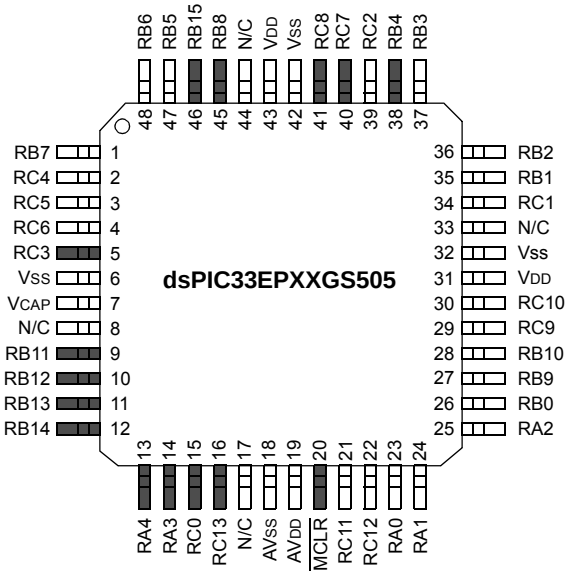


Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/**RP39**/RB7	23	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2
2	AN1ALT/**RP52**/RC4	24	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0
3	AN0ALT/**RP53**/RC5	25	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9
4	AN17/**RP54**/RC6	26	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10
5	**RP51**/RC3	27	AN11/PGA1N3/**RP57**/RC9
6	VSS	28	AN10/PGA1P4/EXTREF2/**RP58**/RC10
7	VCAP	29	VDD
8	TMS/PWM3H/**RP43**/RB11	30	VSS
9	TCK/PWM3L/**RP44**/RB12	31	AN8/PGA2P4/CMP4C/**RP49**/RC1
10	PWM2H/**RP45**/RB13	32	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1
11	PWM2L/**RP46**/RB14	33	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2
12	PWM1H/RA4	34	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3
13	PWM1L/RA3	35	PGEC2/ADTRG31/**RP36**/RB4
14	FLT12/**RP48**/RC0	36	AN9/CMP4D/EXTREF1/**RP50** /RC2
15	FLT11/**RP61**/RC13	37	ASDA1/**RP55**/RC7
16	AVSS	38	ASCL1/**RP56**/RC8
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	AN12/ISRC1/**RP59**/RC11	41	PGED3/SDA2/FLT31/**RP40**/RB8
20	AN14/PGA2N3/**RP60**/RC12	42	PGEC3/SCL2/**RP47**/RB15
21	AN0/PGA1P1/CMP1A/RA0	43	TDO/AN19/PGA2N2/**RP37**/RB5
22	AN1/PGA1P2/PGA2P1/CMP1B/RA1	44	PGED1/TDI/AN20/SCL1/**RP38**/RB6

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

Pin Diagrams (Continued)

48-Pin TQFP

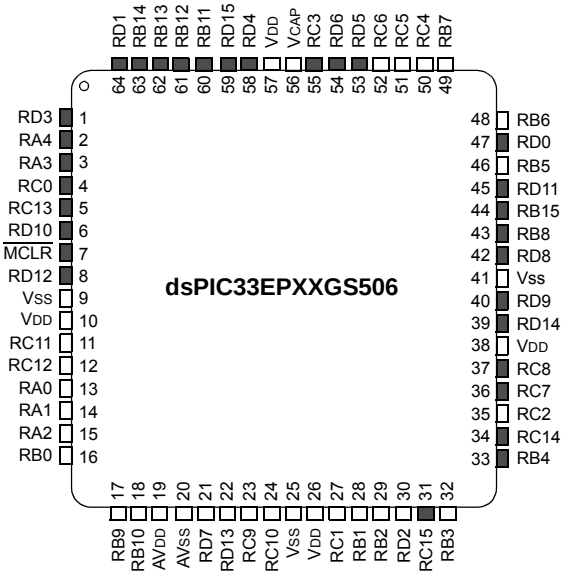


Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/**RP39**/RB7	25	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2
2	AN1ALT/**RP52**/RC4	26	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0
3	AN0ALT/**RP53**/RC5	27	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9
4	AN17/**RP54**/RC6	28	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10
5	**RP51**/RC3	29	AN11/PGA1N3/**RP57**/RC9
6	VSS	30	AN10/PGA1P4/EXTREF2/**RP58**/RC10
7	VCAP	31	VDD
8	N/C	32	VSS
9	TMS/PWM3H/**RP43**/RB11	33	N/C
10	TCK/PWM3L/**RP44**/RB12	34	AN8/PGA2P4/CMP4C/**RP49**/RC1
11	PWM2H/**RP45**/RB13	35	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1
12	PWM2L/**RP46**/RB14	36	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2
13	PWM1H/RA4	37	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3
14	PWM1L/RA3	38	PGEC2/ADTRG31/**RP36**/RB4
15	FLT12/**RP48**/RC0	39	AN9/CMP4D/EXTREF1/**RP50** /RC2
16	FLT11/**RP61**/RC13	40	ASDA1/**RP55**/RC7
17	N/C	41	ASCL1/**RP56**/RC8
18	AVSS	42	VSS
19	AVDD	43	VDD
20	$\overline{\text{MCLR}}$	44	N/C
21	AN12/ISRC1/**RP59**/RC11	45	PGED3/SDA2/FLT31/**RP40**/RB8
22	AN14/PGA2N3/**RP60**/RC12	46	PGEC3/SCL2/**RP47**/RB15
23	AN0/PGA1P1/CMP1A/RA0	47	TDO/AN19/PGA2N2/**RP37**/RB5
24	AN1/PGA1P2/PGA2P1/CMP1B/RA1	48	PGED1/TDI/AN20/SCL1/**RP38**/RB6

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

Pin Diagrams (Continued)

64-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PWM4L/RD3	33	PGEC2/ADTRG31/**RP36**/RB4
2	PWM1H/RA4	34	**RP62**/RC14
3	PWM1L/RA3	35	AN9/CMP4D/EXTREF1/**RP50**/RC2
4	FLT12/**RP48**/RC0	36	ASDA1/**RP55**/RC7
5	FLT11/**RP61**/RC13	37	ASCL1/**RP56**/RC8
6	FLT10/RD10	38	VDD
7	$\overline{\text{MCLR}}$	39	RD14
8	FLT9/T5CK/RD12	40	RD9
9	VSS	41	VSS
10	VDD	42	RD8
11	AN12/ISRC1/**RP59**/RC11	43	PGED3/SDA2/FLT31/**RP40**/RB8
12	AN14/PGA2N3/**RP60**/RC12	44	PGEC3/SCL2/**RP47**/RB15
13	AN0/PGA1P1/CMP1A/RA0	45	INT4/RD11
14	AN1/PGA1P2/PGA2P1/CMP1B/RA1	46	TDO/AN19/PGA2N2/**RP37**/RB5
15	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	47	T4CK/RD0
16	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0	48	PGED1/TDI/AN20/SCL1/**RP38**/RB6
17	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9	49	PGEC1/AN21/SDA1/**RP39**/RB7
18	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10	50	AN1ALT/**RP52**/RC4
19	AVDD	51	AN0ALT/**RP53**/RC5
20	AVSS	52	AN17/**RP54**/RC6
21	AN15/RD7	53	RD5
22	AN13/DACOUT2/RD13	54	PWM5H/RD6
23	AN11/PGA1N3/**RP57**/RC9	55	PWM5L/**RP51**/RC3
24	AN10/PGA1P4/EXTREF2/**RP58**/RC10	56	VCAP
25	VSS	57	VDD
26	VDD	58	RD4
27	AN8/PGA2P4/CMP4C/**RP49**/RC1	59	RD15
28	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1	60	TMS/PWM3H/**RP43**/RB11
29	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2	61	TCK/PWM3L/**RP44**/RB12
30	AN16/RD2	62	PWM2H/**RP45**/RB13
31	ASDA2/**RP63**/RC15	63	PWM2L/**RP46**/RB14
32	PGED2/AN18/DACOUT1/ASCL2/INT0/RP35/RB3	64	PWM4H/RD1

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

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1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXGS50X Digital Signal Controller (DSC) devices.

dsPIC33EPXXGS50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXGS50X FAMILY BLOCK DIAGRAM