

CSC220
Computer organization
Lab project

Arithmetic And logic unit (ALU) with Shifter

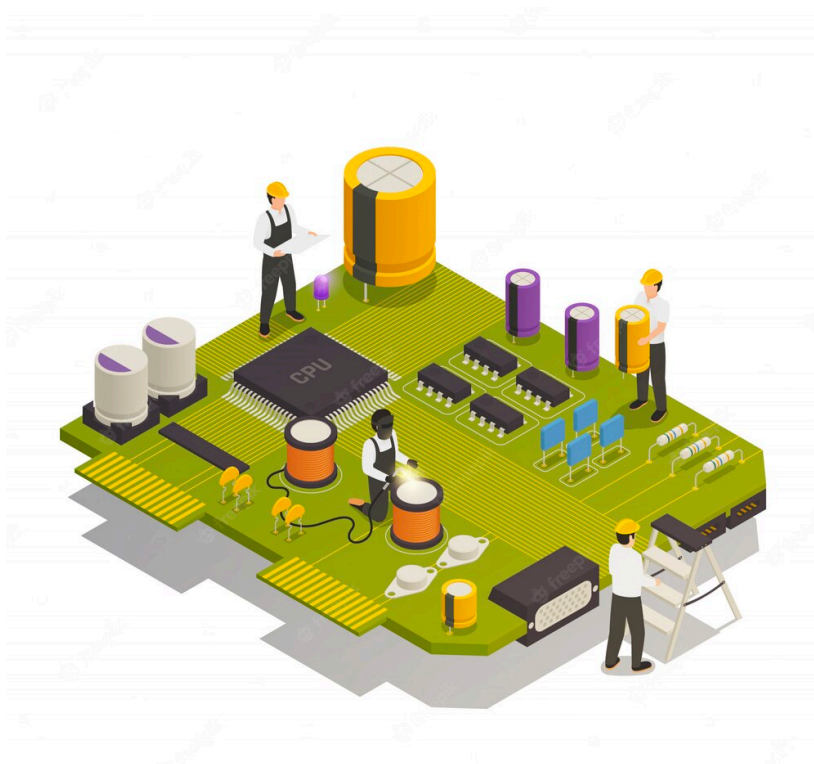
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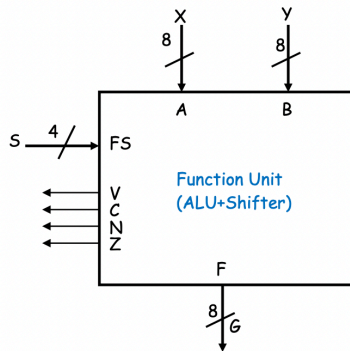
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Project Description :

We will build an ALU with a shifter that takes in two 8-bit values and 4 control lines. Depending on the value of the control line the operation will be performed.

Schematically, here is what we want to build :



The Block-Diagram of 8-bit function unit

This Block diagram is an interface of the ALU . It shows the ALU as an Abstraction we can't see how it works but we do know what it does

What we need to know is that there is 3 status bits that are related to the arithmetic operations which are :

- **Overflow (V)** : set to 1 if the input operands have the same sign, and the result has a different sign.
- **Carry (C)** : set to 1 if there is a carry in the most-significant bit .
- **Negative (N)** : set to 1 when the most-significant bit is 1.

One status bit that is related to the Arithmetic and Logic operations :

- **Zero (Z)** : This is only true if all of the bits of the result are zero

The Default Input To test all the cases are :

- Default input for X : 10001111
- Default input for Y : 10000001

Test cases :

Input				Operation	Input		Expected Output				
					X	Y	G	C	V	N	Z
S3	S2	S1	S0								
0	0	0	0	$G=X+Y'$	1000 1111	1000 0001	0000 1101	1	0	0	0
0	0	0	1	$G=X-Y$	1000 1111	1000 0001	0000 1110	1	0	0	0
0	0	1	0	$G=X$	1000 1111	1000 0001	1000 1111	0	0	1	0
0	0	1	1	$G=X+1$	1000 1111	1000 0001	1001 0000	0	0	1	0
0	1	0	0	$G=X+2$	1000 1111	1000 0001	1001 0001	0	0	1	0
0	1	0	1	$G=X+3$	1000 1111	1000 0001	1001 0010	0	0	1	0
0	1	1	0	$G=X*2$	1000 1111	1000 0001	0001 1110	1	1	0	0
0	1	1	1	$G=X*2+1$	1000 1111	1000 0001	0001 1111	1	1	0	0
1	0	0	0	$G=X \text{ XOR } Y$	1000 1111	1000 0001	0000 1110	X	X	X	0
1	0	0	1	$G=X \text{ OR } Y'$	1000 1111	1000 0001	1111 1111	X	X	X	0
1	0	1	0	$G=X \text{ NAND } Y$	1000 1111	1000 0001	0111 1110	X	X	X	0
1	0	1	1	$G = X'$	1000 1111	1000 0001	0111 0000	X	X	X	0
1	1	0	0	$G = Y$	1000 1111	1000 0001	1000 0001	X	X	X	0
1	1	0	1	$G = \text{Arithmetic Shift Right } Y$	1000 1111	1000 0001	1100 0000	X	X	X	0
1	1	1	0	$G = \text{Logical Shift Right } Y$	1000 1111	1000 0001	0100 0000	X	X	X	0
1	1	1	1	$G= \text{Switch Tail Left } Y$	1000 1111	1000 0001	0000 0010	X	X	X	0

Circuit diagram :

