## CSE 331 - Computer Organization Project-4: I-Type MIPS II (Addition of lw and sw)

Due to December 10 Wednesday-23:00

In this project, you will use Altera Quartus II with Verilog. You will design **another small** part of the 32-bit MIPS processor.

The only supported instructions in your design will be **lW**, **SW** and **Project 3 instructions**, which were **addi**, **addiu**, **andi**, **ori**, **lui**, **sltiu**, **slti**, **beq and bne** instructions. Your top block will get NO inputs, but you should initialize the Instruction memory with the desired assembly program.

You will write the contents of the **registers**, the **instruction memory** and the **data memory** before and after the execution of instructions using **writemenh** in your testbench verilog code. You will initialize all memory contents using **readmenh**. Also you will have a Program Counter register that shows the next instruction.

YOU WILL NOT SUPPORT R-TYPE INSTRUCTIONS. Therefore do not put any additional logic for that.

BITS:	31-26	25-21	20-16	15-0	
	op	rs	rt	immediate/address	
'	6 bits	5 bits	5 bits	16 bits	
I-FORMAT INSTRUCTION					
op - operation rs - source register rt - transition register (made this up) immediate/address - immediate value					

- 1. Other than the parts you used in Project 3 you need a Data Memory to load data from it and to store data to it. Data Memory will be a 4GB memory with 32-bit address input.
- 2. Also you have to insert Instruction Memory to your design. Its size will be 4K.
- 3. You will insert a PC register to show the address of the next instruction. Therefore beq and bne instructions must also work as they work in the real case.
- 4. Do not use behavioral Verilog other than for the memory modules.

Read the rules on the next page too!!

Your design should not support R-type or J-type instructions. Only the instructions listed above.

Please be sure that your design simulates correctly. **Designs that are not even simulating can get at most 25 points.** Therefore at least support a subset of instructions correctly to get more points.

Submit your Altera Project folder as a zip file to Moodle. We will simulate your design using not only your testbench but also our testbench to see whether all instructions are executing correctly or not.

No late submissions even if it is 5 minutes. No medical reports. No excuses. No cry. So start early.

Any cheating attempt with the previous years' projects or with your friends or Internet will result in at least -100 and at most -300. No matter you gave or take the code. Protect your code.

