

24/07/24

VLSI Testing & Testability

1 → 10
3 → 30 $\frac{100}{50}$

- * Introduction to Digital Testing
- * Fault simulation and Testability measures.
- * Comb ckt's Test Pattern Generation
- * Seq ckt testing and scan change
- * Built in Self Test (BIST)

Books:
① Abramovici, M. Breuer, M.A. & Friedman
A.D Digital systems testing and testable design
② Bushnell & Agarwal

Application areas of chips

- (a) Mobile / laptop / Desktop
- (b) Automobile Industry (sensors)
- (c) Aerospace
- (d) Defence

VLSI realization process

design
customer's need

ASIC (Application Specific Integrated ckt)
(more cost)
general purpose

determine requirements
write specification

Design synthesis & verification

Test development

fabrication

Manufacturing test

chips to customer

digital design

Xilinx vivado
Mostly used device
for synthesis &
simulation

Simulation : functional verification (checks only the O/p)

Synthesis : code is converted to the H/w. (ready for fabrication)

code
— Behavioral
— Structural
— Data flow

ATE → Automatic Test Equipment

* After fabrication testing will be done

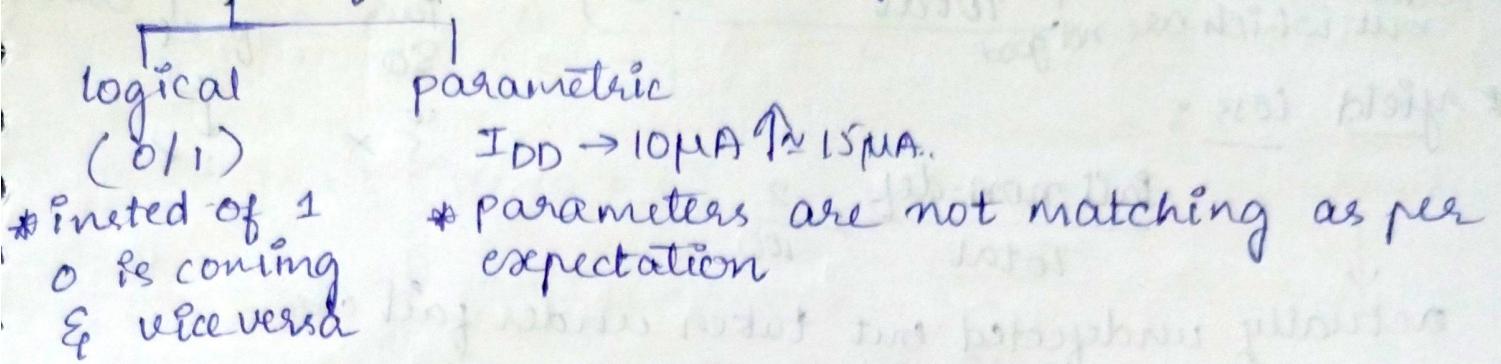
verification → analysis to ensure that the synthesized design, when manufactured, will perform the given I/O fun.

Verification	Test
• correctness of design	* correctness of manufactured H/w
• performed by simulation, H/w emulation or formal methods.	* (i) <u>Test generation</u> : S/w process executed once during design (ii) <u>Test applications</u> electrical tests applied to H/w
• performed once prior to manufacturing	* Test application performed on every manufactured device
* Responsible for quality of design	* Responsible for quality of device.

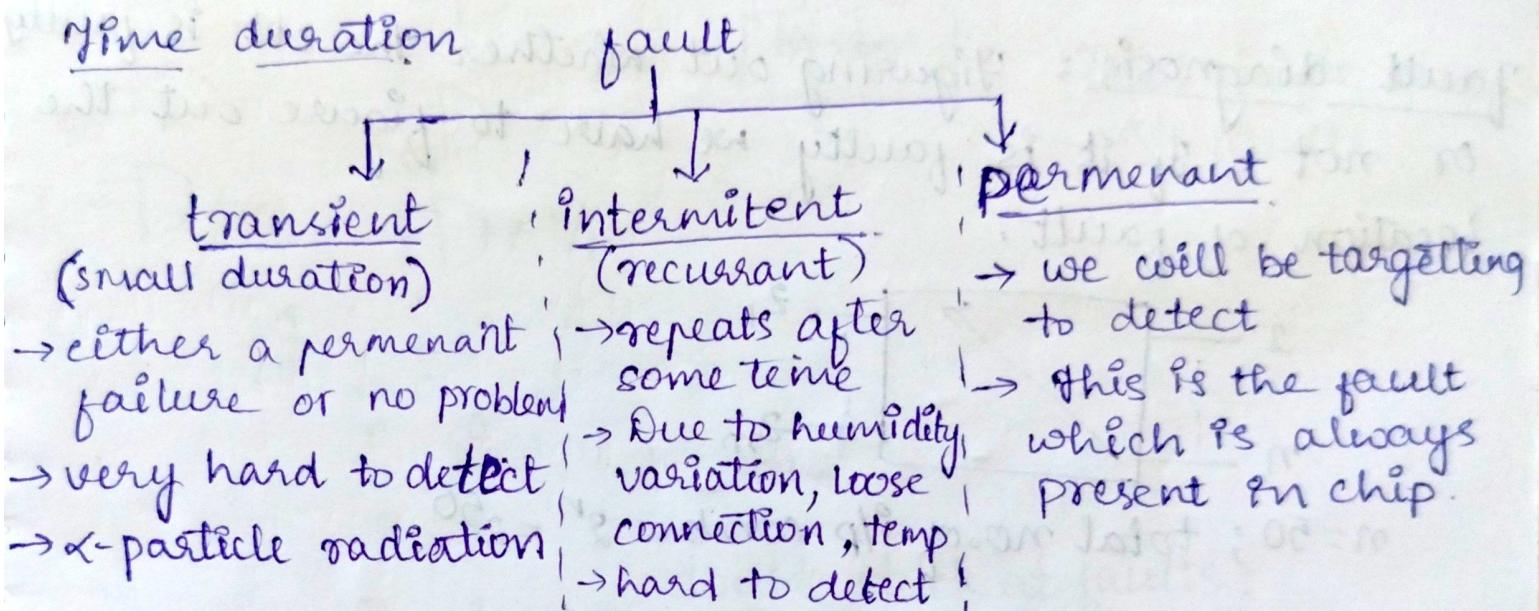
* Detection of defects → nonfunctions in eqn
imperfection in H/w
fault → defect in digital design.

error → if p's are applied but q/p's are not as per required.

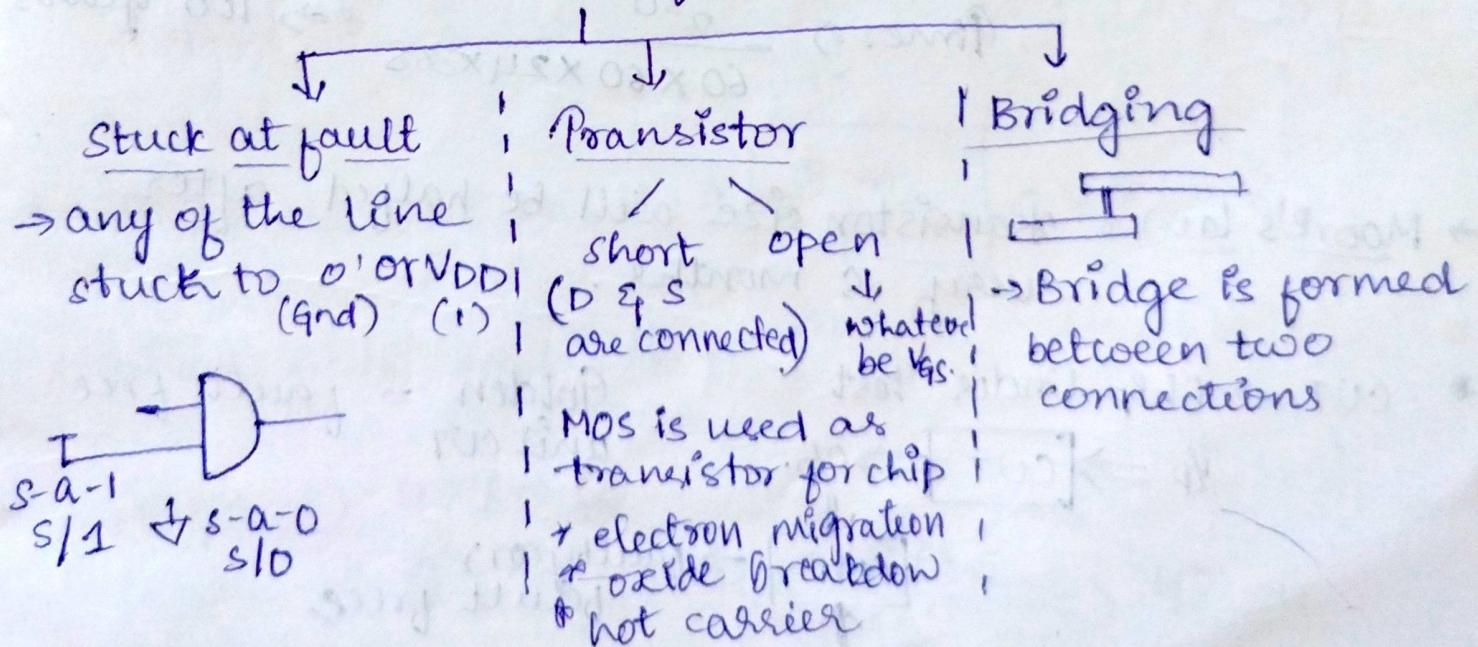
Faults: defects in digital design



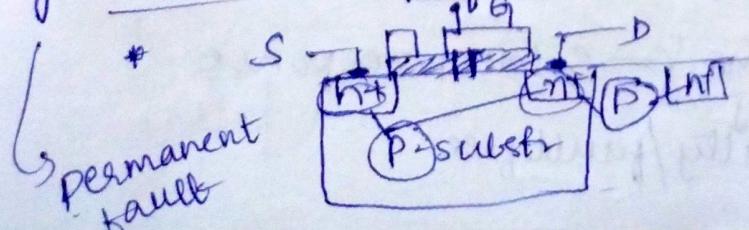
Time duration



Permanent fault



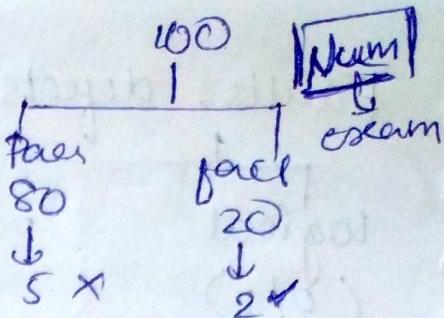
geometrical Imperfections



* n-p-n transistors or p-n-p transistors are formed which are not required

defect level :-
termed as pces
but which are not good

$$\frac{\text{defect pces}}{\text{Total}} = \frac{5}{100}$$

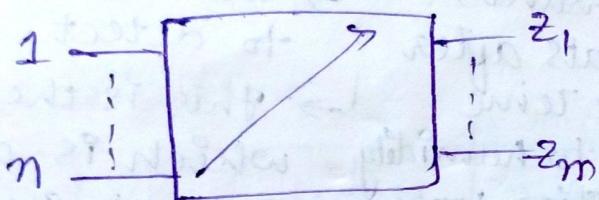


* yield loss :-

$$\frac{\text{fail non-def}}{\text{Total}} = \frac{2}{100}$$

actually undefected but taken under fail case.

fault diagnosis :- Figuring out whether the ckt is faulty or not. If it is faulty we have to figure out the location of fault.



$$n=50; \text{ total no. of i/p comb} = 2^n = 2^{50}$$

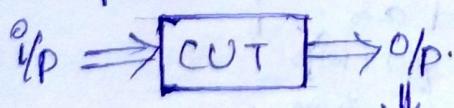
$$1 \text{ MHz} \rightarrow t = 1 \mu\text{s}$$

$$\Rightarrow 2^{50} \times 10^{-6} = 2^{30} \text{ sec}$$

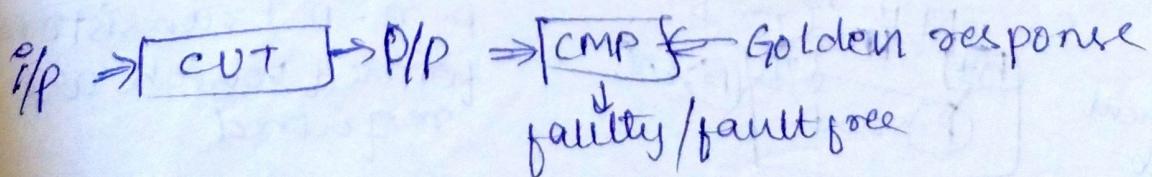
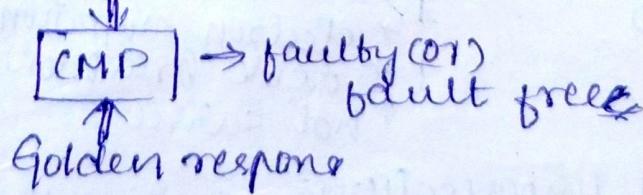
$$\text{Time.} \Rightarrow \frac{2^{30}}{60 \times 60 \times 24 \times 365} \Rightarrow 100 \text{ years}$$

→ Moore's law :- Transistor size will be halved after every 18 months.

* CUT → Chip Under Test

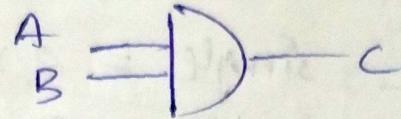


Golden unit CUT ⇒ fault free



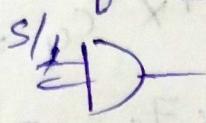
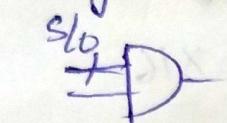
* Stuck at faults

S-a-0
S-a-1



Nets fault sites (A, B, C)

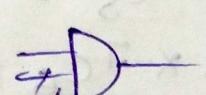
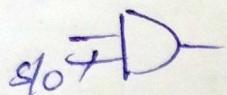
Single stuck at fault;



$n = \text{fault sites}$

$$\boxed{n \times 2^1}$$

← Total single stuck at faults



$$= D + S_0$$

$$= D + S_1$$

*

00	A	B	C
00	0	0	0
01	0	1	0
01	1	0	0
11	1	1	0
11	1	1	1
00	0	0	1
01	0	1	1
11	1	1	1
10	1	0	1

$$4 \times 3 = 12$$

double stuck at faults;

$$\boxed{2^2 \cdot n_{C_2}} \Rightarrow 4 \cdot 3_{C_2} = \frac{4 \times 3 \times 2}{2!} \Rightarrow \frac{12}{2!}$$

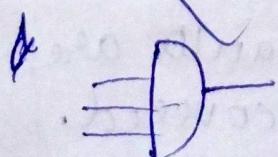
* Triple stuck at faults $\Rightarrow \boxed{2^3 \cdot n_{C_3}} \Rightarrow 8 \times 1 = 8$

$$\Rightarrow \text{Multiple stuck at faults} = 3^n - 1$$

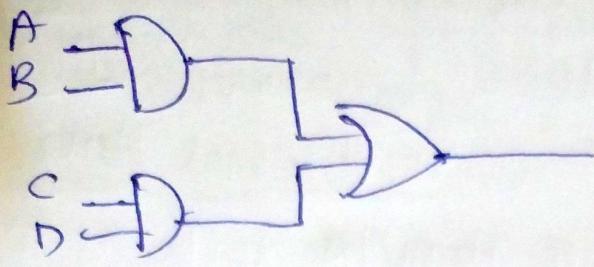
single $\Rightarrow 4 \times 2 \Rightarrow 8$

double $\Rightarrow 2^2 \times 4_{C_2} \Rightarrow 4 \times \frac{4 \times 3 \times 2}{2!} \Rightarrow 48$ 24

triple $\Rightarrow 8 \times 4_{C_3}$



$$n_{C_2} \Rightarrow \frac{4 \times 3 \times 2}{2!} \times 4$$



$$\text{sevent} \quad 7C_4 = \frac{7 \times 6 \times 5 \times 4}{4! \times 3! \times 2}$$

$$n=7$$

$$\text{single} = 2 \times {}^7C_1 = 14$$

$$\text{double} \Rightarrow 2 \times {}^7C_2 = 2 \times \frac{7 \times 6}{2} = 84$$

$$\text{triple} \Rightarrow 2^3 \times {}^7C_3 = 8 \times \frac{7 \times 6 \times 5}{3!} = 560$$

$$\text{quadruple} \Rightarrow 2^4 \times {}^7C_4 = 16 \times 35 = 560$$

$$\text{Pent} = 32 \times {}^7C_5 = \\ \text{six} \Rightarrow 64 \times {}^7C_6$$

$$\text{single} = 2 \cdot {}^4C_1 = 8$$

$$\text{double} = 2 \cdot {}^4C_2 =$$

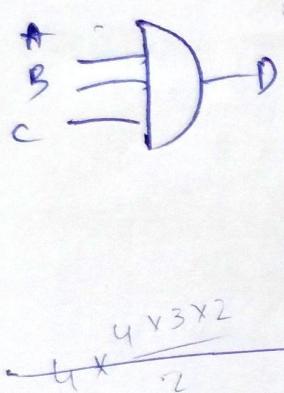
$$\text{triple} = 2^3 \cdot {}^4C_3 =$$

$$\text{quadruple} = 2^4 \times {}^4C_4 = 16$$

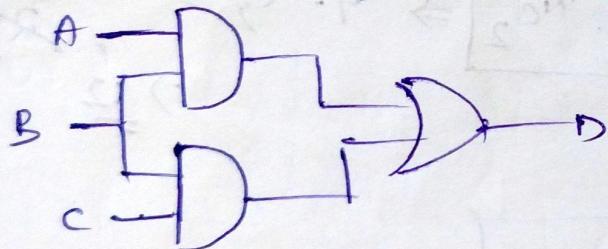
seven

$$10 \times 56 \\ 16 \times 7 \times$$

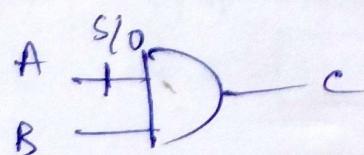
$$7C_2 = \frac{56}{240} = \frac{7 \times 6}{7 \times 6}$$



Total fault sites = 8



* Stuck at fault



We well know that there is fault when we will give

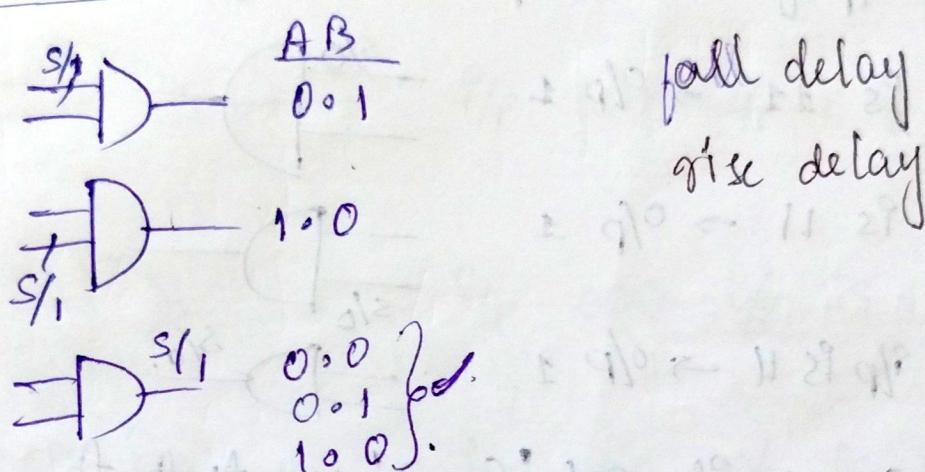
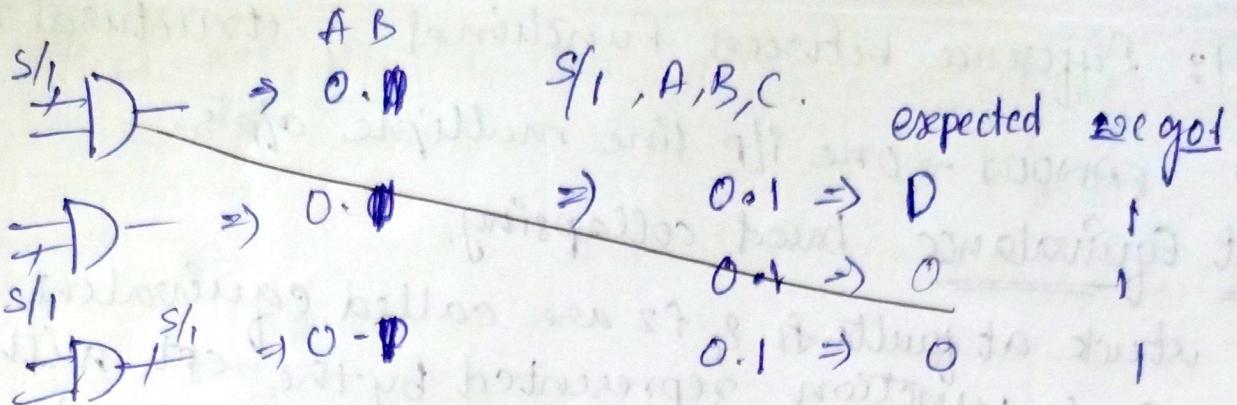
$$A=0 \quad A=B=1$$

$$\begin{array}{l} 0,0 \\ 0,1 \\ 1,0 \\ 1,1 \end{array} \rightarrow 0 \quad C^f = A \cdot B$$

$$1,1 \rightarrow 1 \Rightarrow S/0, A, B, C$$

double stuck at $\{S/0\}$ are covered.

$\Rightarrow 50\%$ of faults are covered.



Functional versus structural testing

Testing → Functional (only observe O/P) 3²⁷-1

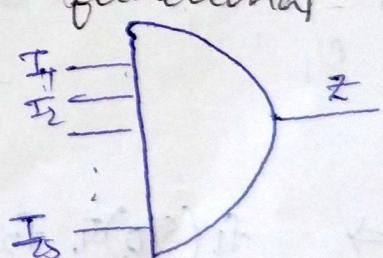
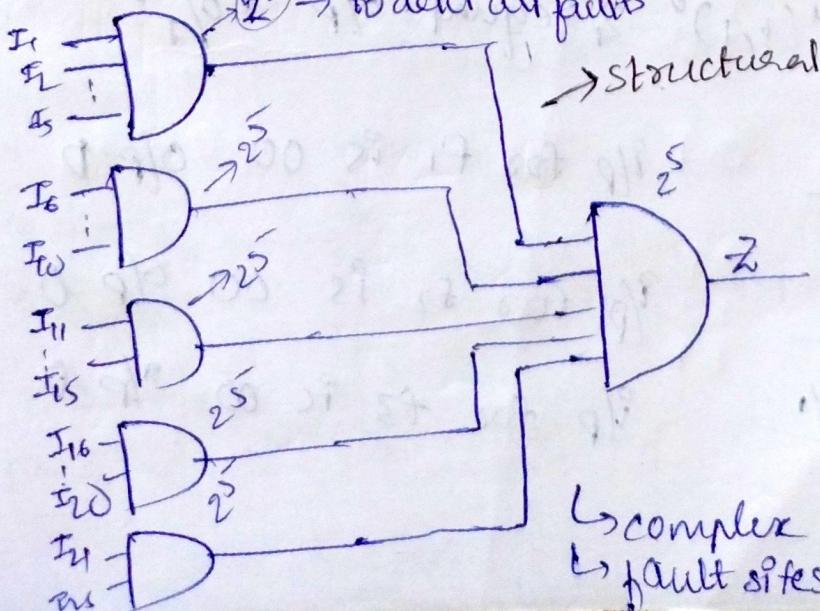
→ structural (inside design)

Wherever there is a stuck at fault give that I/P as opposite of that fault.

$S_0 \rightarrow$ rem I/P (controlling I/P's - 1)

$S_1 \rightarrow$ rem I/P (control I/P - 1)

(25) → to detect all faults



$$\text{Total faults} \Rightarrow 6 \times 2^5$$

$$\Rightarrow 192$$

$$192 \times 4 = 10^6 \text{ Hz}$$

$$T = 1 \text{ ms}$$

$$\text{Testing time} = 0.19 \text{ ms}$$

↳ complex nature

↳ fault sites ↑ so no. of faults ↑

IMP: Difference between Functional & structural

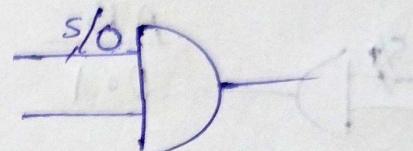
08/08/24

FANOUT \rightarrow one I/P line multiple O/P's

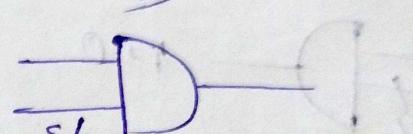
Fault equivalence based collapsing.

Two stuck at faults f_1 & f_2 are called equivalent if the output function represented by the ckt with f_1 is same as the o/p function represented by ckt with f_2 .

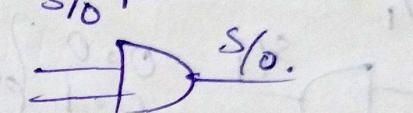
I/P for f_1 is 11 \rightarrow O/P 1



I/P for f_2 is 11 \rightarrow O/P 1

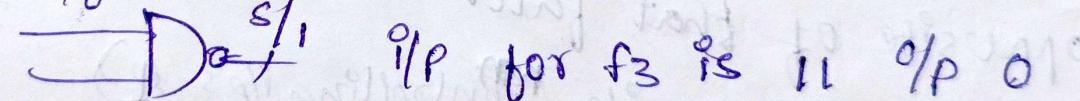
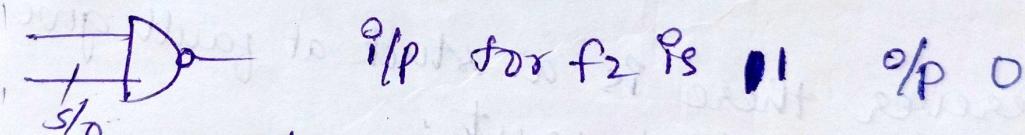
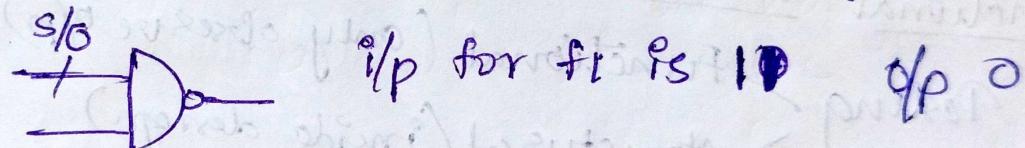


O/P is f_3 I/P is 11 \rightarrow O/P 1



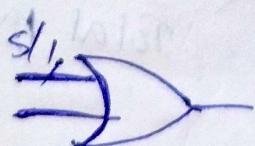
* Implies that same I/P set '(1, 1)' for f_1, f_2, f_3 .
& same O/P "1/0"

101
001
011
110
011

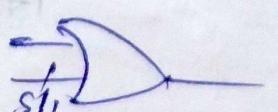


$\Rightarrow f_1(S/I)I_1, f_2(S/I)I_2, f_3(S/I)O$ all these faults are having equal I/P's "(1, 1)" & equal O/P "1/0".

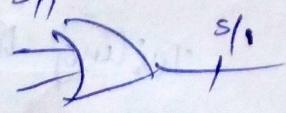
000
011
101
111



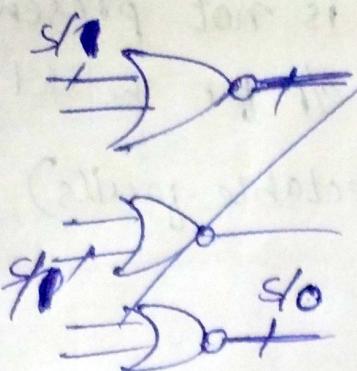
I/P for f_1 is 00 O/P 0



I/P for f_2 is 00 O/P 0

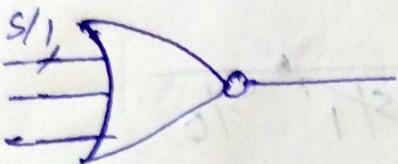


I/P for f_3 is 00 O/P 0



q/p 00

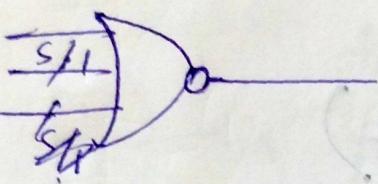
00	1
01	0
10	0
11	0



q/p 000 q/p is 1

11	0
----	---

000 1



q/p 000 q/p is 1



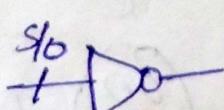
q/p 000 q/p is 1



q/p 000 q/p is 1

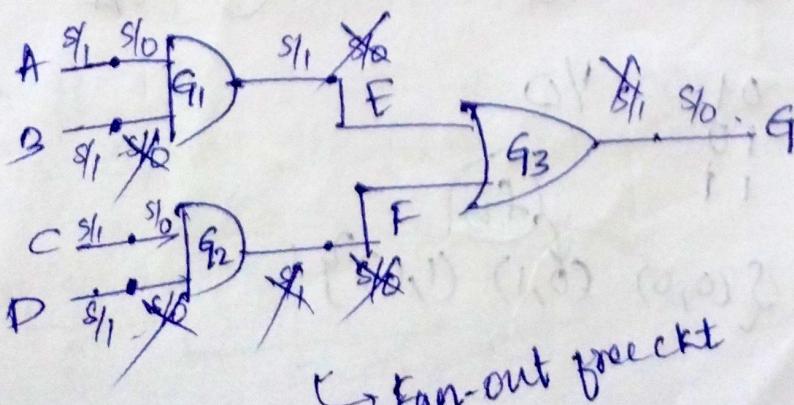
$\Rightarrow f_1(s1), f_2(s1), f_3(s1), f_4(s0)$ & all these faults are having equal q/p(0,0,0) & equal o/p "1/0"

o/p "1/0"



q/p stuck at 0 = o/p stuck at 1

q/p - s1 \Rightarrow o/p + s1

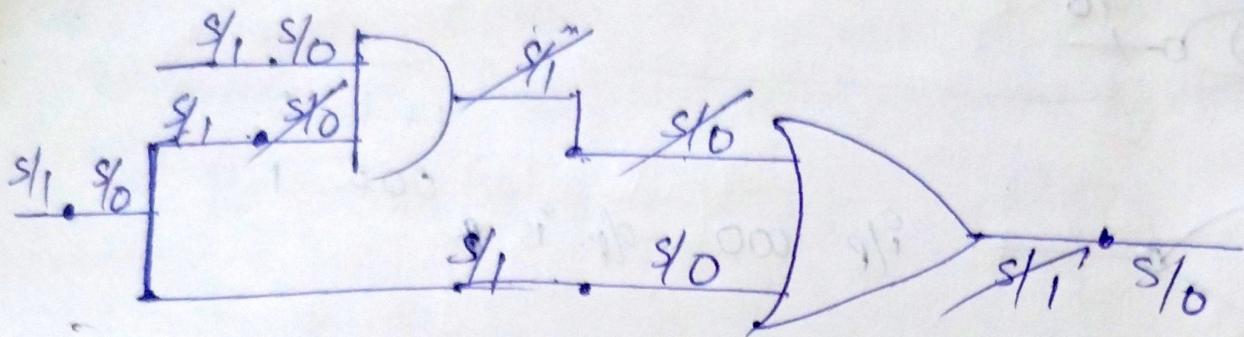


removal of equivalent faults is called fault equivalence based collapsing.

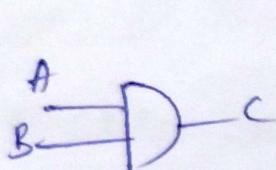
fan-out freeckt

Fan out free Ckt \rightarrow if fault equivalence is not present
(same P/Ps & same O/P for the ckt)

\rightarrow Every fault can not be detected (undetectable faults)

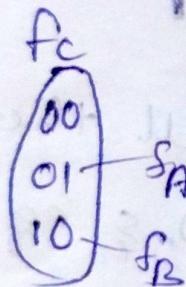


* FAULT DOMINANCE

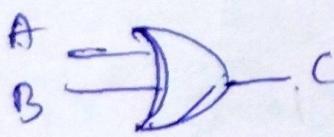


	A/1	P/P	O/P	(F/F/F)
B/1,	10	01	01	
C/1,	00	01	01	

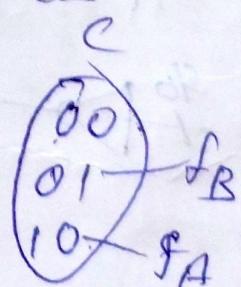
\rightarrow Here f_c is dominant so we have to remove it



f_A & f_B are subset of f_c " by given any of the P/P's of A or B faults of 'C' also will be removed.

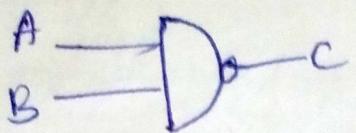


	A/0	P/P	O/P
B/0	10	10	10
C/0	01	10	10
	10	10	10

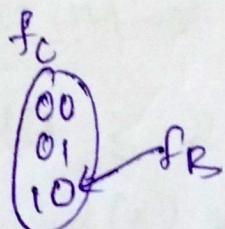
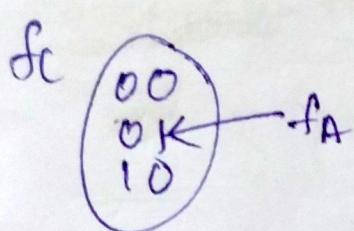


$f_c \{ (0,1) \} \{ (0,1), (1,0) \} \{ (0,1), (1,0) \}$

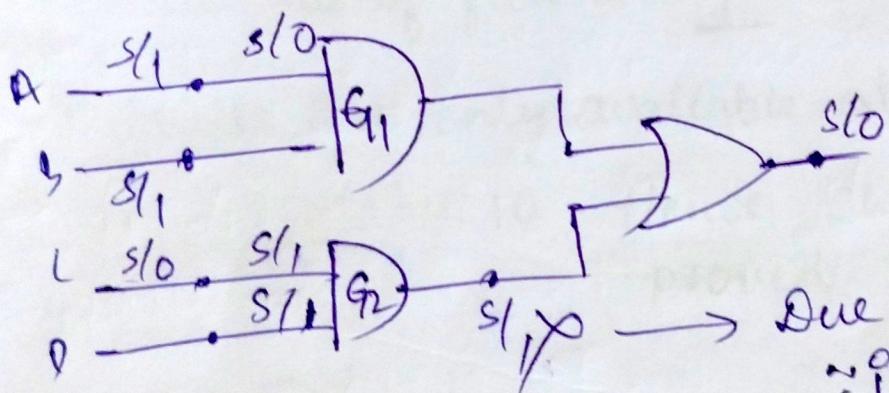
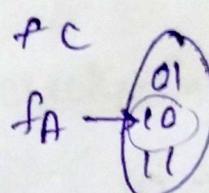
$f_c \{ (0,0) \} \{ (0,1), (1,0) \} \{ (0,1), (1,0) \}$



<u>fault location</u>	$\overset{?}{I/P}$	O/P
A/0	01	10
B/0	10	10
C/0	00 01 10	10



<u>fault location</u>	$\overset{?}{I/P}$	O/P
A/0	10	01
B/0	01	01
C/1	01 10 11	01

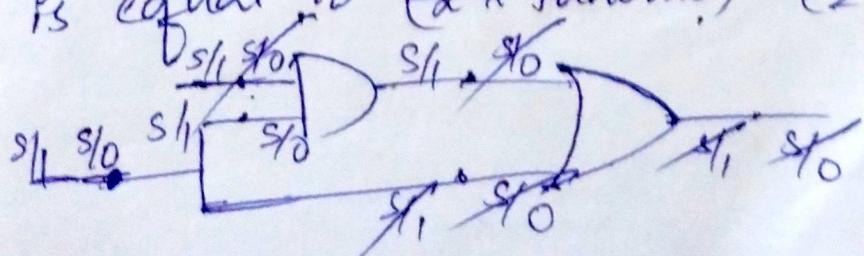


Due to fault dominance
it can be eliminated
by the S_{11} 's at C & D.

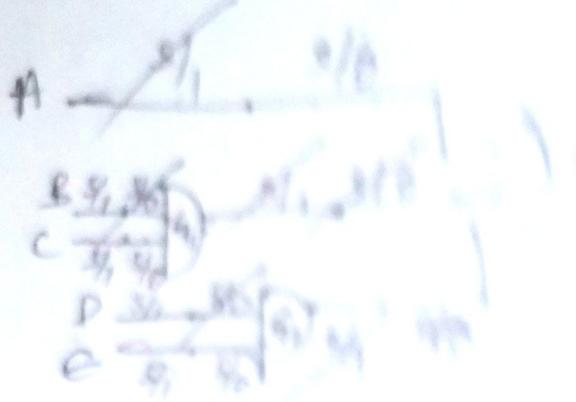
Check-point theorems

$$\text{Check-points} = \overset{?}{I/P} + \text{fanout}$$

It says that the total no. of faults after collapsing is equal to $(2 \times \text{fanouts})$ ($2 \times \text{check points}$)



$$2 \times 4 = 8$$



no. of i/p's = 2
Fanout's = 2

check fault tolerance

no. of faults = 2

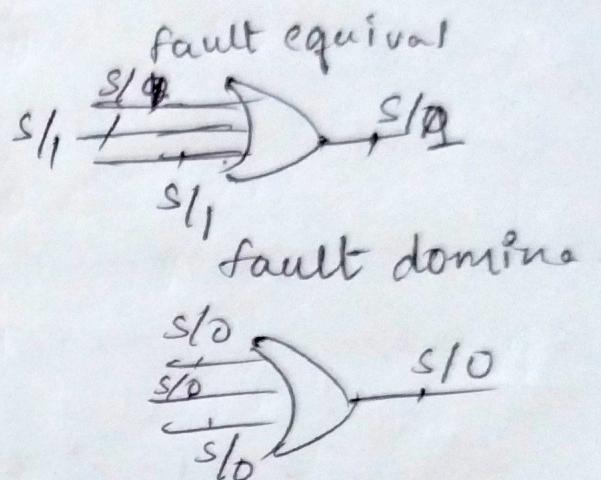
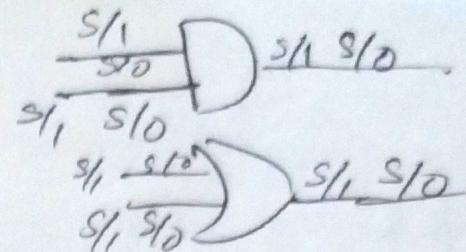
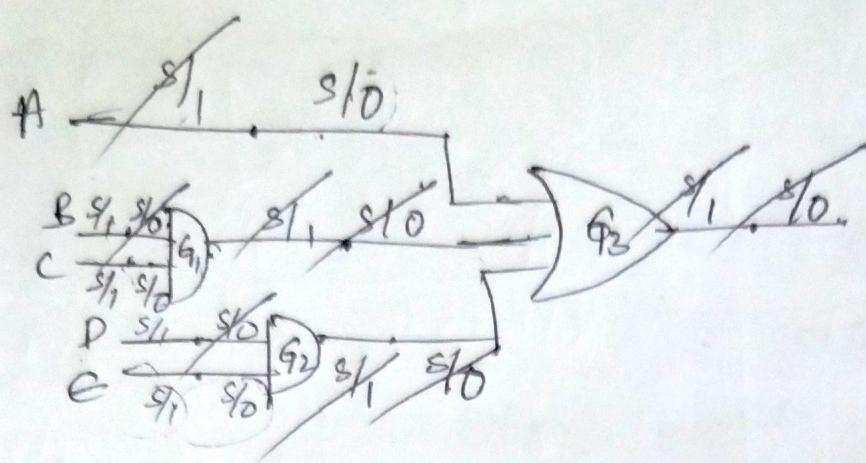
no. of faults = 2

* faults are 2

= 2

using some controllability

x	y	z
0	0	1
0	1	1
1	0	1
1	1	0



No. of I/P's = 5

Fanout's = 0

check point theorem

No. of faults $\leq 2(\text{No. of checkpoint})$

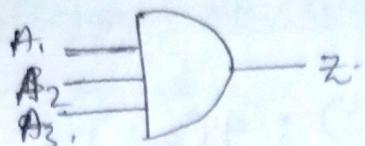
$2(5) = 10 \times 10 \rightarrow \text{Max no. of faults available}$.

No. of faults = 7

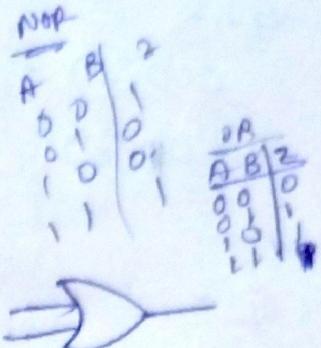
* Faults are only available at I/P's & fanout's.

$7 < 10$ Hence Check-point theorem is proved.

21/08/24
Wednesday



AND	
0	0
0	0
1	0
1	1



$$\therefore \text{CCO}(Z) = \min(\text{CCO}(A_i)) + 1$$

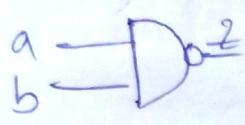
$$\text{CCI}(Z) = \sum(\text{CCI}(A_i)) + 1$$

$A_i^o \rightarrow$ Inputs of gate



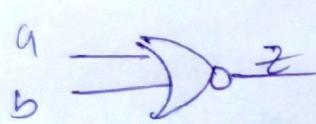
$$\text{CCO}(Z) = \min(\text{CCO}(a) + \text{CCO}(b), \text{CCI}(a) + \text{CCI}(b) + 1)$$

$$\text{CCI}(Z) = \min(\text{CCI}(a) + \text{CCO}(b), \text{CCO}(a) + \text{CCI}(b)) + 1$$



$$\text{CCO}(Z) = \text{CCI}(a) + \text{CCI}(b) + 1$$

$$\text{CCI}(Z) = \min(\text{CCO}(a), \text{CCO}(b)) + 1$$

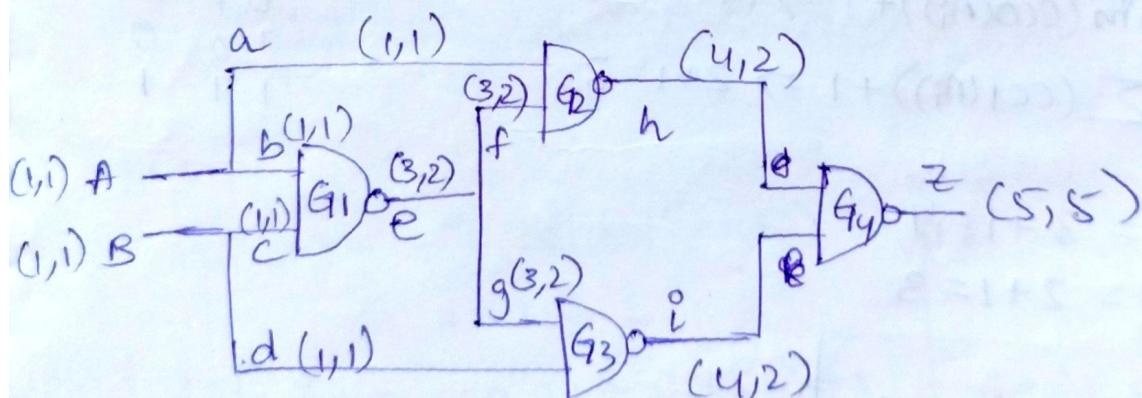


$$\text{CCO}(Z) = \min(\text{CCI}(a), \text{CCI}(b)) + 1$$

$$\text{CCI}(Z) = \text{CCO}(a) + \text{CCO}(b) + 1$$

* (CCO, CCI)

A, B are the I/P let us assume CC's at I/P as 1



Since branching/fanout are having same controllability

$$\text{For NAND: } \text{CCO}(Z) = \sum(\text{CCI}(A_i)) + 1$$

$$\text{CCI}(Z) = \min(\text{CCO}(A_i)) + 1$$

+ 0	= 2
0	0
0	1
1	1
1	0
1	1

Q1:

$$\begin{array}{l} \text{CCO}(e) = 1+1+1=3 \\ \text{CCI}(e) = 1+1=2 \end{array} \quad \left| \Rightarrow f(3,2); g(3,2) \right.$$

Q2:

$$\begin{array}{l} \text{CCO}(n) = 1+2+1=4 \\ \text{CCI}(n) = 1+1=2 \end{array} \quad \left| \Rightarrow \text{due to symmetry} \quad h(4,2) \quad i(4,2) \right.$$

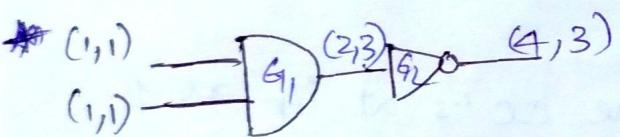
Q3:

due to symmetry $h=i$

Q4:

$$\text{CCO}(z) = 2+2+1=5$$

$$\text{CCI}(z) = 4+1=5$$



$$\underline{\text{Q1:}} \quad \text{CCO}(z) = \min(\text{CCO}(A_i)) + 1 \Rightarrow 1+1=2$$

$$\text{CCI}(z) = \sum(\text{CCI}(A_i)) + 1 \Rightarrow 2+1=3$$

AND

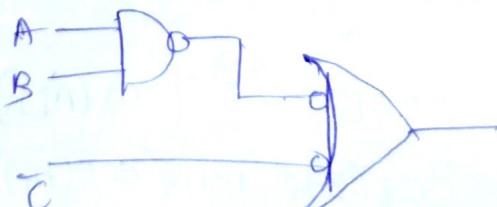
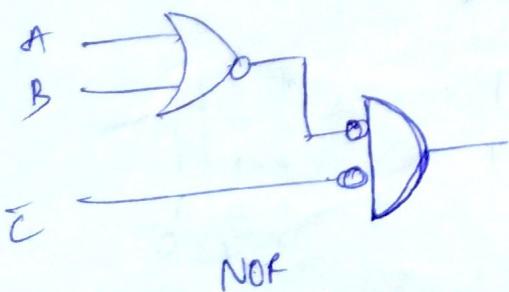
0	0	0
0	1	0
1	0	0
1	1	1

$$\underline{\text{Q2:}} \quad \text{CCO}(z) = 3+1=4$$

$$\text{CCI}(z) = 2+1=3$$

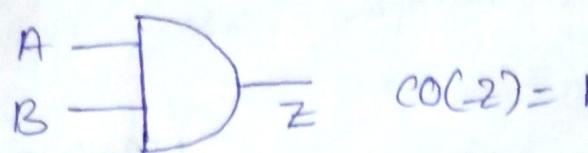
Assignment

Ex-NOR using NOR's only



Combinational observability (CO)

$$CO = [CO(A)]$$



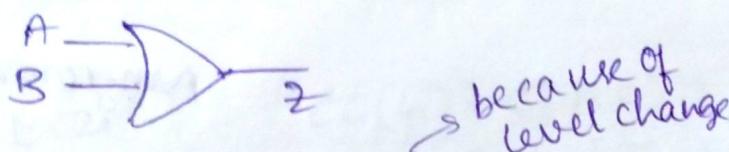
$$CO(2) = 1$$

Observing the
Op is easy

controlling the
Op is easy

$$CO(A) = CO(Z) + 1 + CC1(B)$$

$$CO(B) = CO(Z) + 1 + CC1(A)$$



$$CO(A) = CO(Z) + 1 + CC0(B)$$

$$CO(B) = CO(Z) + 1 + CC0(A)$$

$$CO(A) = CO(Z) + 1 + CC1(B) + CC1(C)$$

$$CO(B) = CO(Z) + 1 + CC1(A) + CC1(C)$$

$$CO(C) = CO(Z) + 1 + CC1(A) + CC1(B)$$

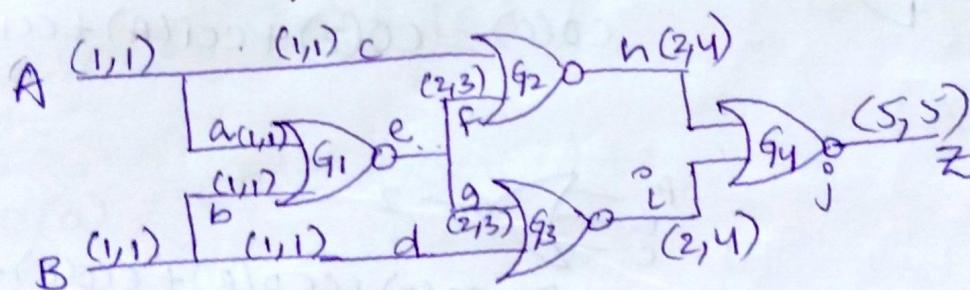


$$CO(A) = CO(Z) + CC0(B) + CC0(C) + 1$$

$$CO(B) = CO(Z) + CC0(A) + CC0(C) + 1$$

$$CO(C) = CO(Z) + CC0(A) + CC0(B) + 1$$

EX-NOR using NOR



G1

$$CC0(Z) = \min(CC1(a), CC1(b)) + 1$$

$$\Rightarrow 1+1=2$$

$$CC1(Z) = CC0(a) + CC0(b) + 1$$

$$\Rightarrow 1+1+1=3$$

- e(2,3)

due to symmetry or fanout ; f(2,3) ; g(2,3)?

G2

$$CC0(Z) = \min(CC1(a), CC1(b)) + 1$$

$$\Rightarrow 1+1=2$$

$$CC1(Z) = 1+2+1=4$$

n(2,4)

due to symmetry i(2,4)

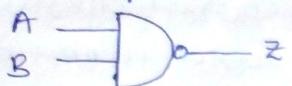
G4

$$\begin{aligned} CO(z) &= 4+1=5 \\ CC_1(z) &= 2+2+1=5 \end{aligned}$$

| P(5,5)

CO

NAND gate

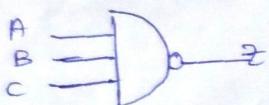


$$CO(z) = 1$$

$$CO(A) = CO(z) + 1 + CC_1(B)$$

$$CO(B) = CO(z) + 1 + CC_1(A)$$

NAND:



$$CO(A) = CO(z) + CC_1(B) + CC_1(C) + 1$$

$$CO(B) = CO(z) + CC_1(A) + CC_1(C) + 1$$

$$CO(C) = CO(z) + CC_1(A) + CC_1(B) + 1$$

NOR



$$CO(A) = CO(z) + CC_0(B) + 1$$

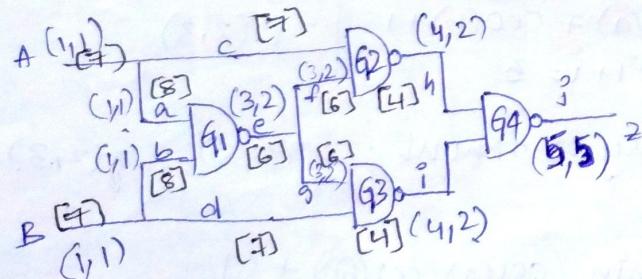
$$CO(B) = CO(z) + CC_0(A) + 1$$



$$CO(A) = CO(z) + CC_0(B) + CC_0(C) + 1$$

$$CO(B) = CO(z) + CC_0(A) + CC_0(C) + 1$$

$$CO(C) = CO(z) + CC_0(A) + CC_0(B) + 1$$



NAND		AND	
00	1	00	0
01	1	01	0
10	1	10	0
11	0	11	1

Non-controlling
is 1

G4

$$\begin{aligned} CO(h) &= CO(j) + CC_1(i) + 1 \\ &\Rightarrow 1 + 1 + 2 = 4 \end{aligned}$$

from symmetry $CO(h) = CO(i) = [4]$

G2

$$\begin{aligned} CO(c) &= CO(h) + CC_1(f) + 1 \\ &\Rightarrow 4 + 2 + 1 \Rightarrow 7 \end{aligned}$$

from symmetry $CO(c) = CO(d) = [7]$

$$\begin{aligned} CO(f) &= CO(h) + CC_1(c) + 1 \\ &\Rightarrow 4 + 1 + 1 = 6 \end{aligned}$$

$$CO(f) = CO(g) = [6]$$

→ If there is a fanout then we have to take the least value:

$$CO(e) = [6]$$

G1

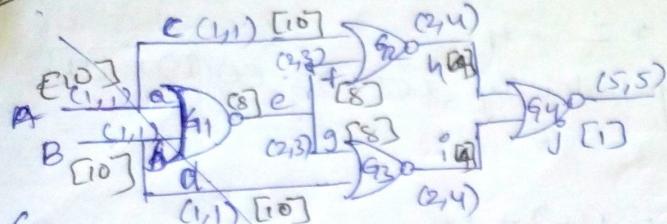
$$\begin{aligned} CO(a) &= CO(e) + CC_1(b) + 1 \\ &\Rightarrow 6 + 1 + 1 = 8 \end{aligned}$$

$$\begin{aligned} CO(b) &= CO(e) + CC_1(a) + 1 \\ &= 6 + 1 + 1 = 8 \end{aligned}$$

$$CO(a) = CO(b) = [8]$$

* CO values are increasing from o/p to i/p while CC's are increasing from i/p to o/p.

Ex.



G₄

$$co(h) = 1 + 2 + 1 = 4$$

due to symmetry $co(h) = co(i) = [4]$

G₃ & G₂

$$co(c) \Rightarrow 6 + 3 + 1 = 10$$

due to symmetry $co(c) = co(d) = [10]$

$$co(f) = co(h) + cco(c) + 1$$

$$\Rightarrow 6 + 1 + 1 = 8$$

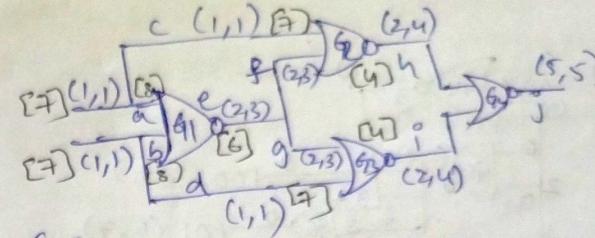
due to symmetry $co(f) = co(g) = [8]$

$$co(e) = [8]$$

G₁ :-

$$co(a) = 8 + 1 + 1 = 10$$

due to symmetry $co(a) = co(b) = [10]$



G₄:

$$co(h) = co(j) + cco(i) + 1$$

$$\Rightarrow 1 + 2 + 1 = 4$$

due to symmetry $co(h) = co(i) = [4]$

G₂ & G₃

$$co(c) = co(h) + cco(f) + 1$$

$$\Rightarrow 4 + 2 + 1 = 7$$

due to symmetry $co(c) = co(d) = [7]$

$$co(f) = co(h) + cco(c) + 1$$

$$\Rightarrow 4 + 1 + 1 = 6$$

due to symmetry $co(f) = co(g) = [6]$

due to fanout $co(e) = [6]$

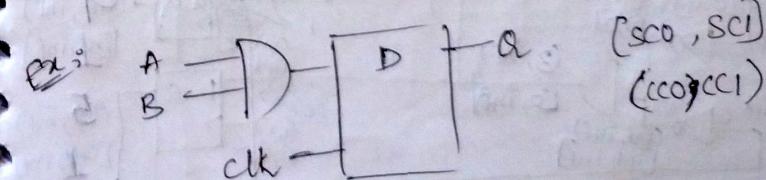
G₁:

$$co(a) = co(e) + cco(b) + 1$$

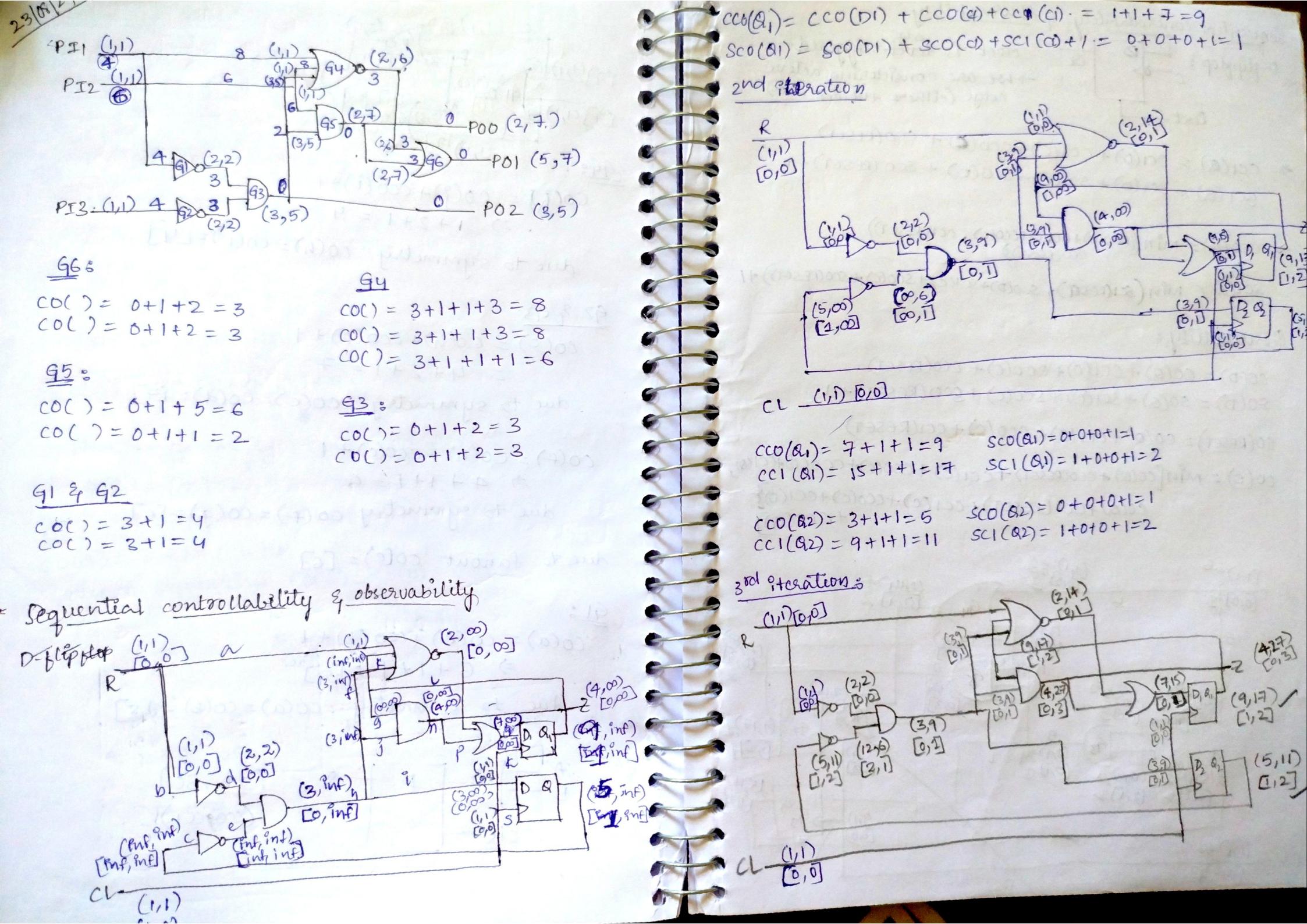
$$\Rightarrow 6 + 1 + 1 = [8]$$

due to symmetry $co(a) = co(b) = [8]$

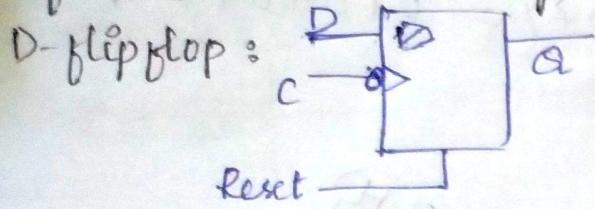
Ex:-



(SCO, SCI)
(CCO, CCI)



Sequential controllability & observability



clock is triggered
→ we are considering active edge (either +ve or -ve)

$$\rightarrow CC_1(Q) = CC_1(D) + CC_1(C) + CC_0(0) + CC_0(Reset)$$

$$SC_1(Q) = SC_1(D) + SC_1(C) + SC_0(0) + SC_0(Reset) + 1$$

$$\rightarrow CC_0(Q) = \min_{CC_0(Reset)} (CC_0(0) + CC_1(C) + CC_0(0), CC_1(Reset))$$

$$SC_0(Q) = \min_{SC_0(Reset)} (SC_1(Reset), SC_0(D) + SC_1(C) + SC_0(0) + SC_0(Reset)) + 1$$

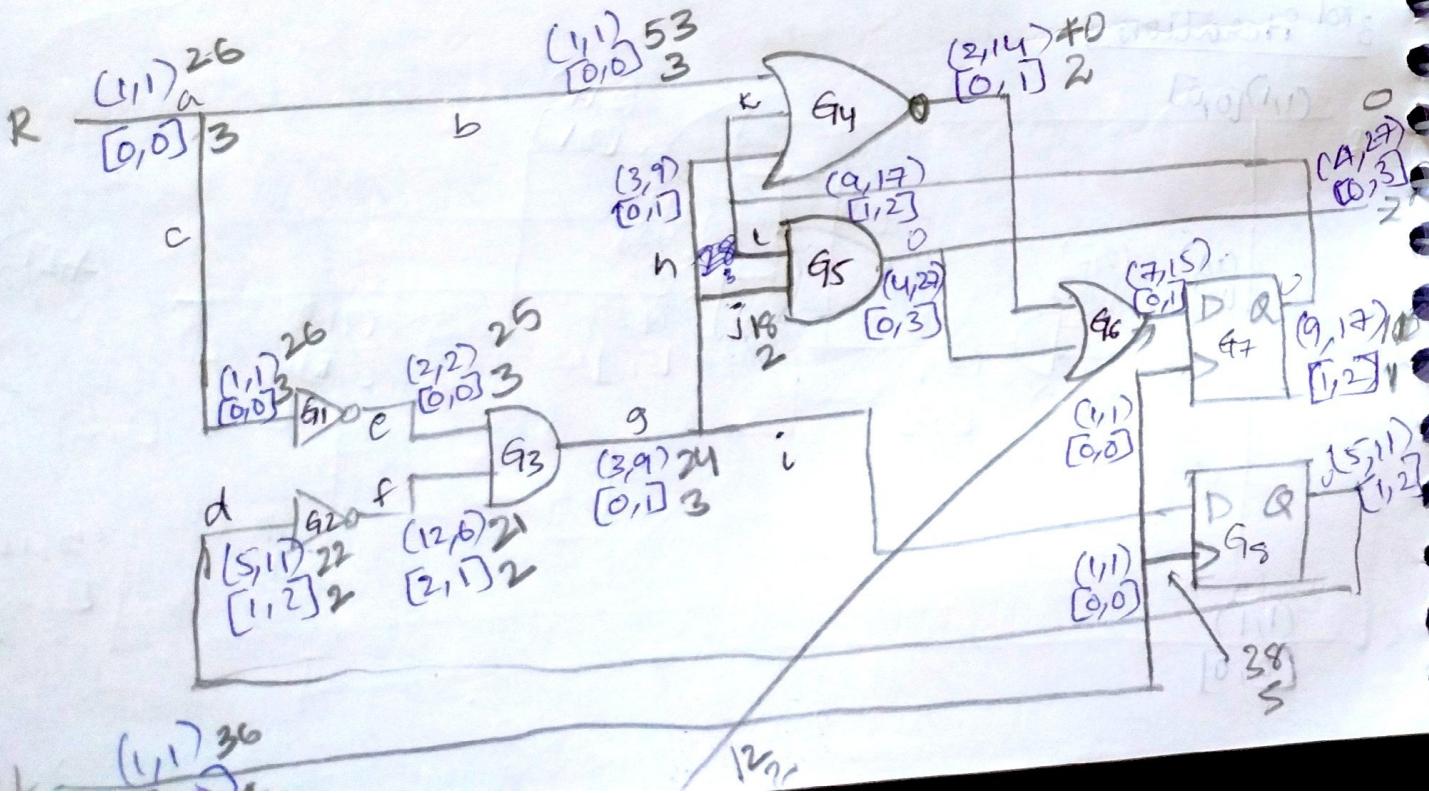
Observability:

$$CO(D) = CO(Q) + CC_1(C) + CC_0(0) + CC_0(Reset)$$

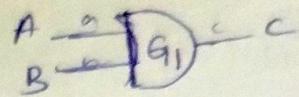
$$SO(D) = SO(Q) + SC_1(C) + SC_0(0) + SC_0(Reset) + 1$$

$$CO(Reset) = CO(Q) + CC_1(Q) + CC_0(0) + CC_1(Reset)$$

$$CO(C) = \min [CO(Q) + CC_0(Reset) + CC_1(C) + CC_0(0) + CC_0(0) + CC_1(0) + CC_1(Q) + CC_1(Reset) + CC_1(C) + CC_0(0) + CC_1(0) + CC_1(Q)]$$



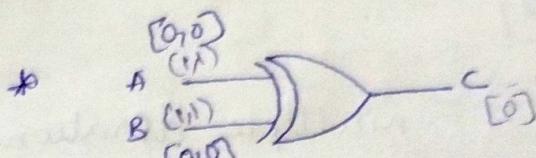
30/10/



$3^3 - 1 = 26 \leftarrow$ multiple stuck
at faults
single stuck at fault = 6

$$CCO(C) = \min(CCO(A_i)) + 1$$

$$CCI(C) = \sum(CCI(A_i)) + 1$$



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

non-controllable

$$CO(A) \Rightarrow \min(C)$$

$$CO(A) = \min(CO(c) + CO(B))$$

$$CO(A) = CO(c) + \min(CCI(B), CCO(B)) + 1$$

$$SC(A) = SC(c) + \min(SCI(B), SCO(B))$$

$$\Rightarrow 0 + (0,0) = 0$$

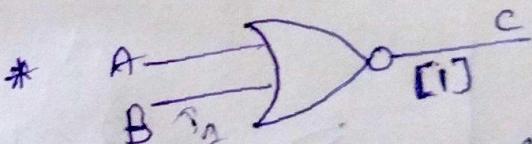
SC's are always initialized with the [0,0]



A	B	C
00	0	0
01	1	1
10	1	1
11	1	1

$$CO(A) = CO(c) + CCO(B) + 1$$

$$CO(B) = CO(c) + CCO(A) + 1$$

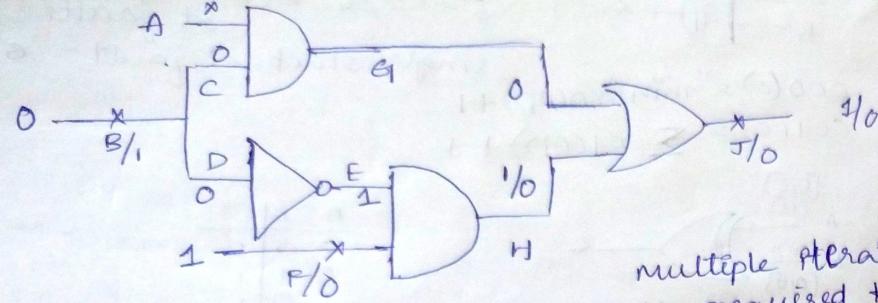


A	B	C
00	0	1
01	1	1
10	1	1
11	1	0

$$CO(A) = CO(c) + \min(CCO(B), CCI(B)) + 1$$

Fault Simulation Techniques

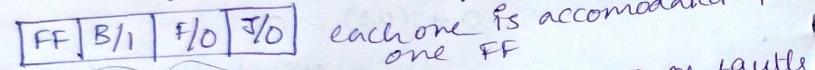
- 1) Serial
- 2) Parallel FST
- 3) Deduction
- 4) Concurrent



$I/O \rightarrow D$ $D \rightarrow D'$
 → only one fault is detected at one time.

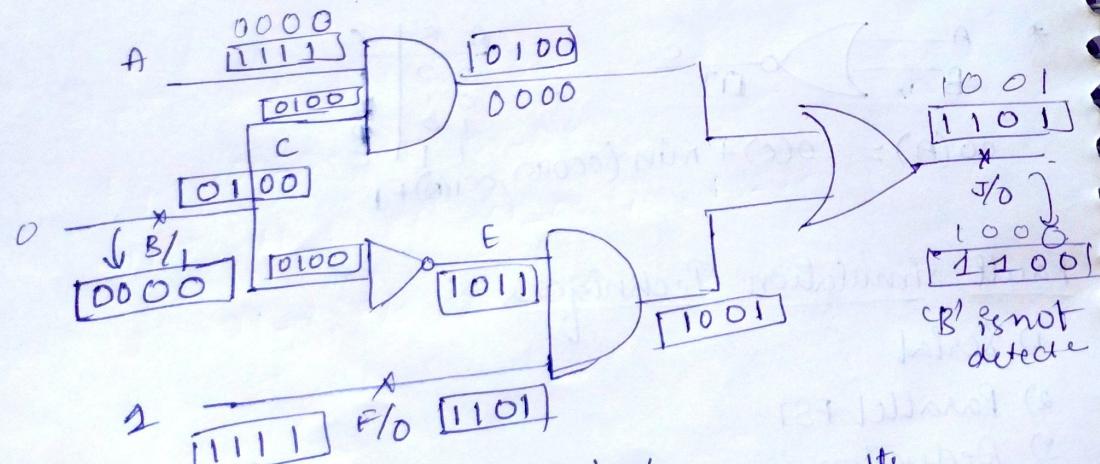
parallel FST

4 bits are reserved for each & every net



→ no. of passes depends on word length & no. of faults
 let's take word length $\rightarrow m$
 no. of faults $\rightarrow n$

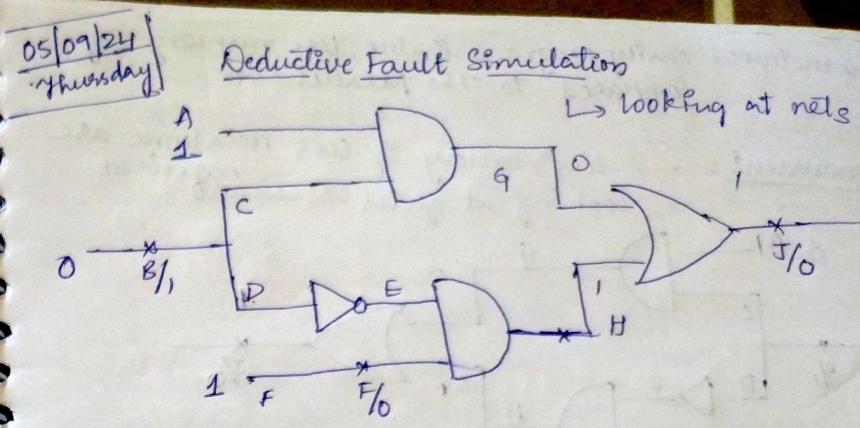
$$\text{No. of pass} = \frac{n}{m-1}$$



A	1	$ $	B/1	0
B	0	$ $	F/O	0
C	1	$ $	J/O	1

all faults are detected after 2 passes.

B' is not detected



$L_A = \emptyset$; → null set \therefore no fault effect is here

$L_B = \{B/1\}$; → only this can be detected at B

$L_F = \{F/O\}$; →

$L_C = L_B = \{B/1\} \subseteq L_D = L_E$

$L_G = L_A + L_C + L_F = \emptyset + \{B/1\} = \{B/1\}$

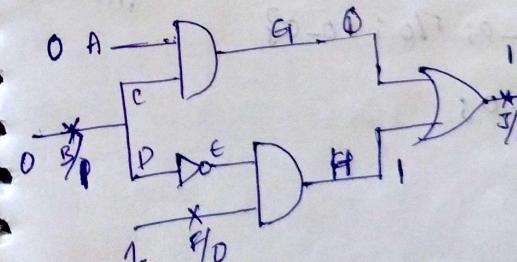
$L_H = L_E + L_F + L_H = \{B/1\} + \{F/O\} = \{B/1, F/O\}$

$L_J = \text{controlling} - \text{non controlling} + L_J$

$\Rightarrow L_H - L_G + \{J/O\}$

$\Rightarrow \{F/O, J/O\}$

If both are non controlling the they will cancel out each other



$L_A = \emptyset$

$L_B = \{B/1\}$

$L_C = L_D = L_E = \{B/1\}$

$L_H = \{B/1, F/O\}$

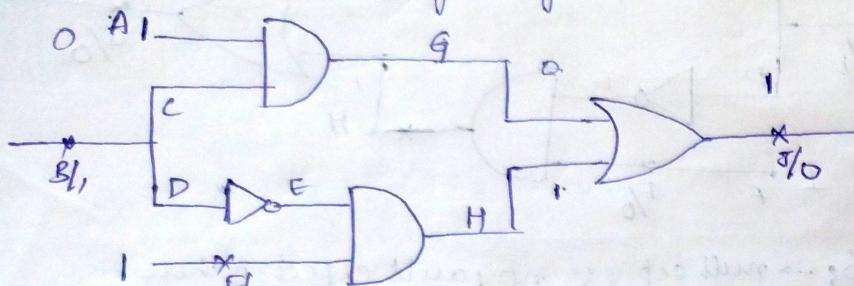
$L_G \Rightarrow$ Both A & C are controlling intersection will be taken

$L_G = \emptyset * \{B/1\} = \emptyset$

$L_J = L_H - L_G + \{J/O\}$
 $= \{B/1, F/O, J/O\}$

deductive \rightarrow easily programmable, less memory req compared to the parallel FST.

concurrent: \rightarrow less memory & less iterations are required
looking at gates



$$L_E = \{0-1; B/1; 1-0\}$$

$$L_G = \{10-0; B/1; 11-1\}$$

$$L_H = \{11-1; B/1; 00-0; F/0; 10-0\}$$

$L_J = \{01-1; B/1; 10-1; F/0; 00-0; J/0; 01-0\}$

This op should not match with remaining op's then only the fault will be detected.

$$L_E = \{0-1; B/1; 1-0\}$$

$$L_G = \{00-0; B/1; 01-0\}$$

$$L_H = \{11-1; B/1; 01-0; F/0; 10-0\}$$

$$L_J = \{01-1; B/1; 01-0;$$

* If 2 are non-controlling add controlling intersection

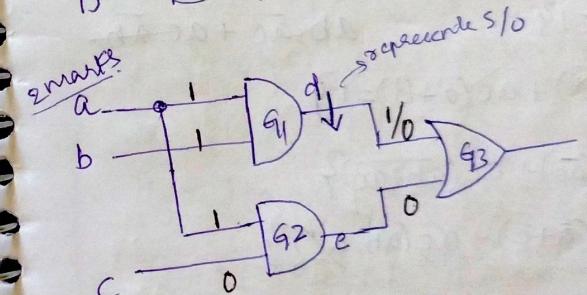
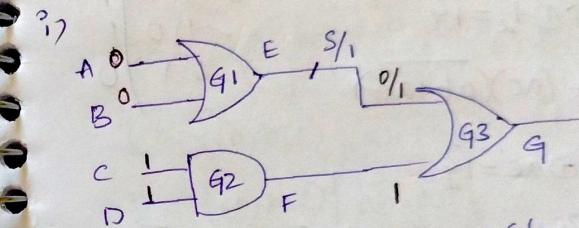
06/09/24 Parallel pattern detection
Friday * Critical Path detection

* Unit-3: Combination Test Generation

Test generation methods

- 1) from truth table
- 2) Using Boolean equation
- 3) Using Boolean difference
- 4) From circuit structure.

(for less marks in exam)



$$f = ab + ac$$

$$f_2 = ac$$

Boolean variables are primary inputs.

$a, b, c = \{0, 1\}$ Boolean set

$(0, 1) \rightarrow$ Range but 0, 1 are excluded

$[0, 1] \rightarrow$ Range (including)

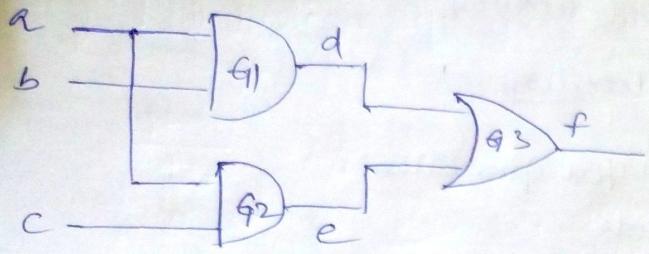
sensitive gates $\rightarrow G_1, G_3$
sensitive nets $\rightarrow E, G$

faulty o/p

abc	f	f ₂
000	0	0
001	0	0
010	0	0
011	0	0
100	0	0
101	1	1
110	1	0
111	1	1

Give o/p

fault is detected



$$f = ab + ac$$

$$f_2 = ac$$

$T_\alpha \rightarrow$ set of all tests for fault α

$$T_\alpha = \text{ON-set}(f) * \text{OFF-set}(f_2) + \text{OFF-set}(f) * \text{ON-set}(f_2)$$

$$\%_{\alpha} T_\alpha = f \cdot f_2' + f' \cdot f_2 = f \oplus f_2 \Rightarrow T_\alpha$$

$$T_\alpha = \{(a, b, c) | f \oplus f_2 = 1\}$$

$$f \oplus f_2 = (ab + ac) \cdot (\bar{ac}) + (ac) \cdot (\bar{ab} + \bar{ac})$$

$$T_\alpha \Rightarrow \{(a, b, c) | (ab + ac) \oplus ac = 1\}$$

$$\Rightarrow T_\alpha = \{(a, b, c) | ab \oplus ac = 1\}$$

$$ab \cdot \bar{ac} + ac \cdot \bar{ab}$$

$$\Rightarrow T_\alpha = \{(a, b, c) | ab(a' + c') + ac(a' + b') = 1\}$$

$$\Rightarrow T_\alpha = \{(a, b, c) | (ab + ac)(\bar{a} + \bar{c}) + ac(ab + bc) = 1\}$$

$$T_\alpha = \{(a, b, c) | (ab + ac)(\bar{a} + \bar{c})\}$$

$$= \{(a, b, c) | ab \cdot \bar{a} \cdot \bar{c}\}$$

$$= \{(a, b, c) | ab(\bar{a} + \bar{c})\}$$

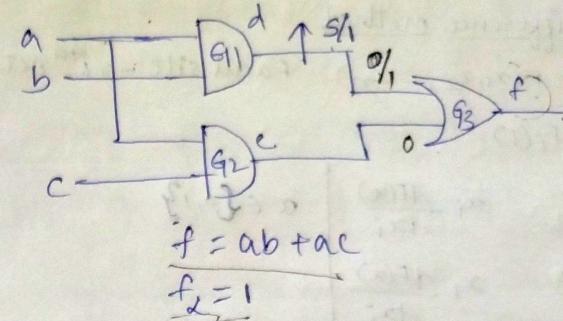
$$= \{(a, b, c) | (ab\bar{a} + abc)\}$$

$$= \{(a, b, c) | abc\}$$

$$ab(\bar{a} + \bar{c})$$

$$ab \cdot \bar{a}$$

$$\bar{a} \cdot \bar{c}$$



$$f = ab + ac$$

$$f_2 = 1$$

$$T_\alpha =$$

$$\rightarrow T_\alpha = f \oplus f_2 = (ab + ac) \oplus 1$$

$$T_\alpha = \{(a, b, c) | (ab + ac)(0) + (\bar{ab} + \bar{ac})\}$$

$$T_\alpha = \{(a, b, c) | (\bar{ab} + \bar{ac})\}$$

$$T_\alpha = \{(a, b, c) | \bar{ab} \cdot \bar{ac}\}$$

$$T_\alpha = \{(a, b, c) | \bar{ab} \cdot (\bar{a} + \bar{c})(\bar{a} + b)\}$$

$$T_\alpha = \{(a, b, c) | (\bar{a} + \bar{c})\bar{a} + (\bar{a} + \bar{c})b\}$$

$$T_\alpha = \{(a, b, c) | \bar{a} \cdot \bar{a} + \bar{a} \cdot \bar{c} + \bar{a} \cdot b + \bar{b} \cdot \bar{c}\}$$

$$T_\alpha = \{(a, b, c) | \bar{a} \cdot \bar{a} (b + \bar{b})(c + \bar{c}) + \bar{a} \cdot \bar{c} (b + \bar{b}) + \bar{a} \cdot \bar{b} (c + \bar{c}) + \bar{b} \cdot \bar{c} \\ \bar{a} \cdot \bar{a} b + \bar{a} \cdot \bar{a}\}$$

$$T_\alpha = \{(a, b, c) | \bar{a} + \bar{b} \bar{c} = 1\}$$

$$T_\alpha = \{(0x0), (x00)\}$$

abc	f	f ₂
000	0	1
001	0	1
010	0	1
011	0	1
100	0	1
101	1	1
110	1	1
111	1	1

Wednesday (iii) Boolean difference method

$F(x) = F(x_1, x_2, \dots, x_n)$ Fault site $\rightarrow i^{\text{th}}$ net

$\frac{dF(x)}{dx_i} = F_i(0) \oplus F_i(1)$

stuck at '1' $x_i/1$ $\overline{x_i} \frac{dF(x)}{dx_i}$ $\alpha \in \{0, 1\}$
 " " "0" $x_i/0$ $x_i \frac{dF(x)}{dx_i}$

$f(a, b, c) = ab + ac$
 $f(a=0) = 0$
 $f(a=1) = b + c$

$\frac{df}{da} = f(a=0) \oplus f(a=1)$
 $\Rightarrow b + c$

$\frac{dF(x)}{dx_i} = F_i(0) \oplus F_i(1)$ $a/1$ $T_x = \{ (a, b, c) \mid \overline{a} \frac{dF}{da} = 1 \}$
 $a/0$ $T_B = \{ (a, b, c) \mid a \frac{dF}{da} = 1 \}$

$s/1 \Rightarrow (b+c)\overline{a} = 1$
 $\Rightarrow \overline{a}b + \overline{a}c = 1$

$s/0 \Rightarrow a(b+c) = 1$
 $ab + ac$

fault site = h
 $f(a, b, c) = ab + ac$
 $f(h=0) = ac$
 $f(h=1) = 1$

$\frac{df}{dh} = f(h=0) \oplus f(h=1)$
 $= ac \oplus 1 \Rightarrow \overline{ac} = \overline{a} + \overline{c}$

$T_x = \{ (a, b, c) \mid \overline{h} \frac{df}{dh} = 1 \}$
 $T_B = \{ (a, b, c) \mid h \frac{df}{dh} = 1 \}$

$s/1 \Rightarrow (\overline{a} + \overline{c})\overline{ab} = 1$
 $(\overline{a} + \overline{ab}) + \overline{c} \cdot \overline{ab}$
 $\Rightarrow (\overline{a} + \overline{c})(\overline{a} + b) \Rightarrow \overline{a} \cdot \overline{a} + \overline{a} \cdot \overline{c} + \overline{c} \cdot b + \overline{ab}$

$s/0 \Rightarrow T_B = (\overline{a} + \overline{c})ab = 1$
 $\overline{a} \cdot ab + \overline{c} \cdot ab \approx \overline{c} \cdot ab$

$T_x = s/1 \Rightarrow (\overline{a} + \overline{c})\overline{ab} = 1$
 $T_x \Rightarrow (\overline{a} + \overline{c})(\overline{a} + b) = 1$
 $\overline{a} \cdot \overline{c} \Rightarrow \overline{a} + \overline{b} \cdot \overline{c} = 1$

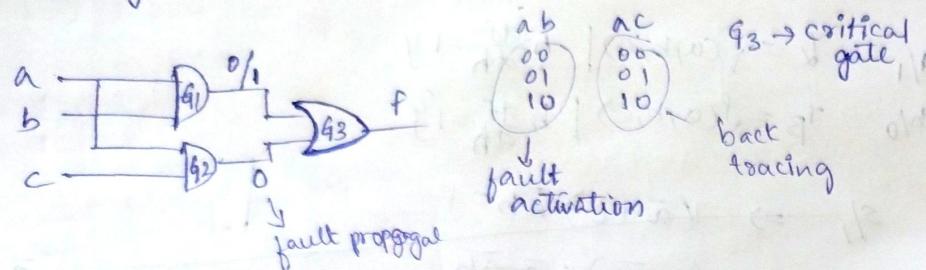
$T_x = \{ (0xx), (x00) \}$

i) from circuit structure

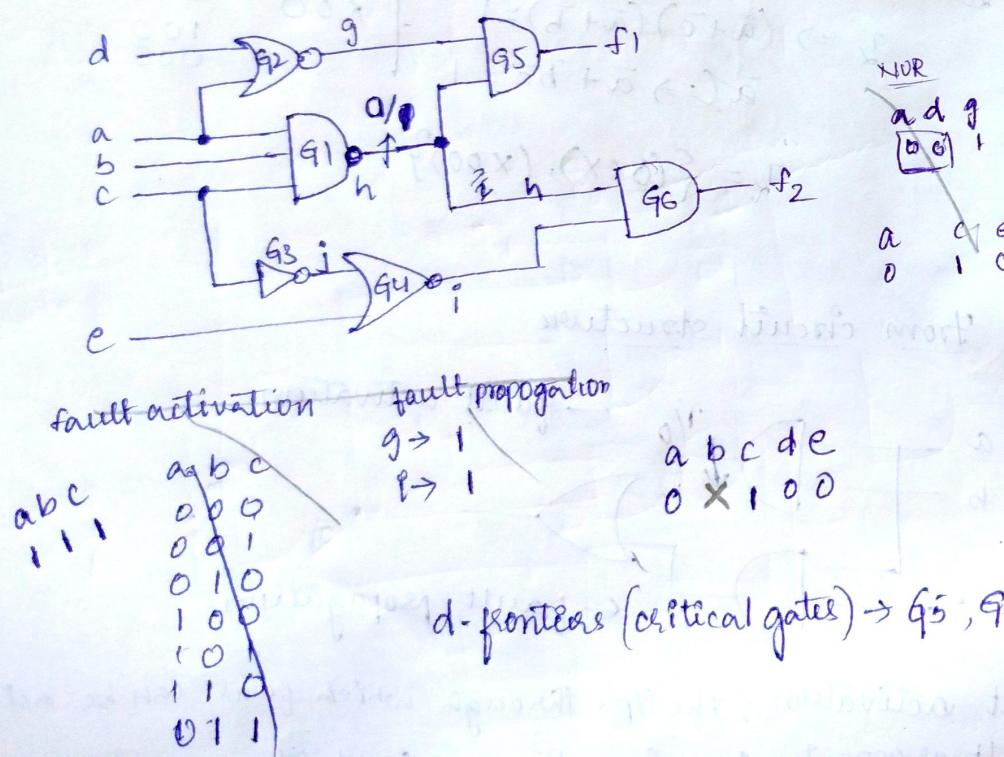
fault activation : the 1/p's through which fault can be activated
 fault propagation : seeing the effect at 0/p

one justification:

Back tracing: all other i/p's of critical gates are non-controlled.



Decisions when fault propagation



fault activation fault propagation

$$\begin{array}{ccc} a & b & c \\ 1 & 1 & 1 \end{array} \quad \begin{array}{c} g \rightarrow 1 \\ i \rightarrow 1 \end{array}$$

back tracing for 96 goal \Rightarrow $h=1$ $j=0$
 $i=1$ $e=0$

$f_1 \rightarrow g_5 \rightarrow g_2 \rightarrow d \rightarrow$ This path is inconsistent

* a is already 1 so the o/p of G2 can never be going to 0

a b c d e
| | | x o

D-cube : A +

<u>AND</u>	<u>A · B</u>	0	1	D'	D
a		0	0	0	0
i		0	1	D'	D
D'		0	D'	D'	0
D		0	D	0	D

$A+B$	0	1	B'	D
0	0	1	D'	D
1	1	1	1	1
B'	D'	1	D	
D	D	1	1	1

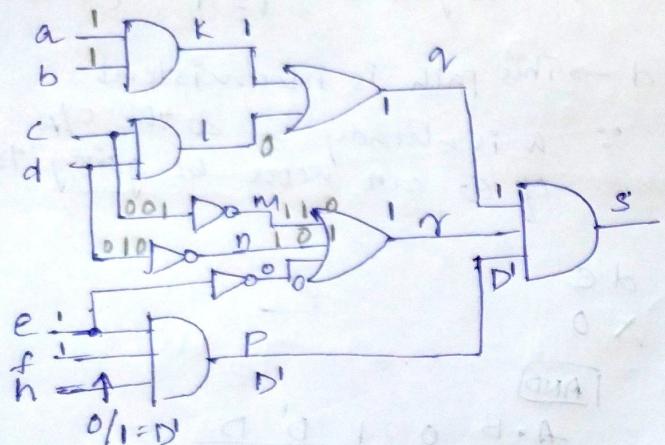
Implications: computation of the values that can be uniquely determined.

Global
local

fwd } non-controlling
bwd } IP to propagate

→ d-frontiers: the gates through which the fault is getting passed.

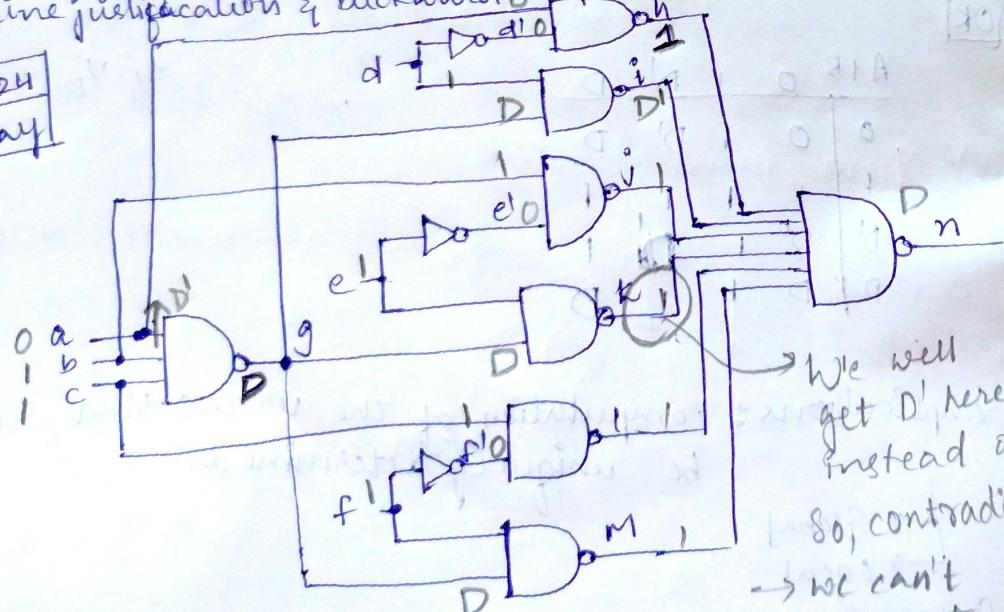
Decisions when line justifications



J-frontier: The set of all gates whose output value is known but is not implied by $\frac{1}{4}P$ values.

helpful for line justification & backward implication.

13/09/24
Today



We will get D' here instead of 1
so, contradiction
→ we can't propagate fault through i_2

$\lceil a/1 \rceil \rightarrow$ fault

a b c
0 1 1
rev of fault non-controlling

we want to propagate the fault through i_2

$$\text{so;} \quad \begin{aligned} & n \oplus k \mid m \\ & (1 \cdot 1 \cdot 1 \cdot D' \cdot 1 \cdot D') = D \\ & (1 \cdot D \cdot 1 \cdot D \cdot 1 \cdot D) = D \end{aligned}$$

↓ There is contradiction at K

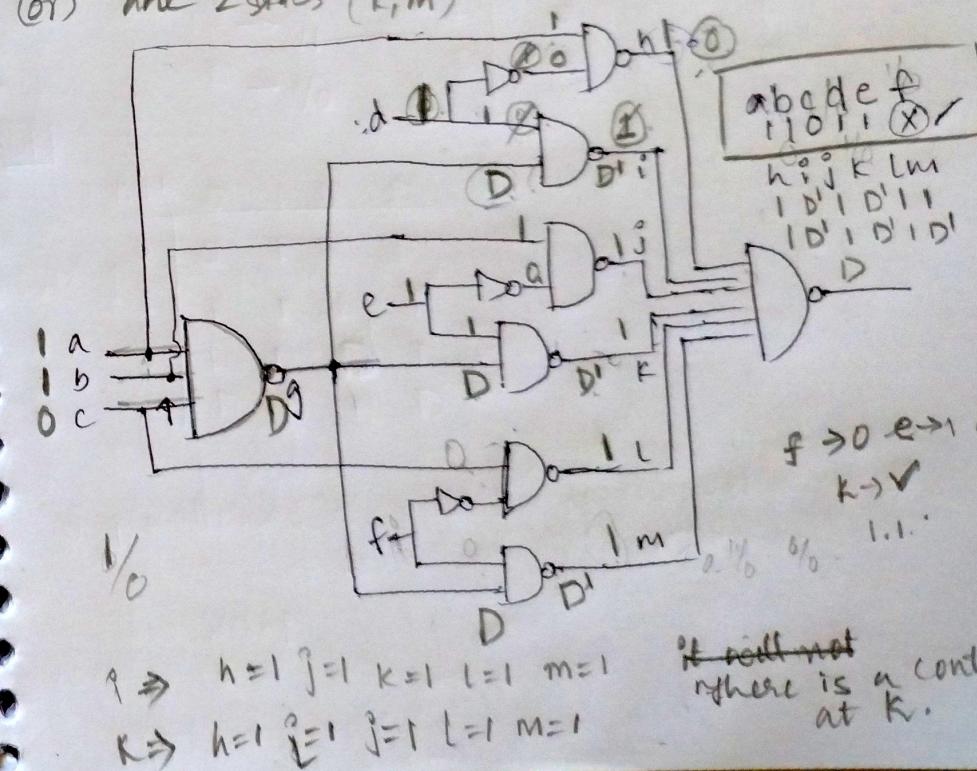
$$\begin{aligned} d \Rightarrow 1 & \quad i \Rightarrow D' \\ d \Rightarrow 0 & \quad i \Rightarrow 1 \end{aligned}$$

Test vectors

$$\begin{array}{ll} abc \& def \\ 011 & 111 \end{array} \rightarrow 011X11$$

While propagating through the k ,
there is a contradiction at m

so, we will take the fault through all the 3 sites
(or) the 2 sites (k, m)



It will not
there is a cont.
at K.