# Bihar Engineering University, Patna
## Special Examination – 2023

***Course: B.Tech.*** ***Time: 03 Hours***

***Code: 100403*** ***Subject: Digital Electronics*** ***Full Marks: 70***

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***Instructions:-***

*(i) The marks are indicated in the right-hand margin.*

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

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***Q.1*** ***Answer any seven question only:*** **[2 x 7 = 14]**

(a) Define Dynamic RAM.

(b) The resolution of a 10-bit AD converter for an input range of 10 V is approximately_____.

(c) The parameter through which 16 distinct values can be represented is known as _____.

(d) Define Multiplexing.

(e) Write the significance of Truth table.

(f) Write the differences between Combinational and Sequential circuit.

(g) A hexadecimal odometer displays F52F. The next reading will be_____.

(h) The basic property of Sequential circuit is _____.

(i) How many entries will be in the truth table of a 4-input NAND gate?

(j) What is Dual Slope ADC?

***Q.2*** What are weighted, non-weighted, cyclic and self-complementary codes? Explain each with examples. **[14]**

***Q.3*** Design a BCD to 7-segment display decoder circuit using logic gates. **[14]**

***Q.4*** Design a 3-bit parallel comparator A/D convertor that provides output in 2's complement format. **[14]**

***Q.5*** Design full adder using the following: **[14]**

(i) 8:1 mux

(ii) 4:1 mux

***Q.6*** What is binary shift register? Write down their application. **[14]**

***Q.7*** Minimize the following expression using k-map **[14]**

$f(P, Q, R, S) = \Sigma m(0,1,4,5,7,12,13)$

***Q.8*** Describe the procedure to design Mod-6 counter. **[14]**

***Q.9*** Write short notes on any two of the following **[7x2=14]**

(i) RAM (ii) ROM (iii) CMOS logic

(iv) Operation of TTL logic circuit working as NAND Gate

# Bihar Engineering University, Patna
## End Semester Examination -2023

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|---|---|---|
| ***Course: B.Tech*** | ***Semester: IV*** | ***Time: 03 Hours*** |
| ***Code: 100403*** | ***Subject: Digital Electronics*** | ***Full Marks:70*** |

***Instructions:-***

*(i) The marks are indicated in the right-hand margin.*
*(ii) There are **NINE** questions in this paper.*
*(iii) Attempt **FIVE** questions in all.*
*(iv) Question No. **1** is compulsory.*

***Q.1*** ***Answer any seven Question only:*** **[2 x 7 = 14]**

(a) Convert the Decimal number (108.025) to their binary equivalent.
(b) Draw Truth table of JK flip flop.
(c) Draw the truth table and logic circuit of Half-adder.
(d) Write the difference between combinational & Sequential circuit.
(e) Draw timing diagram of SR flip-flop.
(f) Find 2's complement of 1011011.
(g) Number of 2:1 mux requires designing 256:1 mux is ……
(h) Add hexadecimal number 2ABC & 98F2.
(i) Discuss Universal gates.
(j) What is the use of K-map?

***Q.2*** Implement the following function using only NAND gate **[14]**
F(A,B,C)=$\sum m(0,1,2,3,7)$.

***Q.3*** (a) Realize XNOR logic function using NAND gate only. **[7]**
(b) Simplify Y= ABC + AB$\overline{C}$ +A$\overline{B}$C **[7]**

***Q.4*** A logic circuit has four inputs A,B,C,D and output Y. Y=1 when A & B are both 1,subjected to the condition that C and D are both low or both high. Design the logic circuit. **[14]**

***Q.5*** Explain Master-slave flip flop. What are race around condition?. How it can be circumvented with the help of Master-slave flip flop. **[14]**

***Q.6*** (a) Design 8 to 3 line Encoder circuit. **[7]**
(b) Implement NAND gate using TTL logic family. **[7]**

***Q.7*** Summarize the design procedure for a synchronous sequential circuit. **[14]**

***Q.8*** (a) Explain the working of R-2R Ladder DAC. **[7]**
(b) Design 3-bit binary counter using T flip-flop. **[7]**

***Q.9*** Write short notes on the following: **[7*2=14]**
(a) Binary Parallel Adder
(b) Digital IC logic families

# Code : 100403

## B.Tech 4th Semester Exam., 2022

( New Course )

## DIGITAL ELECTRONICS

*Time* : 3 hours *Full Marks* : 70

*Instructions* :

*(i) The marks are indicated in the right-hand margin.*

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

**1.** Answer any *seven* of the following : 2×7=14

*(a)* What is the next number in the following octal counting sequence?

724, 725, 726, 727, _____

*(b)* What do you mean by a positive logic system and a negative logic system?

*(c)* Subtract using 9's complement :

745.81 – 436.62

(d) The following operation is correct for at least one number system. Find the correct number system :

$$1234 + 5432 = 6666$$

(e) What is a tri-state logic?

(f) Which are the fastest logic family and the slowest logic family?

(g) Which memory technology needs the least power?

(h) What is a register? What is a shift register?

(i) What is a master-slave flip-flop?

(j) Fill in the blank :

$$(100101000111)_{(BCD)} = (\_\_\_\_\_)_{10}$$

**2.** (a) Which of the following are analog quantities and which are digital?

Number of atoms in a sample of material, Altitude of an aircraft, Pressure in a bicycle tire, Current through a speaker, and Timer setting on a microwave oven.

(b) What do you mean by self-complementing code? Write two self-complementing codes.

(c) If the waveforms $A$ and $B$ shown in Fig. 1 are applied to a two-input XOR gate, determine the output waveform :

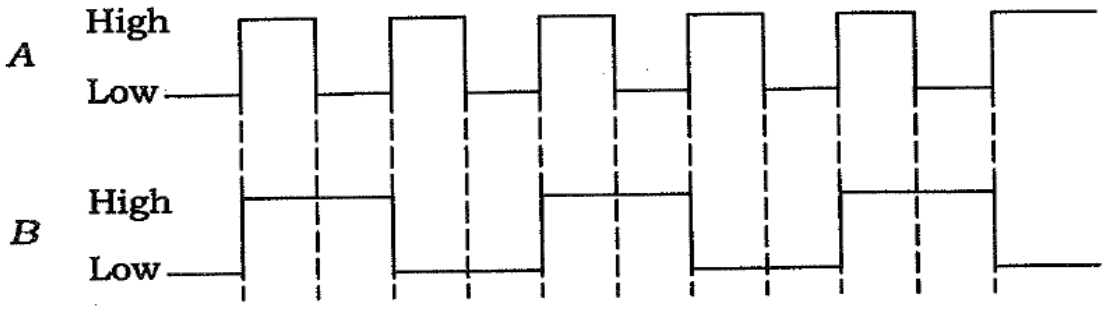


Fig. 1

4+4+6

3. (a) Perform the following in excess-3 code using the 10's complement method :

$$239 - 597$$

(b) Design and implement a 4-bit binary to Gray converter.

(c) Reduce the following expression using K-map and implement it in AOI logic as well as in NOR logic :

$$F = \Pi M(0, 1, 2, 3, 4, 7)$$

5+4+5

**4.** *(a)* Reduce the following expression and implement it using universal logic gate :

$$\Sigma m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

*(b)* Use a multiplexer to implement the logic function $F = A \oplus B \oplus C$. 7+7

**5.** *(a)* Determine the *Q*-output waveform if the inputs shown in Fig. 2 are applied to the gated *D*-latch which is initially RESET :

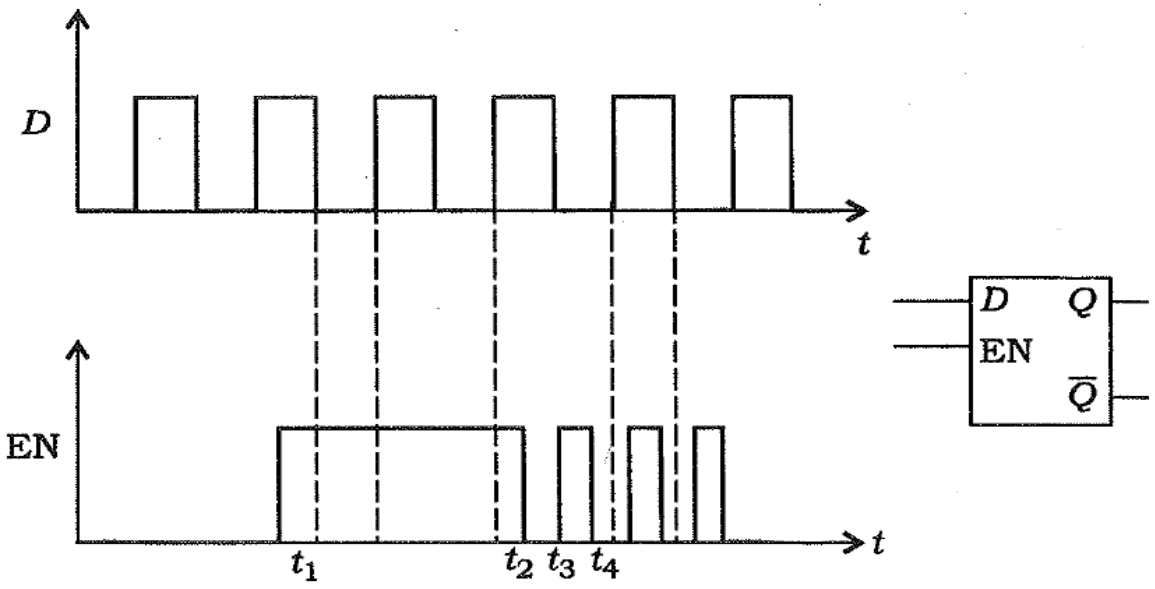


Fig. 2

*(b)* Design the conversion circuit for *S-R* flip-flop to *J-K* flip-flop. 7+7

**6.** *(a)* What is basic difference between a counter and a shift register?

*(b)* With neat diagrams, explain the working of the following types of shift registers :

*(i)* Serial-in, serial-out

*(ii)* Serial-in, parallel-out

*(c)* Design and implement a mod-10 asynchronous counter using *T* flip-flops.

3+6+5

**7.** *(a)* Design and implement a synchronous 3-bit up/down counter using *J-K* flip-flops.

*(b)* Determine the resolution of—

*(i)* 6-bit DAC;

*(ii)* 12-bit DAC

in terms of percentage.

*(c)* What is the resolution of a 9-bit DAC which uses a ladder network? What is this resolution expressed as a percentage? If the full-scale output voltage of this converter is +5 V, what is resolution in volts?

5+4+5

**8.** *(a)* For the 4-bit weighted resistor DAC shown in Fig. 3, determine the—

*(i)* weight of each input bit if the inputs are 0 V and 5 V;

*(ii)* full-scale output if $R_f = R = 1\,k\Omega$.

Also, find the full-scale output if $R_f$ is changed to 500 Ω :

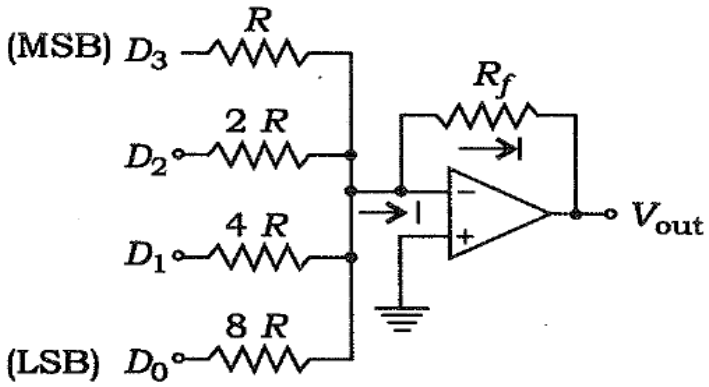


Fig. 3

*(b)* What is a PLD? What do '×' and 'dot' represent on a PLD diagram? 9+5

**9.** *(a)* What are the different technologies used for the fabrication of ROM memories? Determine how many 16K × 4 memory circuits would be required to construct each of the following memories :

*(i)* 256K × 8

*(ii)* 128K × 16

*(b)* Define Memory cell, Address and Byte.

*(c)* Using the simplified connection format of a PLA, show how an $8 \times 1$ PROM should be programmed to implement the logic function

$$F = \Sigma m(1, 4, 5, 7) \qquad 4\frac{1}{2}+4\frac{1}{2}+5$$

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# Bihar Engineering University, Patna

## B.Tech 4th Semester Examination, 2024

*Course: B.Tech*
*Code: 100403*

*Subject: Digital Electronics*

*Time: 03 Hours*
*Full Marks: 70*

***Instructions: -***

*(i) The marks are indicated in the right-hand margin.*
*(ii) There are **NINE** questions in this paper.*
*(iii) Attempt **FIVE** questions in all.*
*(iv) Question No. 1 is compulsory.*

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***Q.1*** ***Answer of the following questions (any seven only):-*** **[2 x 7 = 14]**

(a) What is the use of K-map?
(b) Discuss Universal gates.
(c) Add hexadecimal number 2ABC & 98F2.
(d) Number of 2:1 mux requires designing 256:1 mux is .....
(e) Find 2's complement of 1011011.
(f) What is the function of a sample-and-hold circuit?
(g) Define term propagation delay.
(h) Define race around condition in JK flip flop.
(i) What is the purpose of expanding memory size?
(j) Differentiate between ROM and RAM.

***Q.2*** (a) Realize XNOR logic function using NAND gate only. **[7]**
(b) Simplify $Y = ABC - AB\bar{C} - A\bar{B}C$ **[7]**

***Q.3*** A logic circuit has four inputs A,B,C,D and output Y. Y=1 when A & B are both 1,subjected to the condition that C and D are both low or both high. Design the logic circuit. **[14]**

***Q.4*** (a) Design 8 to 3 line Encoder circuit. **[7]**
(b) Implement NAND gate using TTL logic family. **[7]**

***Q.5*** (a) Design a parallel-to-serial converter using shift registers and explain its operation. **[7]**
(b) Compare the characteristics and applications of JK and T flip-flops. **[7]**

***Q.6*** (a) Explain the working principle of an R-2R ladder DAC with a detailed diagram. **[7]**
(b) Design a 3-bit flash ADC and explain its working with an example. **[7]**

***Q.7*** (a) Find the Simplified logical expression for Y. **[7]**
Y (A, B, C, D, E) = $\sum$m (0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)
(b) Summarize the design procedure for a synchronous sequential circuit. **[7]**

***Q.8*** (a) Implement S-R, T, D flip-flops using J-K flip-flop. Also show the implementation with help of State Tables. **[7]**
(b) Discuss the organization and operation of content-addressable memory (CAM). **[7]**

***Q.9*** Write short notes on the following: **[7x2=14]**
(a) Binary Parallel Adder
(b) Digital IC logic families