Lab 3 PreLab

By Alp Tatar (300241739) and Fahmi Sajid Ahmed (300250180)

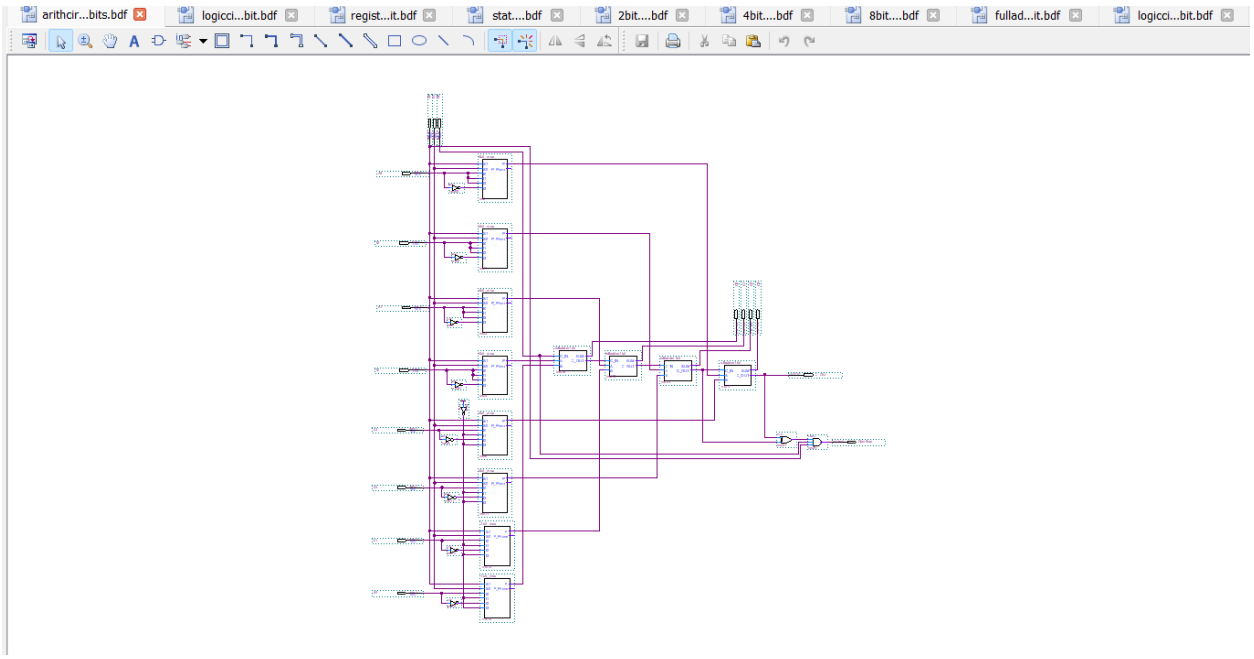
5.4 AC Circuit Design Truth Table

S2	S1	S0	op1	op2	Cy_in	CA output
0	0	0	A	B	0	CA <= A + B
0	0	1	A	B	1	CA <= A + B + 1
0	1	0	A	0	0	CA <= A
0	1	1	A	0	1	CA <= A + 1
1	0	0	A	B’	0	CA <= A + B’
1	0	1	A	B’	1	CA <= A + B’ + 1
1	1	0	A’	0	0	CA <= A’
1	1	1	A’	0	1	CA <= A’ + 1

KMap for Cy_in

S1S0	00	01	11	10
S2				
0	0	1	1	0
1	0	1	1	0

Cy_in = S0



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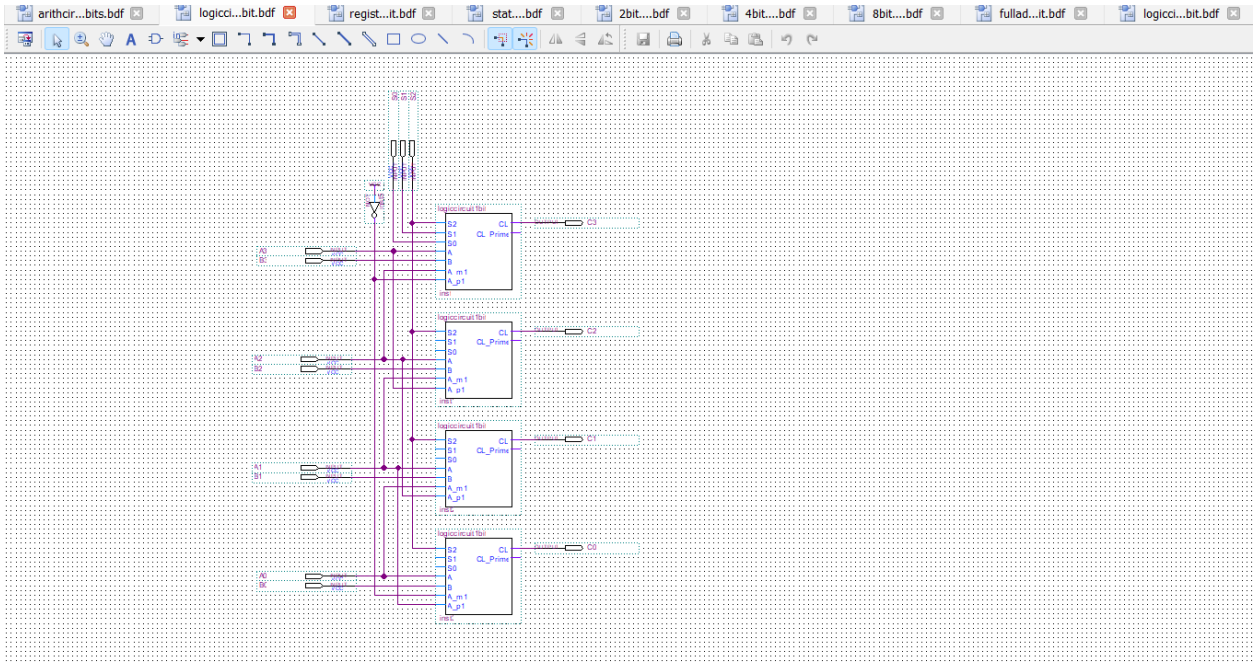
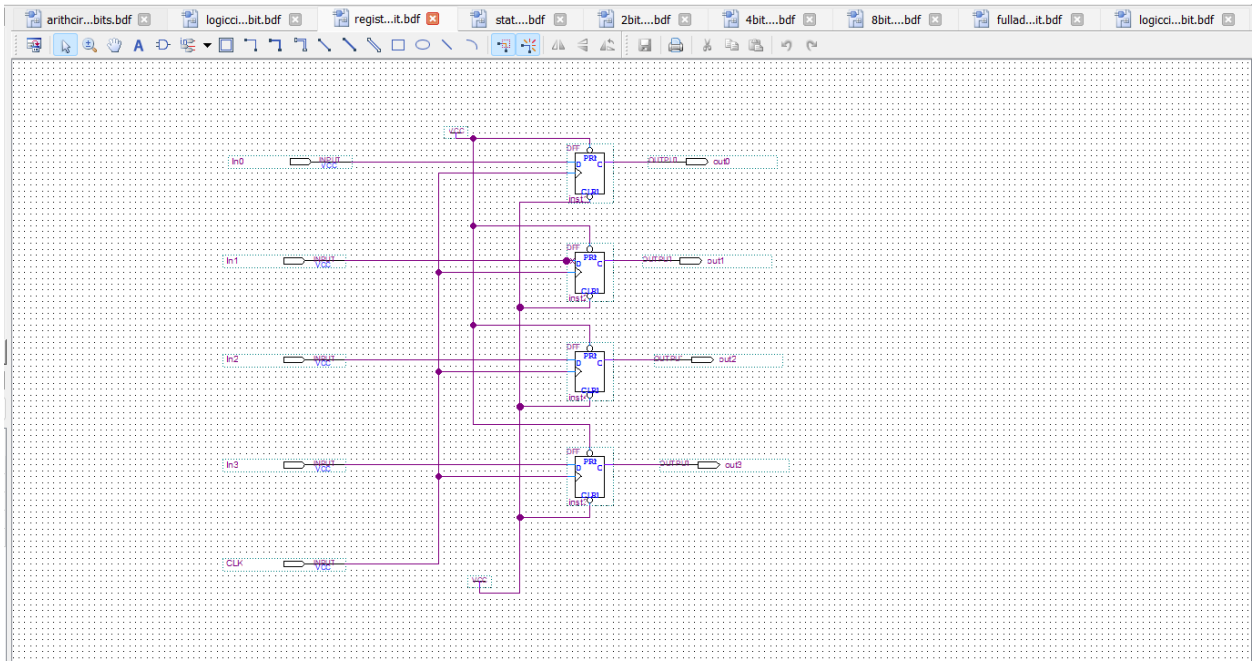
Arithmetic Circuit 4 Bit



Logic Circuit 4 Bit



4-Bit Register

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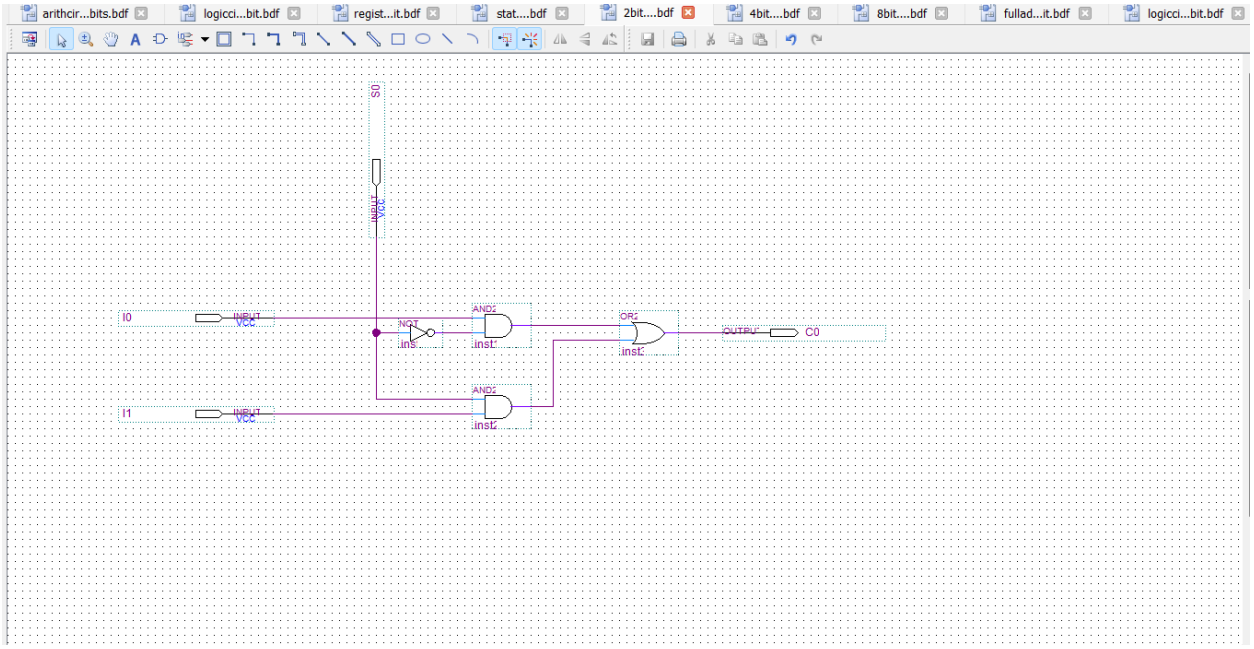
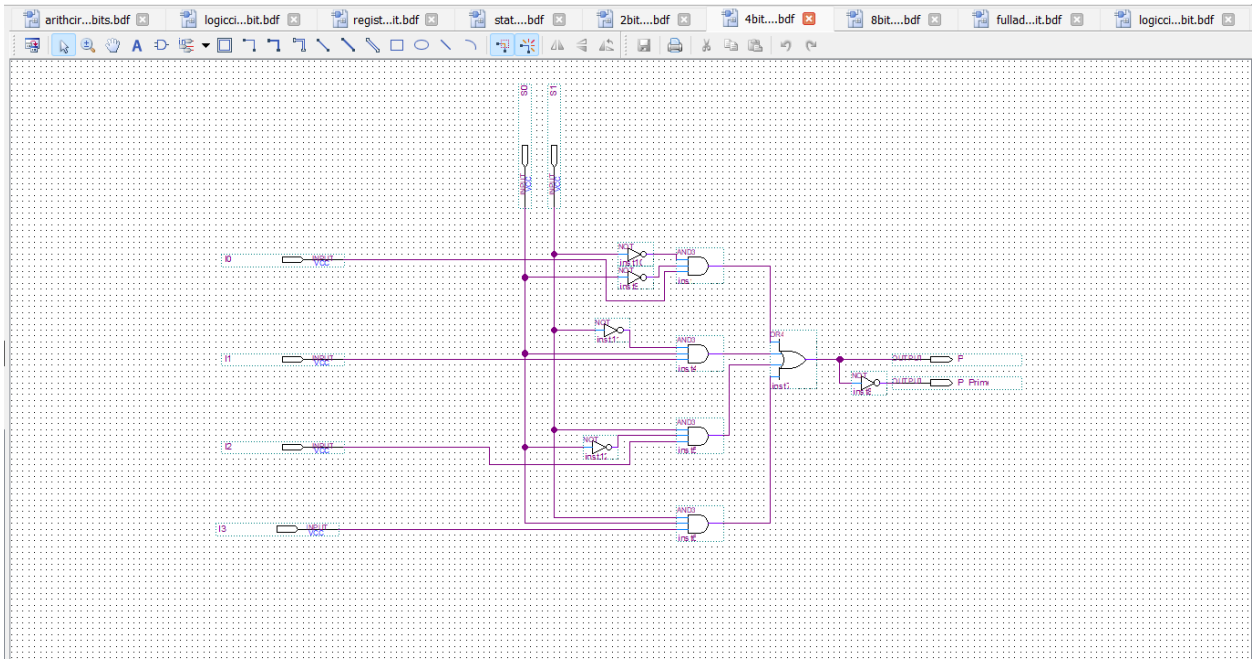


2-Bit MUX



4-Bit MUX

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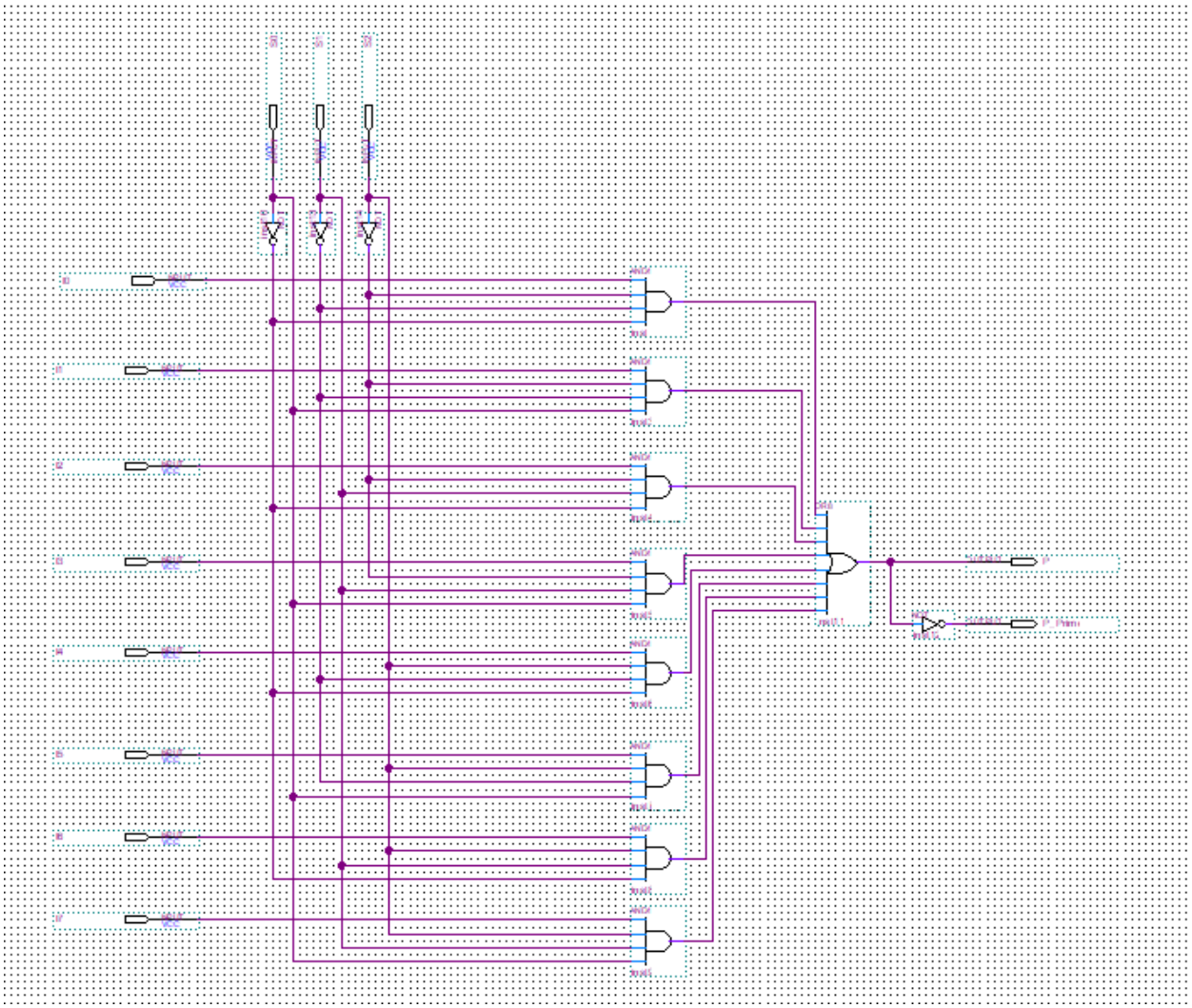
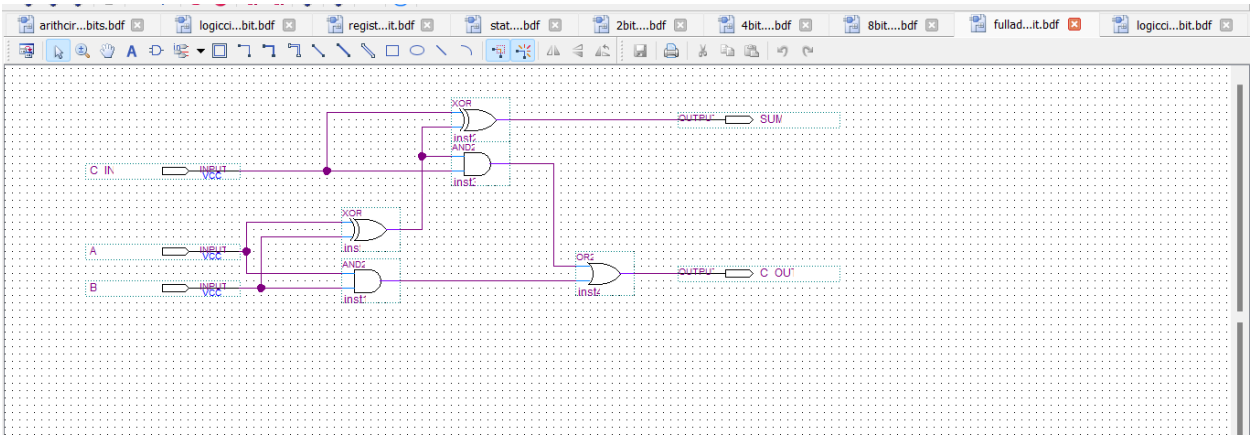


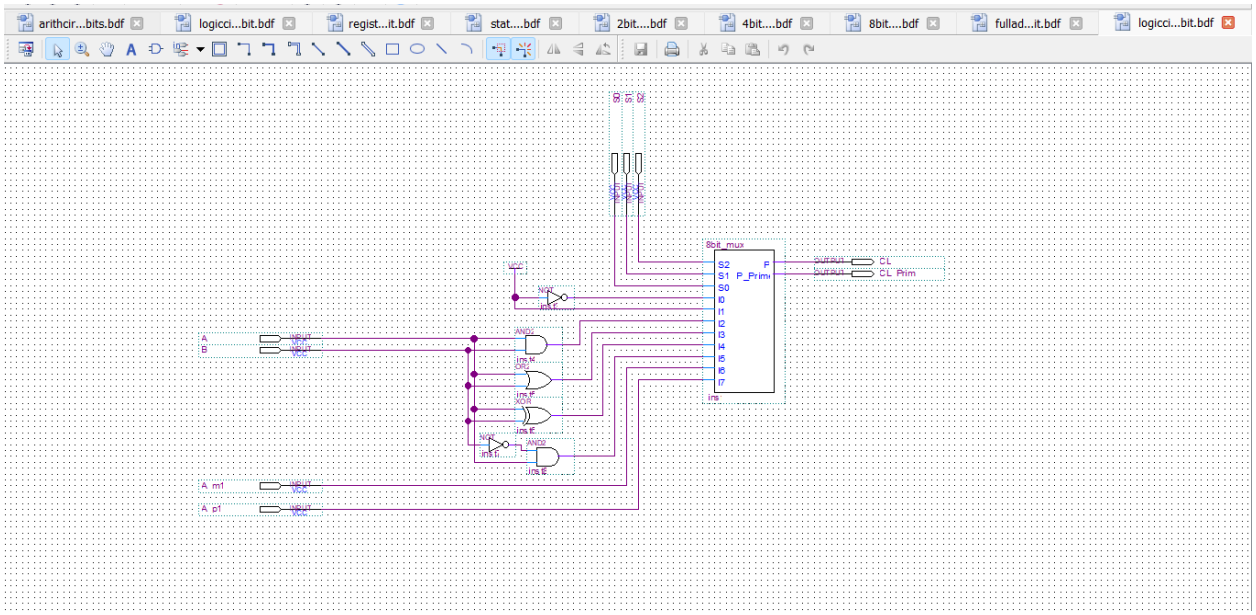
8-Bit MUX



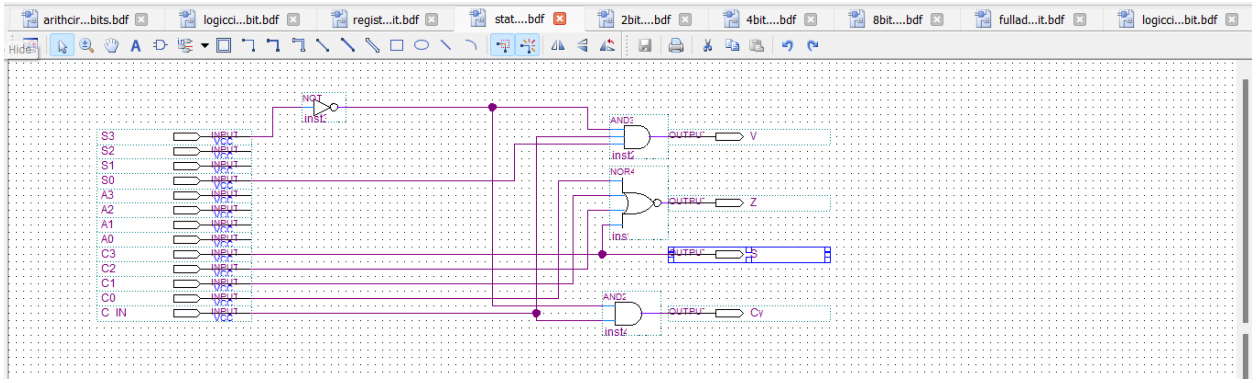
1 Bit Full Adder

Lab 3 PreLab

By Alp Tatar (300241739) and Fahmi Sajid Ahmed (300250180)



1 Bit Logic Circuit



State Indicator