

# **Assignment 3: Digital Simulation for Assignment 2 Using Multisim**

**ELG 3136**

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## Introduction

The cascade amplifier circuit is a fundamental electronic circuit employed for signal amplification. This circuit is the same as the one used in a previous assignment, and its performance plays a crucial role in amplifying a given input signal. The assignment at hand entails the comprehensive design and construction of this cascode amplifier circuit, inclusive of its DC biasing circuitry and coupling capacitors, using the MultiSim simulation software.

To achieve the desired functionality of this cascode amplifier circuit, it is imperative to consider the following important aspects during construction. Proper biasing of both transistors in the saturation mode is essential. This necessitates the introduction of biasing DC sources and resistive networks. An AC sinusoidal source with a  $1\mu\text{V}$  peak-to-peak (pk-pk) amplitude and a 1kHz frequency serves as the input signal to be amplified. Capacitors are positioned at both the input and output of the circuit. The input capacitor couples the AC input source to the circuit while isolating the DC bias source. The output capacitor, on the other hand, filters the AC signal while blocking the DC component from the output node. Care must be taken to select appropriate capacitance values that do not interfere with the circuit's primary function, which is to amplify a 1kHz frequency signal. To facilitate measurement and comparison of input and output voltages, oscilloscopes are integrated into the circuit. This setup enables the visualization of both signals on a single display. In order to achieve successful simulation results that adhere to the specified circuit requirements (as indicated in Figure 1), adjustments to the parameters of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) within the circuit are required.

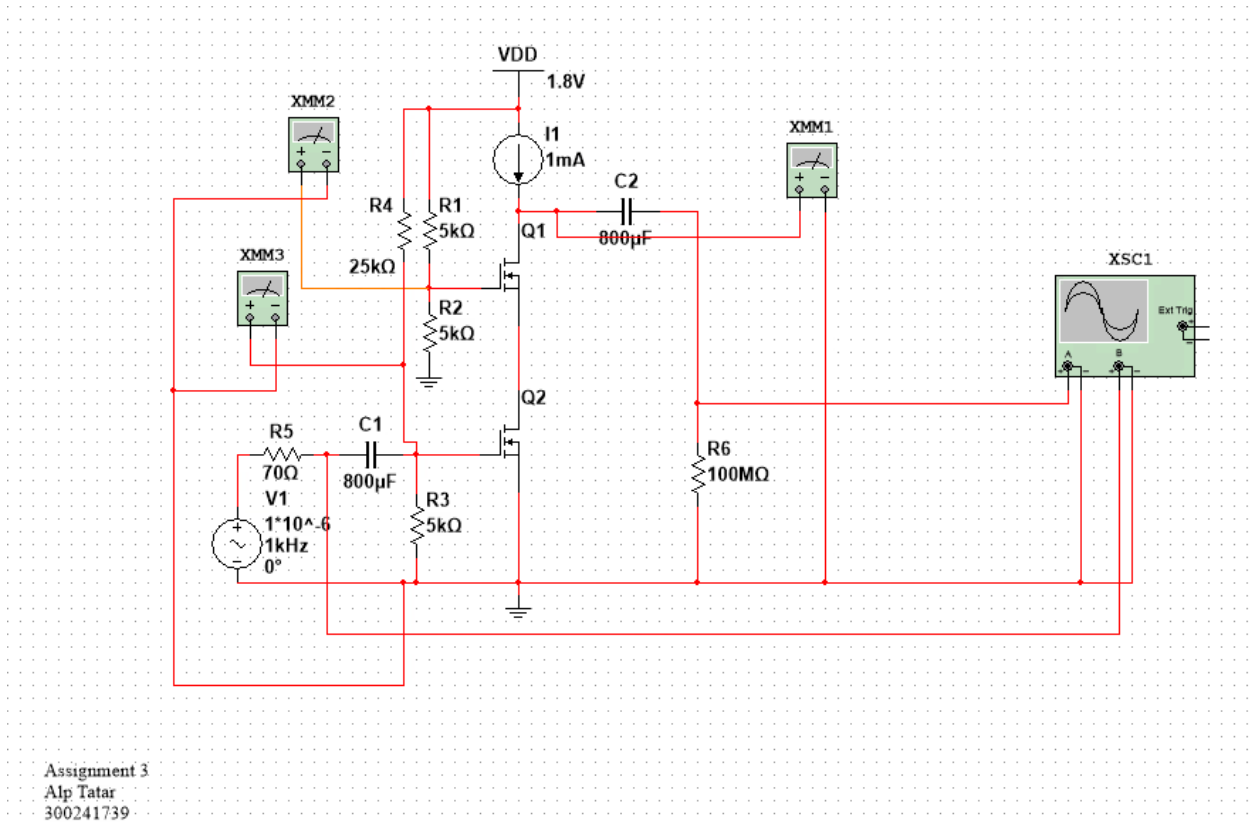


Figure 1: Design of Circuit From Assignment 2

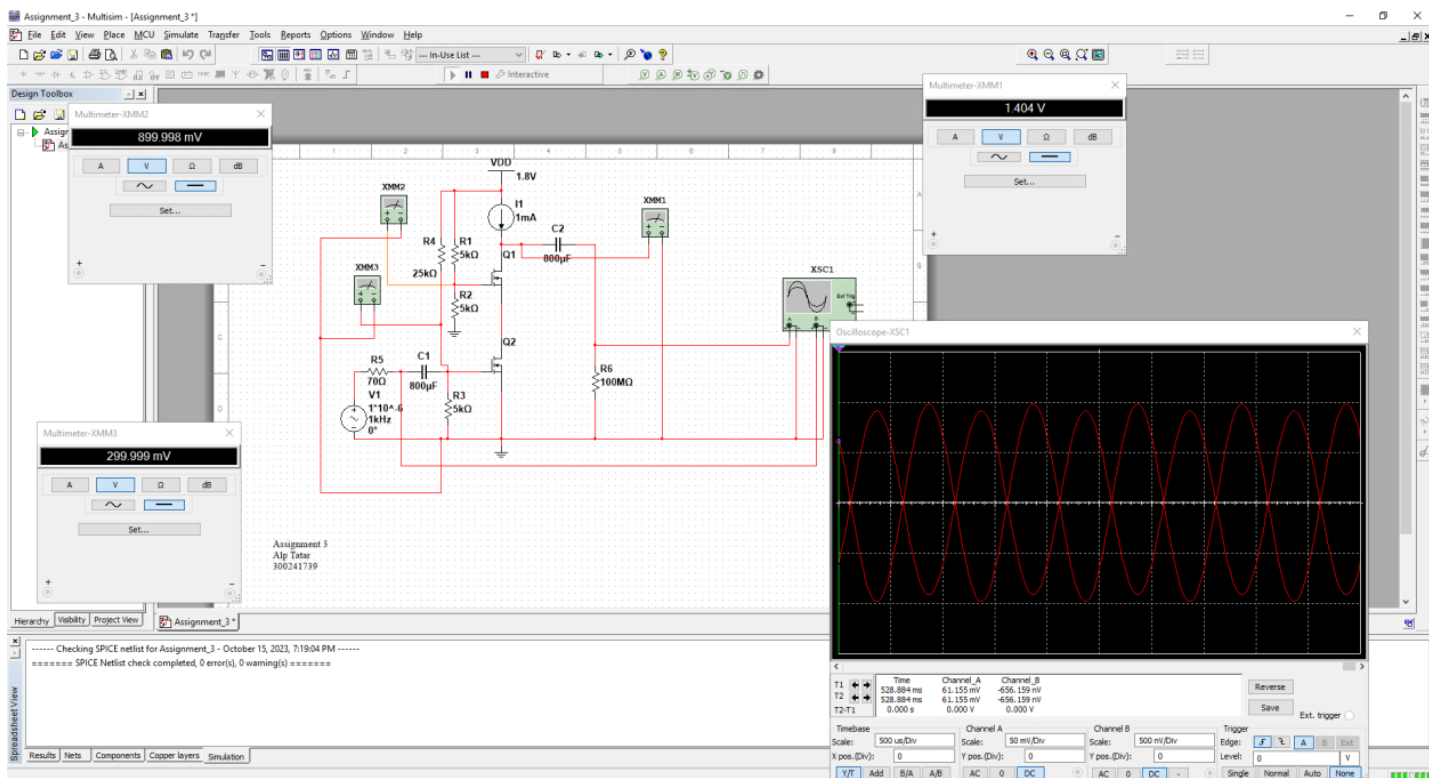
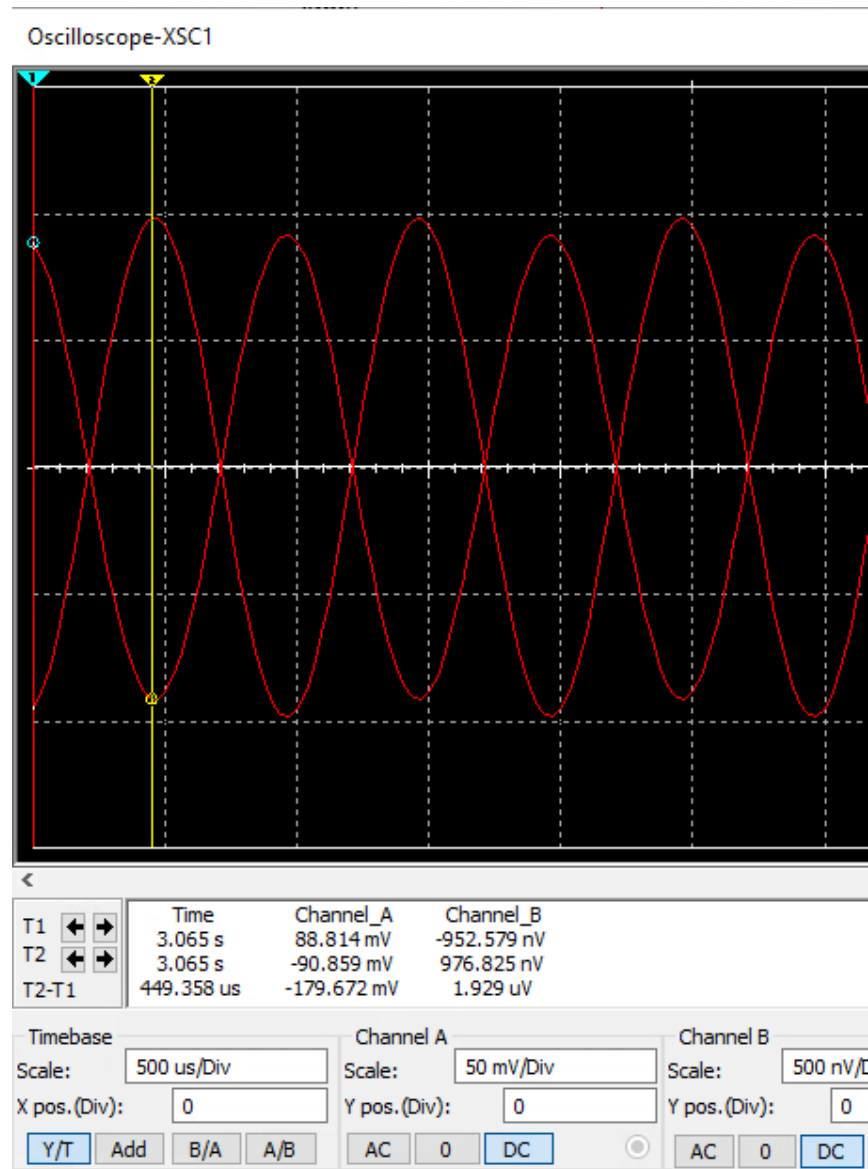


Figure 2: Design of Circuit From Assignment 2 Alongside General Desgin

## Design Decisions

The selection of resistance R6 (Rout) was predicated on the theoretical requirement for an output resistance approaching infinity while maintaining an open circuit configuration. However, a  $100\text{M}\Omega$  resistance value was deemed suitable, acknowledging the inherent limitation of achieving infinite resistance and enhancing the representation of the circuit's gain characteristics. In parallel, a  $70\Omega$  resistance for R5 (Rsig) was chosen to correspond to the established input resistance of Vsig. This  $70\Omega$  value aligns with customary industry practices for the selection of Rsig values. The choice of resistances for R1, R2, R3, and R4 was rooted in their common availability in real-world applications and laboratory environments, with the emphasis placed on their relative proportions rather than their absolute values.

Finally, the capacitance values were derived from an equation prescribed as  $f = \frac{1}{2\pi CXc}$ .



*Figure 3: Oscilloscope Measurements of the Design*

$$\text{Gain} = \frac{88.814 \cdot 10^{-3}}{-952.58910^{-9}} = -96234.33296 \approx 10^{-5} \text{ as seen from Assignment 2}$$

### **Challenges and Problems**

Several challenges were encountered during the course of this experiment. Initially, the process of configuring transistor parameters within MultiSim posed a difficulty, requiring some time to locate the necessary settings for adjustment. Subsequently, the utilization of a  $100\text{M}\Omega$  Rout resistance yielded unexpected gain results, prompting a series of trial and error iterations to identify the underlying issue stemming from Rout's resistance value.

Another noteworthy issue confronted at the assignment's inception was the inexplicable transition from kilovolts (KV) to megavolts (MV) voltage output. This puzzling behavior was eventually resolved after multiple rounds of trial and error.

In addition to the aforementioned challenges, it is essential to acknowledge that MultiSim simulations may introduce several potential issues. These include inaccuracies in component models, convergence difficulties, transient analysis convergence problems, and challenges related to transient noise analysis, which can affect the accuracy and reliability of simulation results.

MOS\_N

Label

Display

Value

Fault

Pins

Variant

Instance parameters:

Tools

Views

Name	Description	Value	Units	Use default	Show on schematic
L	Length	0.18u	m	<input type="checkbox"/>	None
W	Width	1.59u	m	<input type="checkbox"/>	None
M	Multiplicity	1		<input checked="" type="checkbox"/>	None
AD	Drain area	0	m <sup>2</sup>	<input checked="" type="checkbox"/>	None
AS	Source area	0	m <sup>2</sup>	<input checked="" type="checkbox"/>	None
PD	Drain perimeter	0	m	<input checked="" type="checkbox"/>	None
PS	Source perimeter	0	m	<input checked="" type="checkbox"/>	None
NRD	Drain squares	1		<input checked="" type="checkbox"/>	None
NRS	Source squares	1		<input checked="" type="checkbox"/>	None
TEMP	Instance temperature	27	°C	<input checked="" type="checkbox"/>	None
OFF	Device initially off	0		<input checked="" type="checkbox"/>	None
ICVDS	Initial D-S voltage	0	V	<input checked="" type="checkbox"/>	None
ICVGS	Initial G-S voltage	0	V	<input checked="" type="checkbox"/>	None
ICVBS	Initial B-S voltage	0	V	<input checked="" type="checkbox"/>	None

Device model level: MOS 1 (Level 1)

Edit component in DB

Save component to DB

Edit package

Edit model

Replace...

OK

Cancel

Help

Figure 4: Global Transistor Parameters

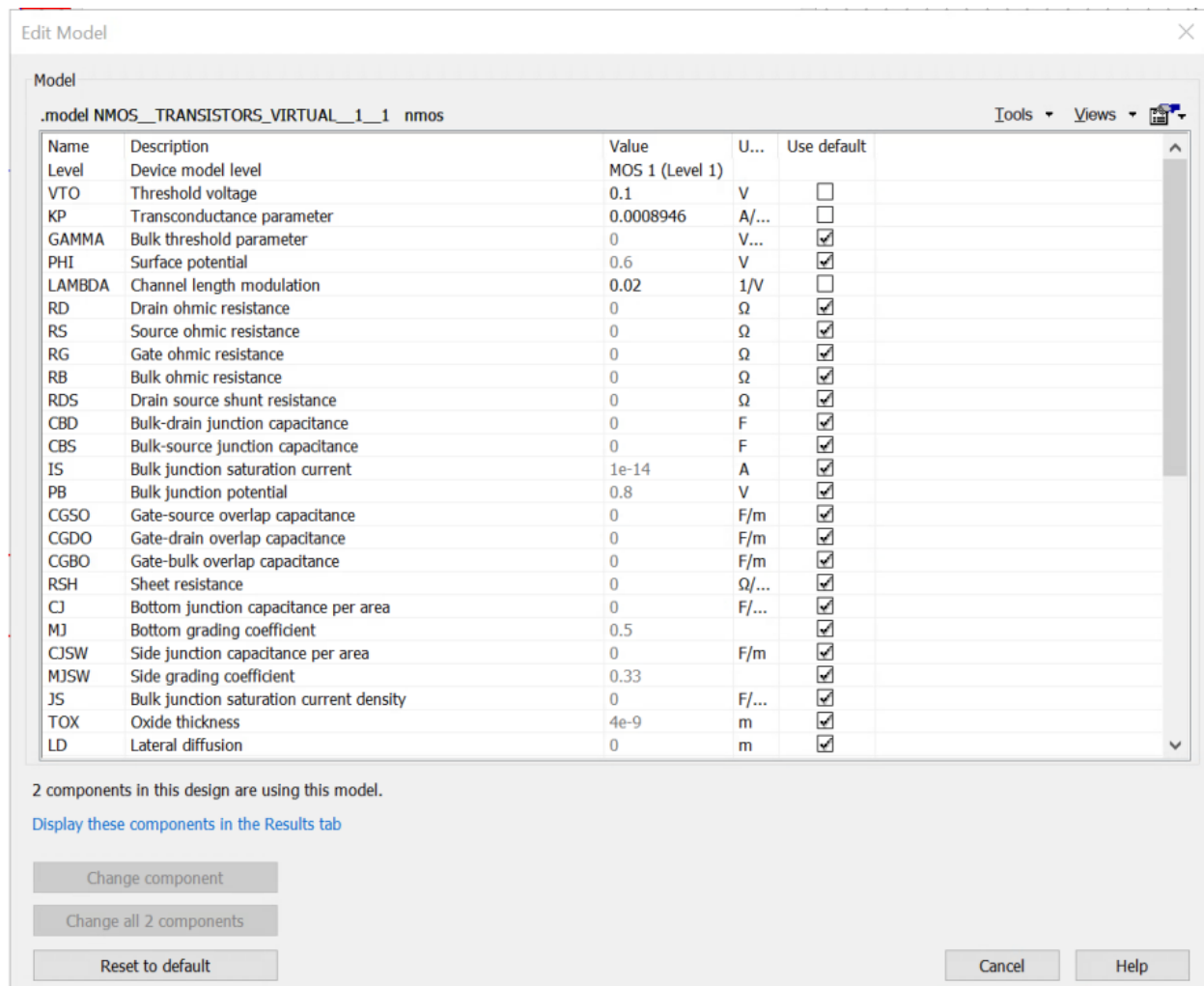


Figure 5: Transistor Parameters for Question One

## Conclusion

The design and construction of the cascode amplifier circuit in MultiSim were both insightful and challenging. Key design decisions included selecting resistance values for R6 (Rout) and R5 (Rsig) to meet the circuit's requirements and choosing common resistances for R1, R2, R3, and R4. Capacitance values were derived from a prescribed equation.

Despite the intention for a robust design, challenges arose. Configuring transistor parameters proved initially perplexing, necessitating time to locate the appropriate settings for adjustment. The selection of a 100M $\Omega$  Rout resistance led to unexpected gain results, requiring iterative trial-and-error solutions.

A peculiar transition from kilovolts (KV) to megavolts (MV) in voltage output was observed initially but was eventually resolved through repeated trial and error. Furthermore, MultiSim simulations introduced potential issues such as inaccuracies in component models, convergence difficulties, and challenges with transient analysis.



In conclusion, this assignment provided valuable insights into the complexities of electronic circuit design and simulation, highlighting the significance of parameter selection, biasing, and rigorous testing for accurate and dependable results.