CS 224

Lab06

Sec04

Preliminary Design Report

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Question 1.

no	Cache size KB	N way cache	Word size in bits	Block size(no .of words)	No. of sets	Tag size in bits	Index size(set no.) in bits	Word block offset size in bits1	Byte Offset Size in bits2	Block replacement policy needed(yes/no)
1	128	1	32	4	2^13	15	13	2	2	no
2	128	2	32	4	2^12	16	12	2	2	yes
3	128	4	32	8	2^10	17	10	3	2	yes
4	128	full	32	8	1	27	0	3	2	yes
9	256	1	16	4	2^15	14	15	2	1	no
10	256	2	16	4	2^14	15	14	2	1	yes
11	256	4	16	16	2^11	16	11	4	1	yes
12	256	full	16	16	1	27	0	4	1	yes

Question 2.

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 00 24	00	no
00 00 00 42	00	no
00 00 00 68	01	no
00 00 00 04	00	no
00 00 00 0C	01	no
00 00 00 4C	01	no

Question 3.

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 00 2C	01	no
00 00 00 48	01	no
00 00 00 44	00	no
00 00 00 0C	01	no
00 00 00 04	00	no
00 00 00 0C	01	yes

Question 4.

Name	**Time**	**Miss rate**
L1	1 clock cycle	20%
L2	2 clock cycle	5%
Main memory	20 clock cycle	

AMAT = Time of L1 + miss rate of L1 * (time of L2 + (miss rate of L2 * time of MM))

= 1 + 0.2 * (2+(0.05*20))

= 1.6

4ghz => clock period = 0.25 ns

1.6 * 0.25ns * 10^12 = 400 s (1ns = 10^-9s)