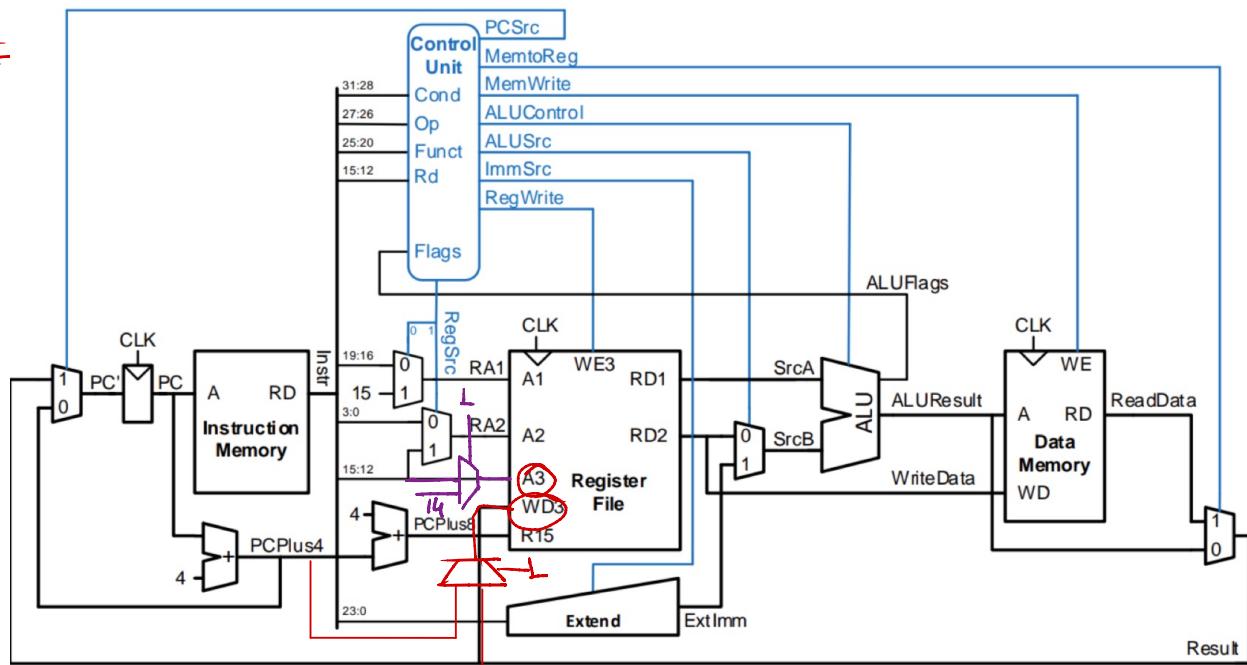


1.2.1

BL

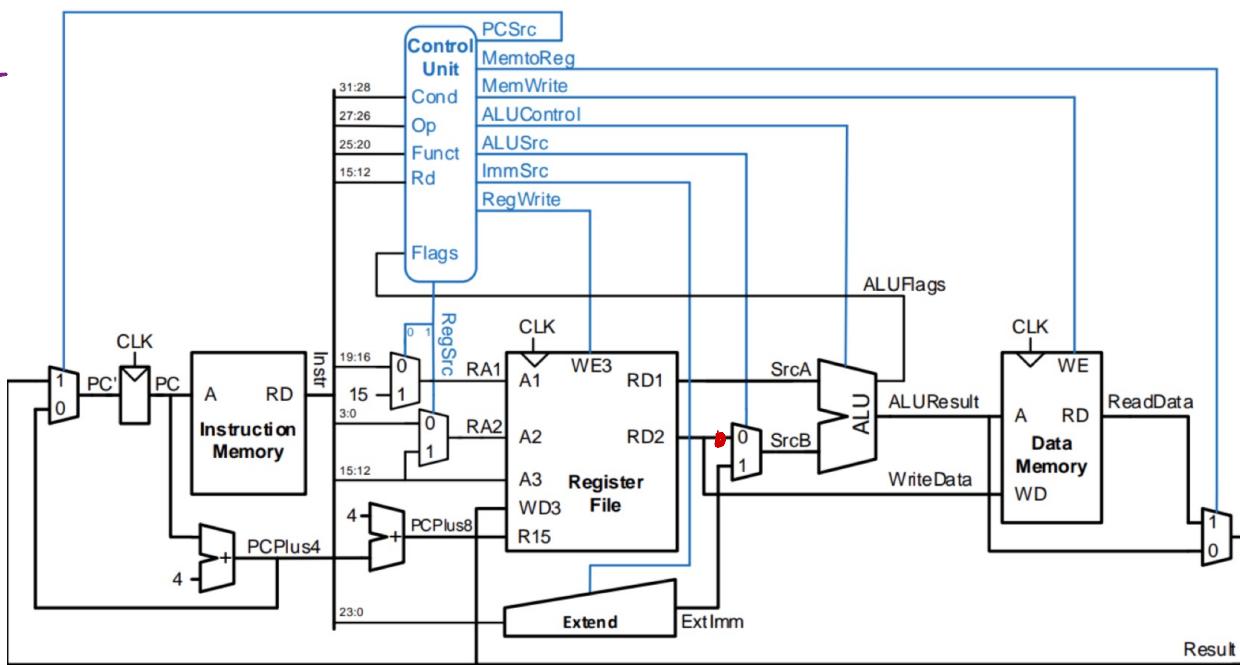


Red mux → Output WD3  
Input 0 → Result  
Input 1 → RD2  
Select → Opcode[1] & L

Purple mux → Output A3  
Input 0 → ISTR[15:12]  
Input 1 → 14  
Select → Opcode[1] & L

Selects would be only opcode = 10 and 11 which represents BL  
since ALU-Src = L our changing will not effect anything

MOV



I placed a shifter to red point, in order to get immediate shifting.  
There are three muxes to run this shifter

Shifter control Mux →

Input 0 = INSTR 6:5

Input 1 = 11

Select → I

Output → Shifter Control

111100  
|  
1000100

Shifter Data Mux →

Input 0 → RD2

Input 1 → imm8

Select → I

Output → Data

1000000 → R14

Shifter Shunt Mux →

Input 0 → INSTR 11:7

Input 1 → INSTR 11:8 << 1

Select → I

Output → shunt

When I=1 shifter goes to immediate form.

## 1.2.2

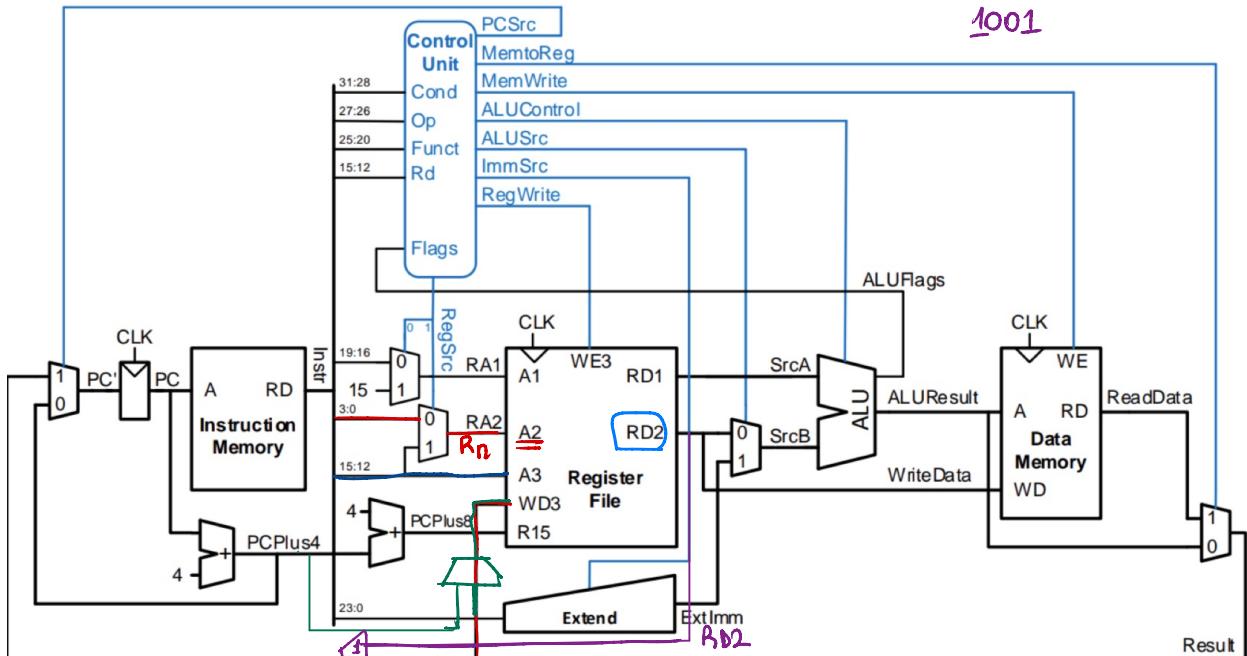
I did not put MOV in controller

However I did some changes in controller for BX, BL.

Since we need to add PC+8, R1=R15 so that RegSrc[0] = 1  
RegSrc[1] = X

ALU-CONTROL = 0100 ⇒ ADD → (PC+8) + Imm

→ For that ALU-Src = 1



$R_{n1}$  always  $R_n$  value       $RegSrc\ 1 = 0 \quad RegSrc\ 0 = \alpha$   
 when BX is used       $Funct3 \& Funct0 \& \neg Funct1 \& \neg Funct2$

If we set  $WE = 1$       we can import  $R_n$  value to  $R_{15}$

I have connected the output of purple mux to input-1 of Mux-PC.

## 1.2.2

Whereas I did some modifications in controller for BX, not for B, BL, mov.  
 Because all modifications is in datapath. The biggest one is to use BX in DP mode  
 Since it has constant byte set Funct part will be 1001 but we know that  
 there is no operation for 1001 in ALU, therefore we can use it.

# Top Level Design (1.2.3)

```
//=====
// This code is generated by Terasic System Builder
//=====

]module Project_top_module(
    ////////////// SEG7 //////////
    output      [6:0]    HEX0,
    output      [6:0]    HEX1,
    output      [6:0]    HEX2,
    output      [6:0]    HEX3,
    output      [6:0]    HEX4,
    output      [6:0]    HEX5,
    ////////////// KEY //////////
    input       [3:0]    KEY,
    ////////////// LED //////////
    output      [9:0]    LEDR,
    ////////////// SW //////////
    input       [9:0]    SW
);

wire [31:0] reg_out, PC;
hexto7seg hex_0 (.hexn(HEX0),.hex(reg_out[3:0]));
hexto7seg hex_1 (.hexn(HEX1),.hex(reg_out[7:4]));

assign HEX2 = 7'b1111111;
assign HEX3 = 7'b1111111;

hexto7seg hex_4 (.hexn(HEX4),.hex(PC[3:0]),);
hexto7seg hex_5 (.hexn(HEX5),.hex(PC[7:4]),);

]COMPUTER_MODULE my_computer (.clk(~KEY[0]),.reset(~KEY[1]),.debug_reg_select(SW[3:0]),
    .debug_reg_out(reg_out),.PC(PC));
endmodule
```

## Test Bench (T.2.b)



```
89999.00ns DEBUG Performance Model ***** Clock cycle: 7 *****
89999.00ns DEBUG Performance Model ***** Instruction No: 8 *****
89999.00ns DEBUG Performance Model ***** Current Instruction *****
89999.00ns DEBUG Performance Model Binary string:11100011010000000111111001000110
89999.00ns DEBUG Performance Model Operation type Data Processing
89999.00ns DEBUG Performance Model cond:E
89999.00ns DEBUG Performance Model Immediate bit:0
89999.00ns DEBUG Performance Model cmd:D
89999.00ns DEBUG Performance Model Set bit:0
89999.00ns DEBUG Performance Model Rn:0 Rd:7
89999.00ns DEBUG Performance Model shamt:28 sh:2 Rm:6
89999.00ns DEBUG Performance Model ***** DUT DATAPATH Signals *****
89999.00ns DEBUG Performance Model ***** DUT Controller Signals *****
89999.00ns DEBUG Performance Model ***** Performance Model / DUT Data *****
89999.00ns DEBUG Performance Model PC:36 PC:36
89999.00ns DEBUG Performance Model Register0: 0 0
89999.00ns DEBUG Performance Model Register1: 19 19
89999.00ns DEBUG Performance Model Register2: 38 38
89999.00ns DEBUG Performance Model Register3: 2 2
89999.00ns DEBUG Performance Model Register4: 76 76
89999.00ns DEBUG Performance Model Register5: 10 10
89999.00ns DEBUG Performance Model Register6: 2147483650 2147483650
89999.00ns DEBUG Performance Model Register7: 4294967288 4294967288
89999.00ns DEBUG Performance Model Register8: 0 0
89999.00ns DEBUG Performance Model Register9: 0 0
89999.00ns DEBUG Performance Model Register10: 0 0
89999.00ns DEBUG Performance Model Register11: 0 0
89999.00ns DEBUG Performance Model Register12: 0 0
89999.00ns DEBUG Performance Model Register13: 0 0
89999.00ns DEBUG Performance Model Register14: 0 0
89999.00ns DEBUG Performance Model Register15: 44 44
89999.00ns DEBUG Performance Model ***** Clock cycle: 8 *****
89999.00ns DEBUG Performance Model ***** Instruction No: 9 *****
89999.00ns DEBUG Performance Model ***** Current Instruction *****
89999.00ns DEBUG Performance Model Binary string:111001011000000010010000001010101
89999.00ns DEBUG Performance Model Operation type Memory
89999.00ns DEBUG Performance Model Load bit:0
89999.00ns DEBUG Performance Model Rn:1 Rn:2
89999.00ns DEBUG Performance Model imm12:85
89999.00ns DEBUG Performance Model ***** DUT DATAPATH Signals *****
89999.00ns DEBUG Performance Model ***** DUT Controller Signals *****
89999.00ns DEBUG Performance Model ***** Performance Model / DUT Data *****
100000.00ns DEBUG Performance Model PC:40 PC:40
100000.00ns DEBUG Performance Model Register0: 0 0
100000.00ns DEBUG Performance Model Register1: 19 19
100000.00ns DEBUG Performance Model Register2: 38 38
100000.00ns DEBUG Performance Model Register3: 2 2
100000.00ns DEBUG Performance Model Register4: 76 76
100000.00ns DEBUG Performance Model Register5: 10 10
100000.00ns DEBUG Performance Model Register6: 2147483650 2147483650
100000.00ns DEBUG Performance Model Register7: 4294967288 4294967288
100000.00ns DEBUG Performance Model Register8: 0 0
100000.00ns DEBUG Performance Model Register9: 0 0
100000.00ns DEBUG Performance Model Register10: 0 0
100000.00ns DEBUG Performance Model Register11: 0 0
100000.00ns DEBUG Performance Model Register12: 0 0
100000.00ns DEBUG Performance Model Register13: 0 0
100000.00ns DEBUG Performance Model Register14: 0 0
100000.00ns DEBUG Performance Model Register15: 48 48
100000.00ns DEBUG Performance Model ***** Clock cycle: 9 *****
100000.00ns DEBUG Performance Model ***** Instruction No: 10 *****
100000.00ns DEBUG Performance Model ***** Current Instruction *****
100000.00ns DEBUG Performance Model Binary string:11100101100100111000000001100110
100000.00ns DEBUG Performance Model Operation type Memory
100000.00ns DEBUG Performance Model Load bit:1
100000.00ns DEBUG Performance Model Rn:3 Rn:8
100000.00ns DEBUG Performance Model imm12:162
100000.00ns DEBUG Performance Model ***** DUT DATAPATH Signals *****
100000.00ns DEBUG Performance Model ***** DUT Controller Signals *****
100000.00ns DEBUG Performance Model ***** Performance Model / DUT Data *****
110000.00ns DEBUG Performance Model PC:44 PC:44
110000.00ns DEBUG Performance Model Register0: 0 0
110000.00ns DEBUG Performance Model Register1: 19 19
110000.00ns DEBUG Performance Model Register2: 38 38
110000.00ns DEBUG Performance Model Register3: 2 2
110000.00ns DEBUG Performance Model Register4: 76 76
110000.00ns DEBUG Performance Model Register5: 10 10
110000.00ns DEBUG Performance Model Register6: 2147483650 2147483650
110000.00ns DEBUG Performance Model Register7: 4294967288 4294967288
110000.00ns DEBUG Performance Model Register8: 38 38
110000.00ns DEBUG Performance Model Register9: 0 0
110000.00ns DEBUG Performance Model Register10: 0 0
110000.00ns DEBUG Performance Model Register11: 0 0
110000.00ns DEBUG Performance Model Register12: 0 0
110000.00ns DEBUG Performance Model Register13: 0 0
110000.00ns DEBUG Performance Model Register14: 0 0
110000.00ns DEBUG Performance Model Register15: 52 52
110000.00ns DEBUG Performance Model ***** Clock cycle: 10 *****
110000.00ns DEBUG Performance Model ***** Instruction No: 11 *****
110000.00ns DEBUG Performance Model ***** Current Instruction *****
110000.00ns DEBUG Performance Model Binary string:11100001010100100000000000000001000
110000.00ns DEBUG Performance Model Operation type Data Processing
110000.00ns DEBUG Performance Model cond:E
110000.00ns DEBUG Performance Model Immediate bit:0
110000.00ns DEBUG Performance Model cmd:A
110000.00ns DEBUG Performance Model Set bit:1
110000.00ns DEBUG Performance Model Rn:2 Rd:0
110000.00ns DEBUG Performance Model shamt:0 sh:0 Rm:8
110000.00ns DEBUG Performance Model ***** DUT DATAPATH Signals *****
110000.00ns DEBUG Performance Model ***** DUT Controller Signals *****
110000.00ns DEBUG Performance Model ***** Performance Model / DUT Data *****
120000.00ns DEBUG Performance Model PC:48 PC:48
120000.00ns DEBUG Performance Model Register0: 0 0
120000.00ns DEBUG Performance Model Register1: 19 19
120000.00ns DEBUG Performance Model Register2: 38 38
120000.00ns DEBUG Performance Model Register3: 2 2
120000.00ns DEBUG Performance Model Register4: 76 76
120000.00ns DEBUG Performance Model Register5: 10 10
120000.00ns DEBUG Performance Model Register6: 2147483650 2147483650
120000.00ns DEBUG Performance Model Register7: 4294967288 4294967288
120000.00ns DEBUG Performance Model Register8: 38 38
120000.00ns DEBUG Performance Model Register9: 0 0
120000.00ns DEBUG Performance Model Register10: 0 0
120000.00ns DEBUG Performance Model Register11: 0 0
120000.00ns DEBUG Performance Model Register12: 0 0
120000.00ns DEBUG Performance Model Register13: 0 0
120000.00ns DEBUG Performance Model Register14: 0 0
120000.00ns DEBUG Performance Model Register15: 56 56
120000.00ns DEBUG Performance Model ***** Clock cycle: 11 *****
120000.00ns DEBUG Performance Model ***** Instruction No: 12 *****
120000.00ns DEBUG Performance Model ***** Current Instruction *****
120000.00ns DEBUG Performance Model Binary string:000110100000000000000000000000010001
```

