2020-2021 Spring Semester

Lab-3 Preliminary Report

Course Name:CS223

Section: 1

Lab: 3

Name: Alper

Surname: Mumcular

Student ID: 21902740

Date: 11.03.2021

Trainer Pack: 19

1.1) Behavioral SystemVerilog module for 2-to-4 decoder

```
module decoder2to4( input logic [1:0] i, output logic [3:0] out );
	assign out[0] = ~i[1] & ~i[0];
	assign out[1] = ~i[1] & i[0];
	assign out[2] = i[1] & ~i[0];
	assign out[3] = i[1] & i[0];
endmodule
```

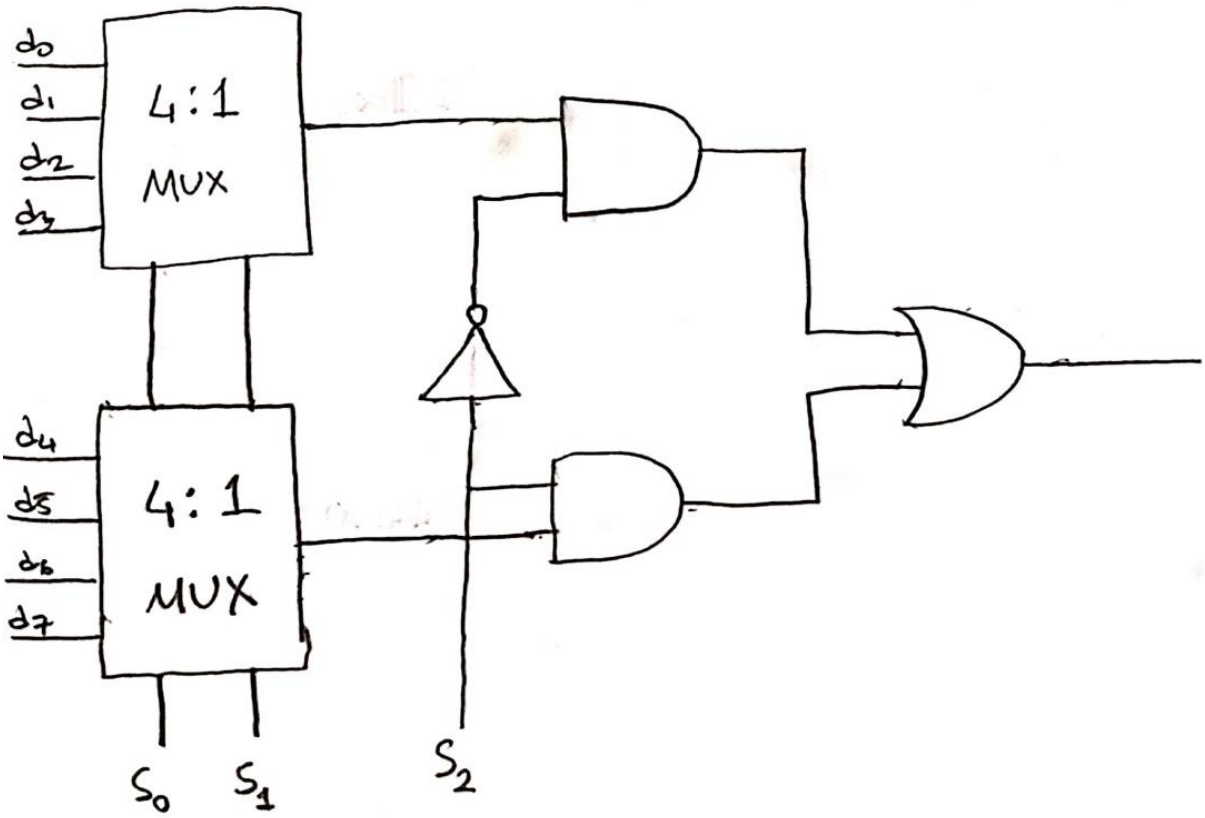
1.2) Testbench for 2-to-4 decoder

```
module testbenchdecoder2to4();
	logic[1:0] i;
	logic[3:0] out;
	decoder2to4 dut( i, out );
	initial begin
		i[0] = 0; i[1] = 0; #10;
		i[0] = 1; #10;
		i[0] = 0; i[1] = 1; #10;
		i[0] = 1; #10;
	end
endmodule
```

2) Behavioral SystemVerilog module for 4-to-1 multiplexer

```
module mux4to1( input logic s1, s0, d0, d1, d2, d3, output logic out );
	logic[1:0] x;
	assign x[0] = s0 ? d1 : d0;
	assign x[1] = s0 ? d3 : d2;
	assign out = s1 ? x[1] : x[0];
endmodule
```

3.1) Schematic of 8-to-1 MUX



3.2) Structural SystemVerilog Module of 8-to-1 MUX

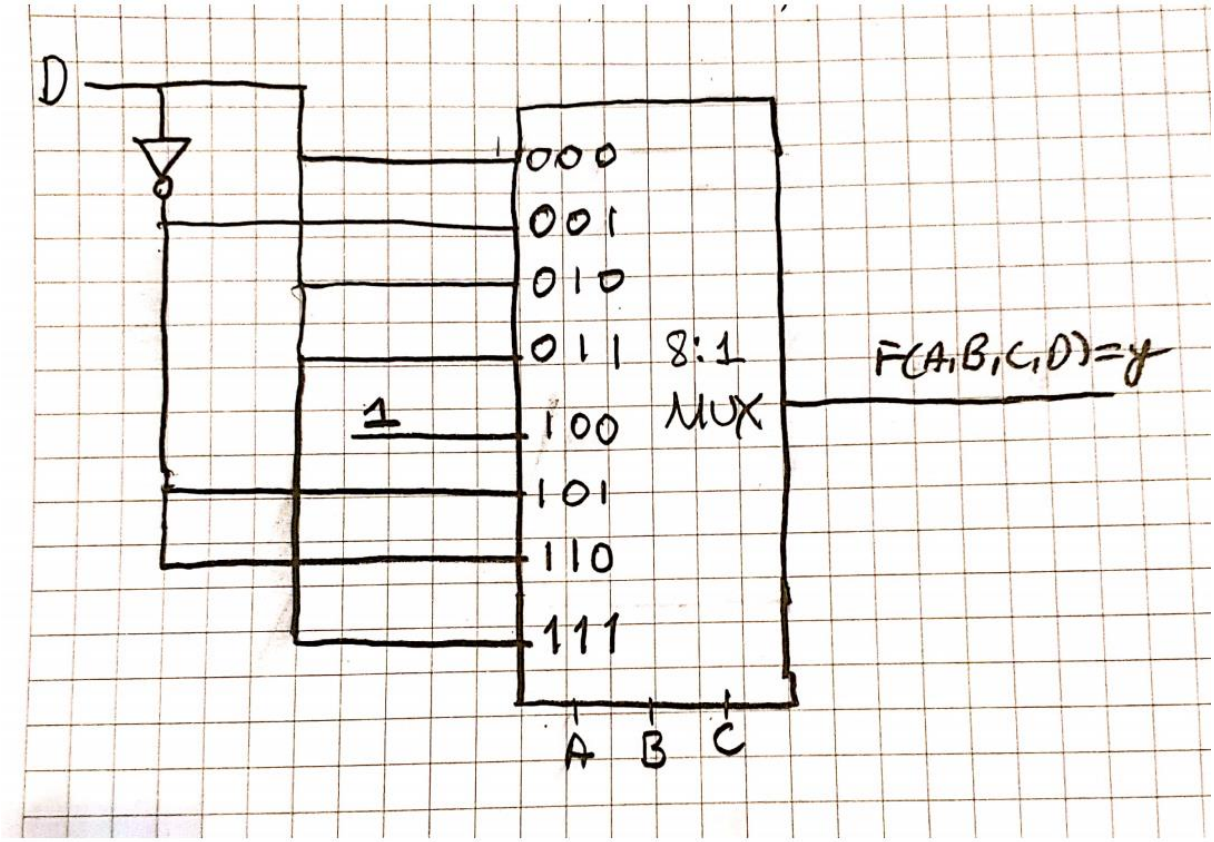
```
module mux8to1( input logic a, b, c, d0, d1, d2, d3, d4, d5, d6, d7, output logic
out);
        logic [1:0] x;
        logic [1:0] and_out;
        mux4to1 mux1( b, c, d0, d1, d2, d3, x[0] );
        mux4to1 mux2( b, c, d4, d5, d6, d7, x[1] );
        and and1 ( and_out[0], x[0], ~a );
        and and2 ( and_out[1], x[1], a );
        or or1 ( out, and_out[0], and_out[1] );
endmodule
```

3.3) Testbench for 8-to-1 MUX

```
module testbench8to1mux();
        logic a, b, c, d;
        logic out;
        mux8to1 dut(a, b, c, d, ~d, d, d, 1, ~d, ~d, d, out);
```

```
        initial begin
                a=0; b=0; c=0; d=0; #10;
                d=1; #10;
                c=1; d=0; #10;
                d=1; #10;
                b=1; c=0; d=0; #10;
                d=1; #10;
                c=1; d=0; #10;
                d=1; #10;
                a=1; b=0; c=0; d=0; #10;
                d=1; #10;
                c=1; d=0; #10;
                d=1; #10;
                b=1; c=0; d=0; #10;
                d=1; #10;
                c=1; d=0; #10;
                d=1; #10;
        end
endmodule
```

4.1) Schematic of F(A,B,C,D) = ∑(1,2,5,7,8,9,10,12,15)



4.2) SystemVerilog module for F(A,B,C,D) = ∑(1,2,5,7,8,9,10,12,15)

```
module F( input logic a, b, c, d, output logic y);
        mux8to1 func(a, b, c, d, ~d, d, d, 1, ~d, ~d, d, y);
endmodule
```