Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring 2023-2024

Lab 1

Due date: March 22, 2024, Friday, 23:55
No late submissions

1 Introduction

This laboratory aims to familiarize you with basic logic gates and combinational circuit design. You will simplify the circuit that is explained below and draw the circuit using the Logisim tool with the given gates.

2 IC Pool

- 74LS04 (NOT, Inverter)
- 74LS08 (AND)
- 74LS32 (OR)

3 Lab Work

In this assignment, you are expected to perform the operations described in the following section.

3.1 Specifications

Suppose A and B are 2-bit binary **input** numbers and **X**, **Y** and **Z** are 1-bit binary **output** numbers. A and B are represented with A_1, A_0, B_1, and B_0 bits, respectively, where A_1 and B_1 are the most significant bits and A_0 and B_0 are the least significant bits of the corresponding numbers, respectively. Your circuit will take A and B as inputs and yield the outputs **X**, **Y** and **Z** with the following behavior:

$$\mathbf{X} = \begin{cases} 1 & (A+B) \equiv 1 \mod 2 \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Y} = \begin{cases} 1 & (B*A) \geq (A+B) \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Z} = \begin{cases} 1 & \frac{1}{1+\exp(-1*(0.15*A_1-0.23*A_0+0.15*B_1-0.40*B_0-0.05))} > 0.5 \\ 0 & \text{otherwise} \end{cases}$$

Note: $\exp(x)$ stands for e^x ('e' is the Euler number).

You have to use "input pins" and "output pins" for your inputs and outputs, respectively, from the Toolbar at the top of Logisim. Please set their labels correctly using the following names. **Please, only set the "label" property of the "pin" objects; do not add a "text" object (A) instead of a label; however, you may add "text" objects in order to take notes or comment about your design.**

The labeling should be done as follows:
Input pins: A1, A0, B1, B0.
Output pins: X, Y, Z.

Each input pin corresponds to a digit in a 2-bit binary number. If it is set, then the value of the digit is 1. If it is reset, then the value of the digit is 0.

Note: You are expected to implement your circuitry using only the ICs specified in the IC pool section.

3.2 Input Output Examples

1. Suppose $A_1A_0 = 00$ and $B_1B_0 = 10$. In this case, A=0 and B=2 in decimal.
   $A + B = 2$
   Since $A + B \equiv 0 \mod 2$, the output X is 0.

2. Suppose $A_1A_0 = 10$ and $B_1B_0 = 01$. In this case, A=2 and B=1 in decimal.
   $A + B = 3$
   Since $A + B \equiv 1 \mod 2$, the output X is 1.

3. Suppose $A_1A_0 = 01$ and $B_1B_0 = 01$. In this case, A=1 and B=1 in decimal.
   $B * A = 1, A + B = 2$
   Since $B * A < A + B$, the output Y is 0.

4. Suppose $A_1A_0 = 11$ and $B_1B_0 = 11$. In this case, A=3 and B=3 in decimal.
   $B * A = 9, A + B = 6$
   Since $B * A > A + B$, the output Y is 1.

5. Suppose $A_1A_0 = 01$ and $B_1B_0 = 10$. In this case, A_1=0, $A_0 = 1$, $B_1 = 1$, and B_0=0.
   $\frac{1}{1+e^{-1*(0.15*A_1-0.23*A_0+0.15*B_1-0.40*B_0-0.05)}} = 0.468$
   Since $0.468 < 0.5$, the output Z is 0.

6. Suppose $A_1A_0 = 00$ and $B_1B_0 = 10$. In this case, A_1=0, $A_0 = 0$, $B_1 = 1$, and B_0=0.
   $\frac{1}{1+e^{-1*(0.15*A_1-0.23*A_0+0.15*B_1-0.40*B_0-0.05)}} = 0.525$
   Since $0.525 > 0.5$, the output Z is 1.

4 Free Session

There will be a "free session week" between March 18 and March 22 (Your specific session will be announced later). You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard using IC components and practice handling possible problems related to a physical circuit.

5 Demo Session

There will be a 2-hour-long "demo session week" following the free session week. In demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard.
- You will show that the circuit drawn in Logisim works as specified.

6 Deliverables

1. Please submit the circuit named `e1234567.circ` prepared in Logisim, which is your preliminary work, until the specified deadline. Please do not forget to replace `e1234567` with your 7-digit student ID. The evaluation of the submission will be a black-box test. **You should use the CENG version of Logisim that is available on the ODTUClass course page. Circuits designed with other Logisim versions, other tools, or not named properly will not be graded!**
2. In the demo session, you will reconstruct and show that the circuit drawn in Logisim works physically. This part will be graded in the lab.

Note: Your overall Lab 1 grade is going to be calculated from the Logisim assignment score, lab demo score, and quiz score.

7 What to Bring in the Lab

- Circuit designs prepared with CENG 232 Logisim (you can have them printed or downloaded on your phone/tablet, etc.).
- Data sheets of chips (you can have them printed or downloaded on your phone/tablet, etc.). www.alldatasheet.com
- Pencil and eraser, as you will have a quiz at the very beginning of the DEMO lab.

Note: The lab materials (gates, cables, etc.) will be distributed at the beginning of each lab session and will be collected at the end of the session. Therefore, you do not have to buy them. If you want to work out of the labs, you may still buy them. Moreover, if you would like to work with your own equipment (ICs, breadboard, cables, etc), you are free to bring them to the sessions as well.

8 Cheating Policy

All the lab work should be **individual**, and there is a zero-tolerance policy for cheating. See the course website for further information about the cheating policy.

9 References

- CENG 232 Logisim Version
- Discussions Forum